AS3681

DataSheet

Power and Lighting Management Unit

1 General Description

The AS3681 is a highly-integrated CMOS Power and Lighting Management Unit to supply power to LCD-and camera-modules in mobile telephones, and other 1-cell Li+ or 3-cell NiMH powered devices.

The AS3681 incorporates one low-power, low-dropout regulator (LDO), one Step Up DC/DC Converter for white backlight LEDs, one high-power Charge Pump for camera flash LEDs, one Analog-to-Digital Converter, support for up to 11 current sinks, a serial interface, and control logic all onto a single die.

The linear analog regulator features extremely high analog performance regarding:

- Noise (< 30µVrms from 100Hz to 100kHz)
- Line/load Regulation
  (<1mV Static and <20mV Transient)
- Power Supply Rejection (>70dB@1kHz)
- Ultra-Low Power Consumption
  (1µA Shutdown, 6µA Standby)

LDO output voltages and output currents are programmable via a serial interface.

2 Key Features

- Programmable High-Performance Regulator
  - Low-Noise LDO (1.85 to 3.4V, 150mA)
  - 2.8V Default Output Voltage after Power-up
  - 3µA Quiescent Current in Standby (I_{out} <5mA)
  - Turns On/Off with Rising/Falling Edge of GPIO Supply Voltage
  - Programmable via Serial Interface
- High-Efficiency Step Up DC/DC Converter
  - Up to 25V/50mA for White LEDs
  - Programmable Output Voltage with External Resistors and Serial Interface
- High-Efficiency High-Power Charge Pump
  - 1:1, 1.5:1, and 2:1 Mode
  - Output Current up to 400mA
  - Efficiency up to 95%
  - Only 4 External Capacitors Required:
    2 x 1µF Flying Capacitors, 2 x 2.2µF Input/Output Capacitors
  - Supports LCD White Backlight LEDs,
    Camera Flash White LEDs, and Keypad Backlight LEDs
- Supports up to 11 Current Sinks
  - Three Programmable (4-bit) from: 10 to 300mA
  - Two Programmable (4-bit) from: 2.5 to 37.5 mA
  - Three Programmable (4-bit) from: 2.5 to 37.5 mA for RGB LEDs
  - Three Programmable (4-bit) from: 2.5 to 37.5mA for General Purpose Applications
  - Programmable Hardware Control (Strobe, PWM)
  - Selectively Enable/Disable Current Sinks
- 10-bit Successive Approximation ADC
  - 11µs Conversion Time
  - Two Selectable Inputs: GPIO0 and GPIO1
- Four General Purpose Inputs/Outputs
  - Digital Input, Digital Output, and Tristate
  - Programmable Pull-Up, and Pull-Down
  - GPIO2 can be used as Camera Flash Strobe
- Negative or High-Voltage Charge Pump
  - Regulated Output Voltage, Programmable by Dual Resistors e.g. -6V, 10mA for OLED or ±15V, 5mA for TFT
  - ±5% Accuracy
  - Requires Few External Components
- Standby LDO
  - Regulated 2.5V
  - Maximum Output Current 10mA
  - Always On (Supplies Internal Digital Blocks)
  - 3µA Quiescent Current
- Wide Battery Supply Range: 3.0 to 5.5V
- Serial Interface Control
- On-Chip Bandgap Tuning for High Accuracy (±1%)
- Overcurrent and Thermal Protection
- 32-Pin, Small Form-Factor QFN Package
  (5 x 5 x 1mm, 0.5mm pitch), Enhanced Thermal Characteristics
- 1 Watt Power Dissipation @ T_{AMB} = 70ºC

3 Application

Power- and lighting-management for mobile telephones and other 1-cell Li+ or 3-cell NiMH powered devices.

4 Block Diagrams

Figure 1. Serial LED Configuration Option (by software): Step Up DC/DC Converter (Pins 23, 24, 28, 29) and External Charge Pump (Pins 25, 26, 27)

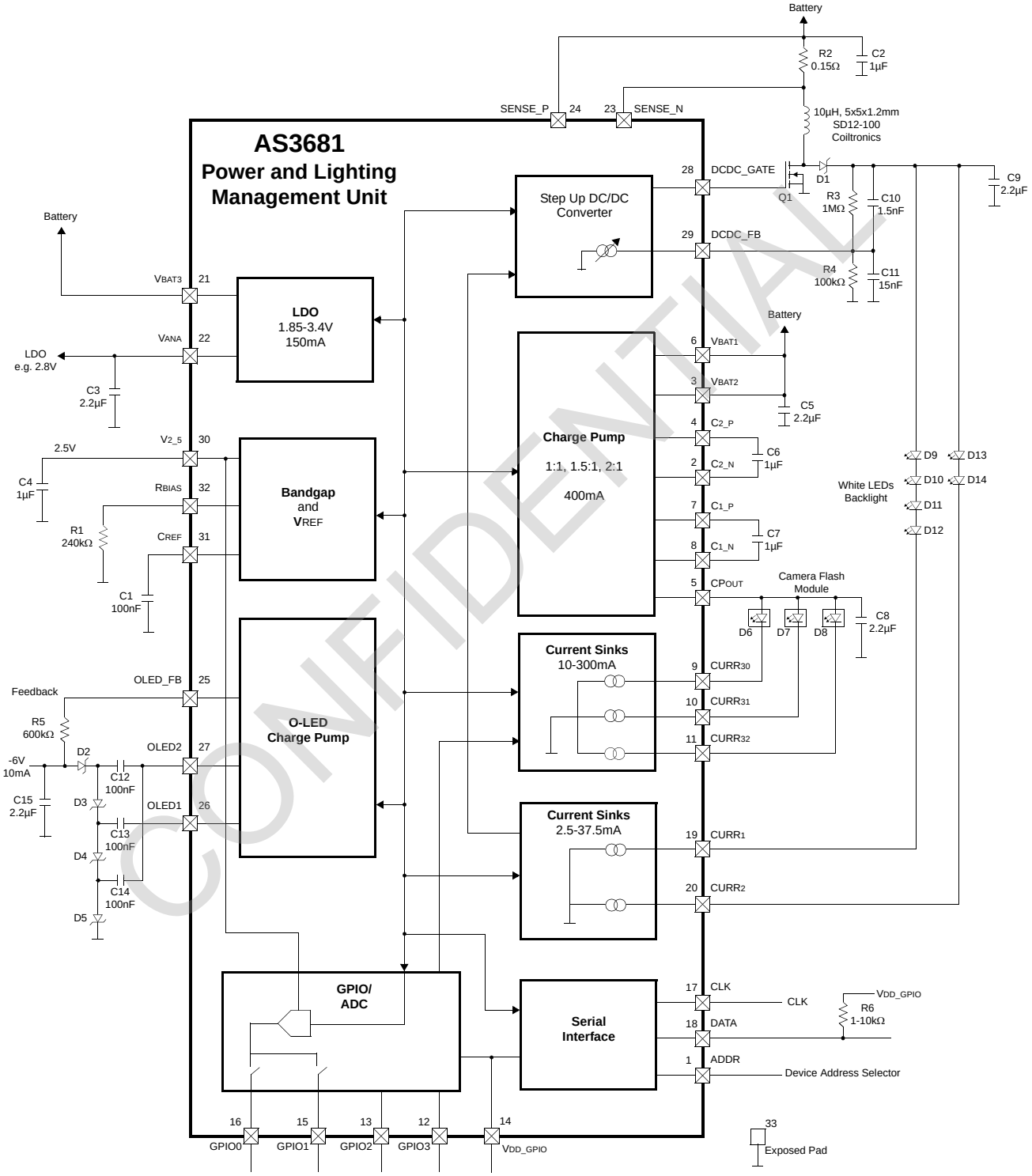
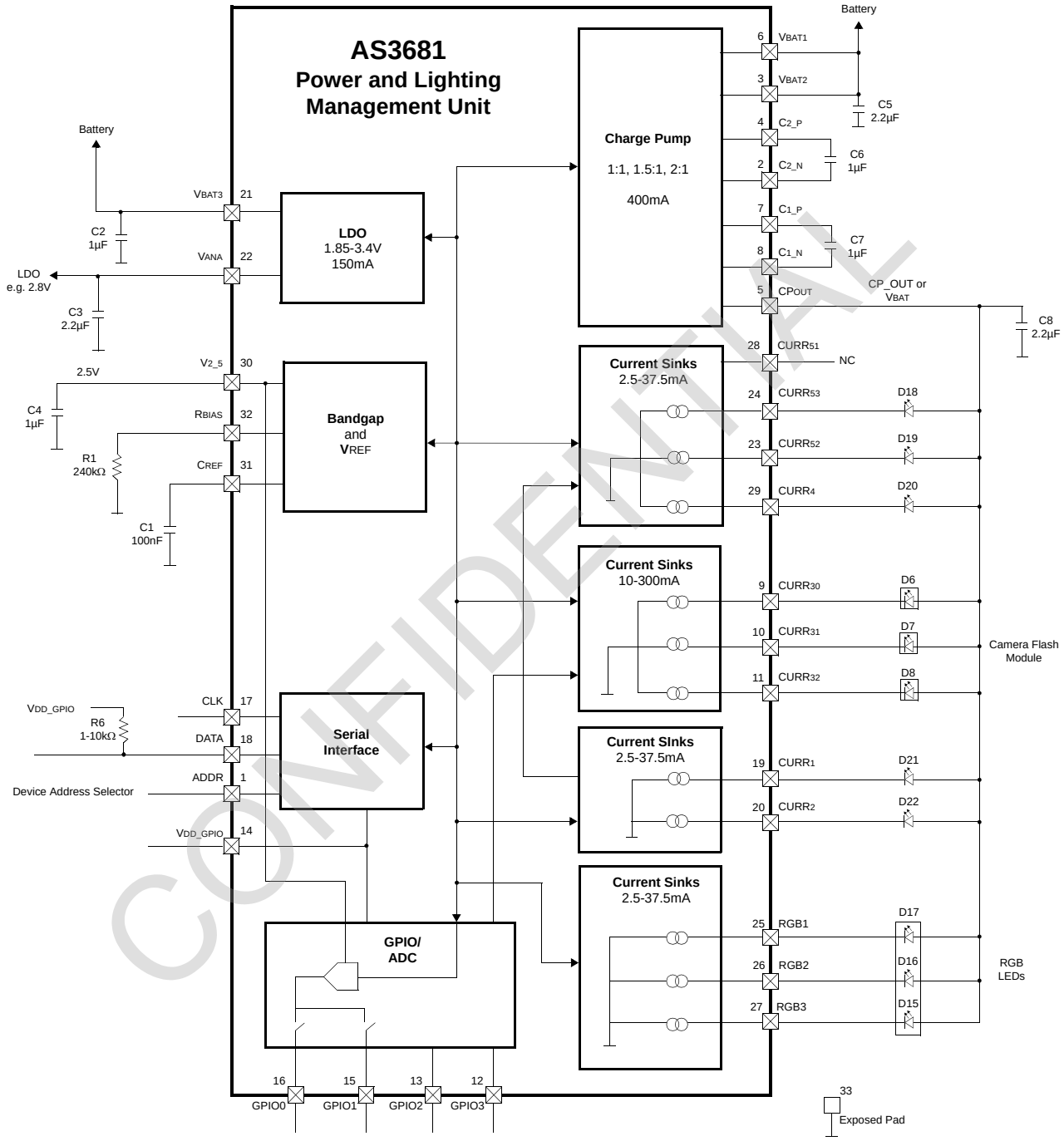


Figure 2. Parallel LED Configuration Option (by software): General Purpose Current Sinks (Pins 23, 24, 28, 29) and RGB LED Current Sinks (Pins 25, 26, 27)



Revision History

Revision	Date	Owner	Description
2.06	11 Aug 2005	ptr	-Updated soldering conditions to *IPC/JEDEC J-STD 020C.*
2.07	29 Jan 2006	ptr	-Updated Table 5, “Voltage Feedback Example Values,” on page 12. -Changed C10 rating to 25V (see Table 24 on page 47).

Contents

5 Absolute Maximum Ratings (Non-Operating)

Stresses beyond the absolute maximum ratings may cause permanent damage to the AS3681. These are stress ratings only. Functional operation of the device at these or beyond those in Section 5.1 is not implied.

Caution: Exposure to absolute maximum rating conditions may affect device reliability.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_HV}	15V Pins	-0.3	17	V	Applicable for high-voltage current sink pins $CURR_1$ and $CURR_2$.
V_{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for 5V pins V_{BAT1}:V_{BAT3}, V_{ANA}, and V_{2_5}; low-voltage current sink pins $CURR_{30}$:$CURR_{32}$; Charge Pump pins C_{1_N}, C_{2_N}, C_{1_P}, C_{2_P}, CP_OUT.
V_{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins GPIO0:GPIO3; serial interface pins CLK, DATA, ADDR; all other pins not listed above.
I_{IN}	Input Pin Current	-25	+25	mA	At 25ºC, Norm: JEDEC 17
T_{strg}	Storage Temperature Range	-55	125	ºC	
	Humidity	5	85	%	Non-condensing
V_{ESD}	Electrostatic Discharge	-1000	1000	V	Norm: MIL 883 E Method 3015
P_t	Total Power Dissipation		1	W	TA = 70 degrees
T_{BODY}	Peak Body Temperature		260	ºC	T = 20 to 40s, in accordance with *IPC/ JEDEC J-STD 020C.*

5.1 Operating Conditions

Table 2. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{HV}	High Voltage	0.0		15.0	V	Applicable for high-voltage current sink pins $CURR_1$ and $CURR_2$.
V_{BAT}	Battery Voltage	3.0	3.6	5.5	V	V_{BAT1}:V_{BAT3}
V_{GPIO}	Periphery Supply Voltage	1.5		3.3	V	For GPIO and serial interface pins.
V_{2_5}	Voltage on Pin V_{2_5}	2.4	2.5	2.6	V	Internally generated.
T_{AMB}	Ambient Temperature	-30	25	70	ºC	
I_{BAT}	Operating Current		85		µA	Normal operating current, no load.
$I_{LOWPOWER}$	Low-Power Mode Current		10		µA	Current consumption in low-power mode; **low_power_mode** (page 8) = 1, both LDOs on, maximum LDO load current = 5mA (1).
$I_{STANDBY}$	Standby Mode Current		6		µA	Current consumption in standby mode. Only 2.5V regulator on V_{DD_GPIO} > 0.3V.
$I_{SHUTDOWN}$	Shutdown Mode Current		1		µA	Current consumption in shutdown mode. V_{DD_GPIO} < 0.3V.

Notes:

1. Overall power consumption in Low-Power mode includes reset control, serial interface receive operation, reference generation for LDOs, and both LDOs on. V_{BAT} and V_{DD_GPIO} are above their reset levels (see Table 17 on page 40).

6 Detailed Functional Descriptions

6.1 Analog LDO

The Analog LDO (V_{ANA}) is designed to supply power to sensitive analog circuits like LNAs, Transceivers, VCOs, and other critical RF components of cellular radios. Additionally, the Analog LDO is suitable for supplying power to audio devices or as a reference for A/D and D/A converters.

The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors (see Figure 3) of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these capacitors ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress ripple on the battery caused by the PA in TDMA systems. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease in performance.

Figure 3. Analog LDO Block Diagram

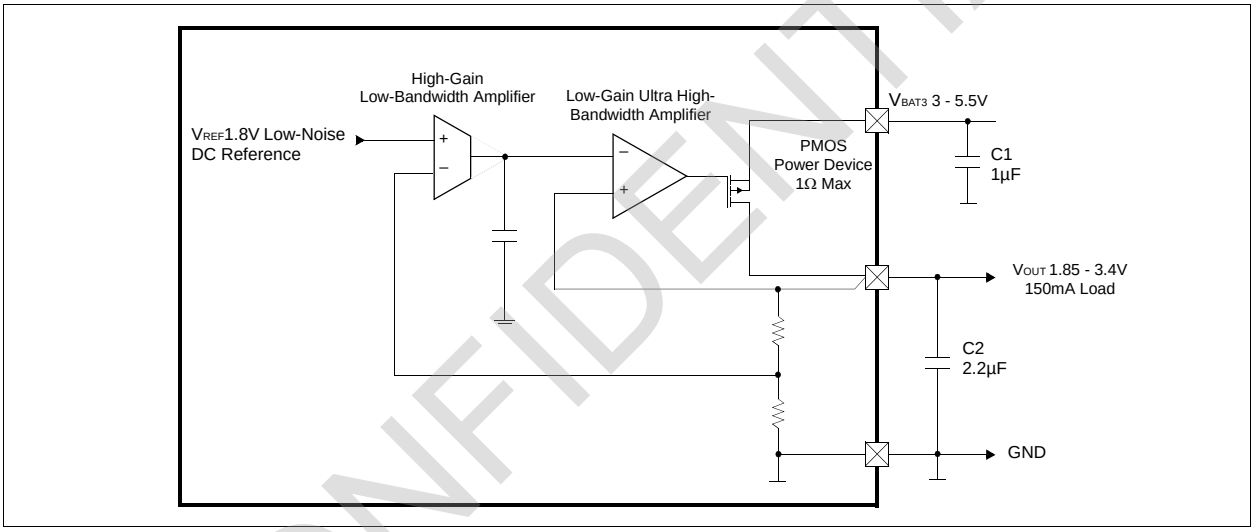


Table 3. Analog LDO Characteristics
V_{BAT}=4V; I_{load}=150mA; T_{AMB} =25ºC; C_{LOAD} = 2.2µF ceramic (unless otherwise specified).

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{BAT}	Supply Voltage Range	3		5.5	V	
R_{ON}	On Resistance			1	Ω	@150mA
P_{SRR}	Power Supply Rejection Ratio	70			dB	f = 1kHz
		55				f = 10kHz
		40				f = 100kHz
I_{On}	Supply Current		50		µA	Without load
			3			Without load, **low_power_mode** (page 8) = 1
			150			With 150mA load
I_{OFF}	Shutdown Current			100	nA	Without load
Noise	Output noise			50	µVrms	10Hz < f < 100kHz

Table 3. Analog LDO Characteristics (Continued)
V_{BAT}=4V; I_{load}=150mA; T_{AMB} =25ºC; C_{LOAD} = 2.2µF ceramic (unless otherwise specified).

Symbol	Parameter	Min	Typ	Max	Unit	Note
tstart	Startup Time			200	µs	
Vout_tol	Output Voltage Tolerance	-2		2	%	**low_power_mode** (page 8) = 0
Vout	Output Voltage	1.85		2.85	V	V_{BAT} > 3.0V
		1.85		3.4		Full Programmable Range
$V_{LineReg}$	Line Regulation **low_power_mode** = 0	-1		1	mV	Static (1)
		-10		10		Transient; Slope: t_r = 10µs
$V_{LoadReg\_HP}$	Load Regulation **low_power_mode** = 0	-1		1	mV	Static (2)
		-20		20		Transient; Slope: t_r = 10µs (3)
I_{LIMIT}	Current Limitation **low_power_mode** = 0		400		mA	LDO acts as current source if the output current exceeds I_{LIMIT}.
	Current Limitation **low_power_mode** = 1		5			
$V_{LoadReg\_LP}$	Load Regulation **low_power_mode** = 1	-10		10	mV	Static (4)
		-50m		50		Transient; Slope: t_r = 10µs (5)

Notes:

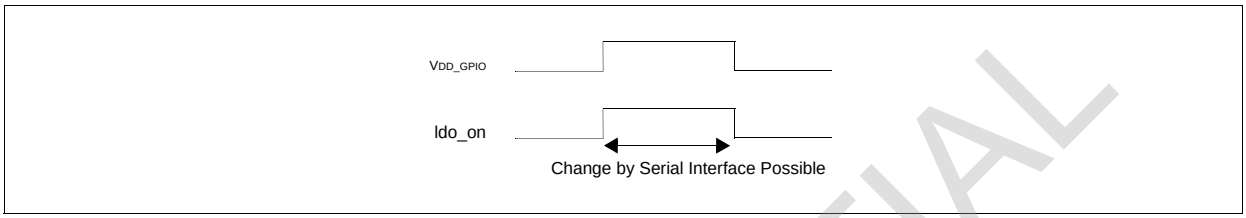
1. The Line Regulation in Table 3 is valid for whole output voltage (1.8 to 3.3V), if (V_{BAT}-V_{ANA}) >200mV.
2. The static Load Regulation in Table 3 is valid for whole output voltage (1.8 to 3.3V) and current range (0 to 100mA), if (V_{BAT}-V_{ANA}) >200mV.
3. The load condition for this value is a 1 to 100mA and 100 to 1mA steps.
4. The static load regulation in Table 3 is valid for the whole output voltage range (1.8 to 3.3V) and current range (0 to 5mA), if (V_{BAT}-V_{ANA}) >500mV.
5. The load condition for this value is a 0.05 to 5mA and 5 to 0.05mA steps.

6.1.1 LDO Registers

Addr: 00		**Reg. Control** This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and AS3681 low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_on	1	R/W	Switches on control of LDO (see Figure 4 on page 9).
1	cp_oled_on			(see cp_oled_on on page 33)
2	cp_led_on			(see cp_led_on on page 17)
3	curr1_on			(see curr1_on on page 20)
4	curr2_on			(see curr2_on on page 20)
5	curr3_on			(see curr3_on on page 21)
6	step_up_on			(see step_up_on on page 13)
7	low_power_mode	0	R/W	0 = Normal operation. 1 = Low-power mode; current consumption is reduced by about 75µA. Reduced performance of LDO: max 5mA load, internal oscillator is switched off. The device will exit low-power mode automatically, if blocks requiring the oscillator are enabled.

Addr: 06		Ldo_voltage_control		
		This register sets the output voltage (VANA) for the LDO.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:4	ldo_v	13h	R/W	Controls LDO voltage selection. 00000b = 1.85V. ... LSB = 50mV 11111b = 3.4V
5:7				N/A

Figure 4. ldo_on Control



6.2 Step Up DC/DC Converter

The Step Up DC/DC Converter is a high-efficiency current mode PWM regulator, providing output voltage up to 25V and a load current up to 50mA. A constant switching-frequency results in a low noise on the supply and output voltages.

Figure 5. Step Up DC/DC Converter Block Diagram; Option: Current Feedback

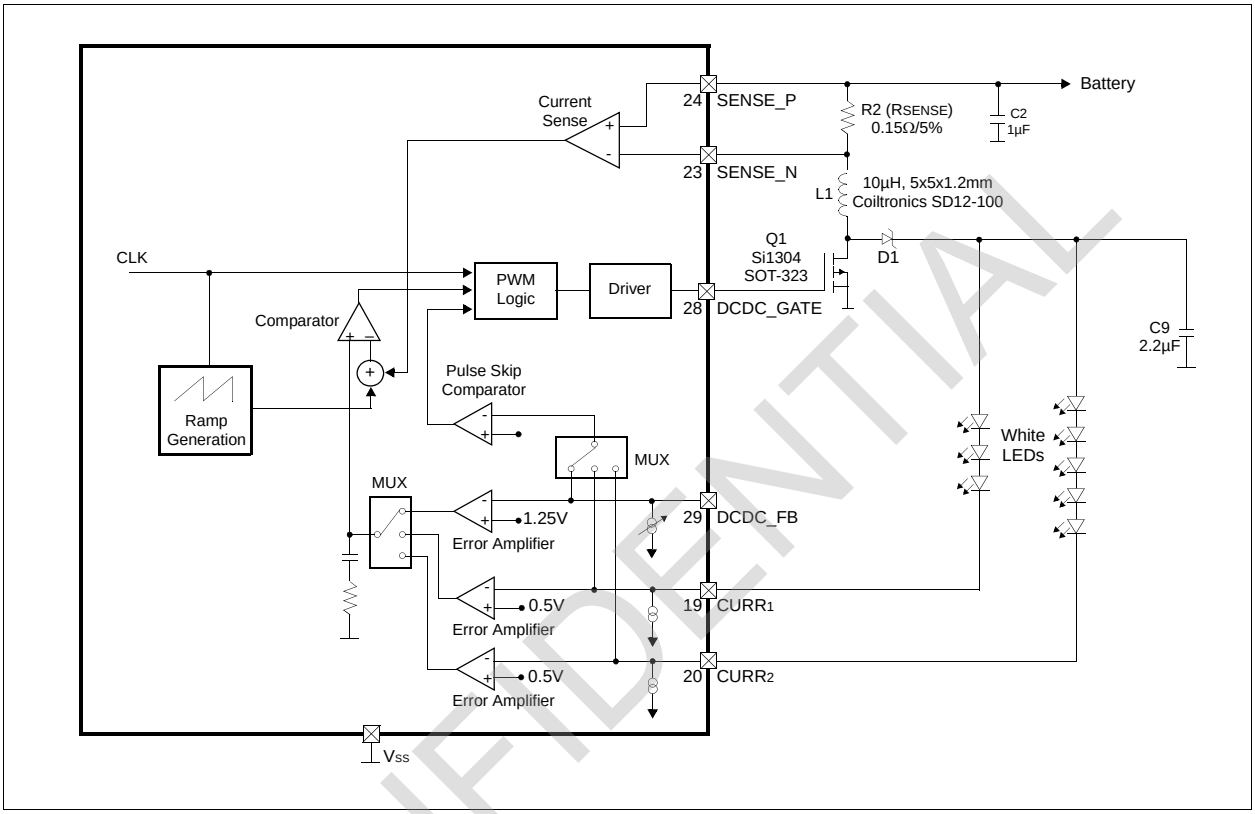


Table 4. Step Up DC/DC Converter Parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
IVDD	Quiescent Current		140		µA	Pulse skipping mode.
VFB1	Feedback Voltage for External Resistor Divider	1.20	1.25	1.30	V	For constant voltage control.
VFB2	Feedback Voltage for Current Sink Regulation		0.5		V	CURR1 or CURR2.
IDCDC_FB	Additional Tuning Current at Pin DCDC_FB	0		15	µA	Adjustable by software in 1µA steps using Register 12 (page 13).
	Accuracy of Feedback Current	-4		4	%	
Vrsense_max	Current Limit Voltage at RSENSE (R2)		100		mV	e.g., 0.65A for 0.15Ω sense resistor.
RSW	Switch Resistance			1	Ω	ON-resistance of external switching transistor.
Iload	Load Current	0		50	mA	At 15V output voltage.
fIN	Switching Frequency	0.9	1	1.1	MHz	Internally trimmed.
Cout	Output Capacitor		2.2		µF	Ceramic, ±20%.

Table 4. Step Up DC/DC Converter Parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
L	Inductor		10		µH	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency.
t_{MIN_ON}	Minimum on Time		130		ns	
MDC	Maximum Duty Cycle		91		%	Guaranteed per design.

6.2.1 Feedback Selection

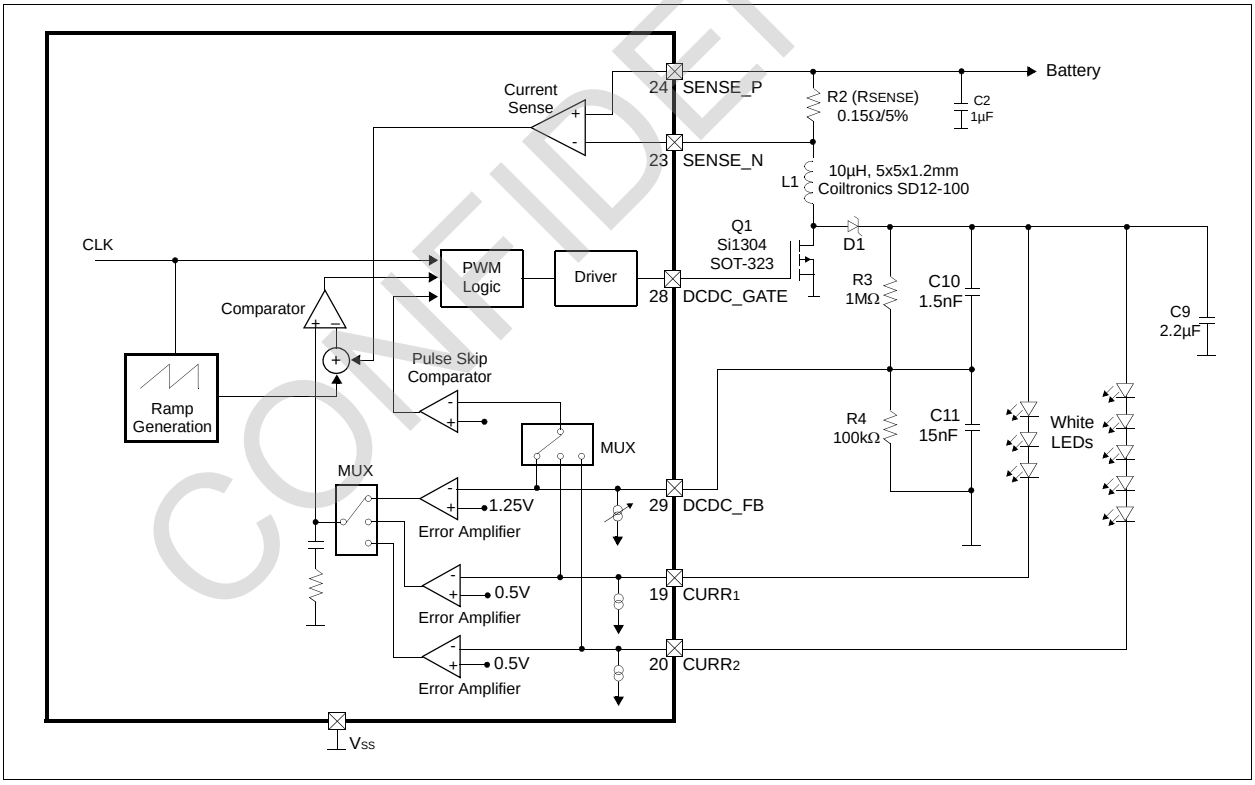
Register 12 (page 13) selects the type of feedback for the Step Up DC/DC Converter.

The feedback for the DC/DC converter can be selected either by current sinks $CURR_1$ or $CURR_2$ (see Figure 5 on page 10) or by a voltage feedback at pin DCDC_FB (see Figure 6). Bit **step_up_res** (page 13) should be set to 0 in both modes.

Setting **step_up_fb** (page 13) = 01 enables feedback at pin 19 ($CURR_1$); setting **step_up_fb** = 10 enables feedback at pin 20 ($CURR_2$). The Step Up DC/DC Converter is regulated such that the required current at the feedback path can be supported.

Note: Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other (unregulated) path.

Figure 6. Step Up DC/DC Converter Block Diagram; Option: Regulated Output Voltage, Feedback is at Pin DCDC_FB



6.2.2 Voltage Feedback

Setting bit **step_up_fb** (page 13) = 00 enables voltage feedback at pin 29 (DCDC_FB). Bit **step_up_res** (page 13) should be set to 1 in this configuration.

The output voltage is regulated to a constant value, given by:

$$U_{stepup\_out} = (R3+R4)/R4 \times 1.25 + I_{IDCDC\_FB} \times R3 \quad \textit{(EQ 1)}$$

If R4 is not used, the output voltage is:

$$U_{stepup\_out} = 1.25 + I_{IDCDC\_FB} \times R3 \quad \textit{(EQ 2)}$$

Where:

U_{stepup_out} = Step Up DC/DC Converter output voltage.

R3 = Feedback resistor R3.

R4 = Feedback resistor R4.

I_{IDCDC_FB} = Tuning current at pin 29 (DCDC_FB); 0 to 15µA in 1µA steps.

Table 5. Voltage Feedback Example Values

$I_{vtuning}$	U_{stepup_out}	U_{stepup_out}
µA	R3 = 1MΩ, R4 not used	R3 = 500kΩ, R4 = 50kΩ
0	-	13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	-	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25

Caution: The voltage on CURR1 and CURR2 must not exceed 15V.

6.2.3 PCB Layout Tips

To ensure good EMC performance of the DCDC converter, keep its external power components C2, R2, L1, Q1, D1 and C9 close together. Connect the ground of C2, Q1 and C9 locally together and connect this path with a single via to the main ground plane. This ensures that local high-frequency currents will not flow to the battery.

6.2.4 Step Up DC/DC Converter Registers

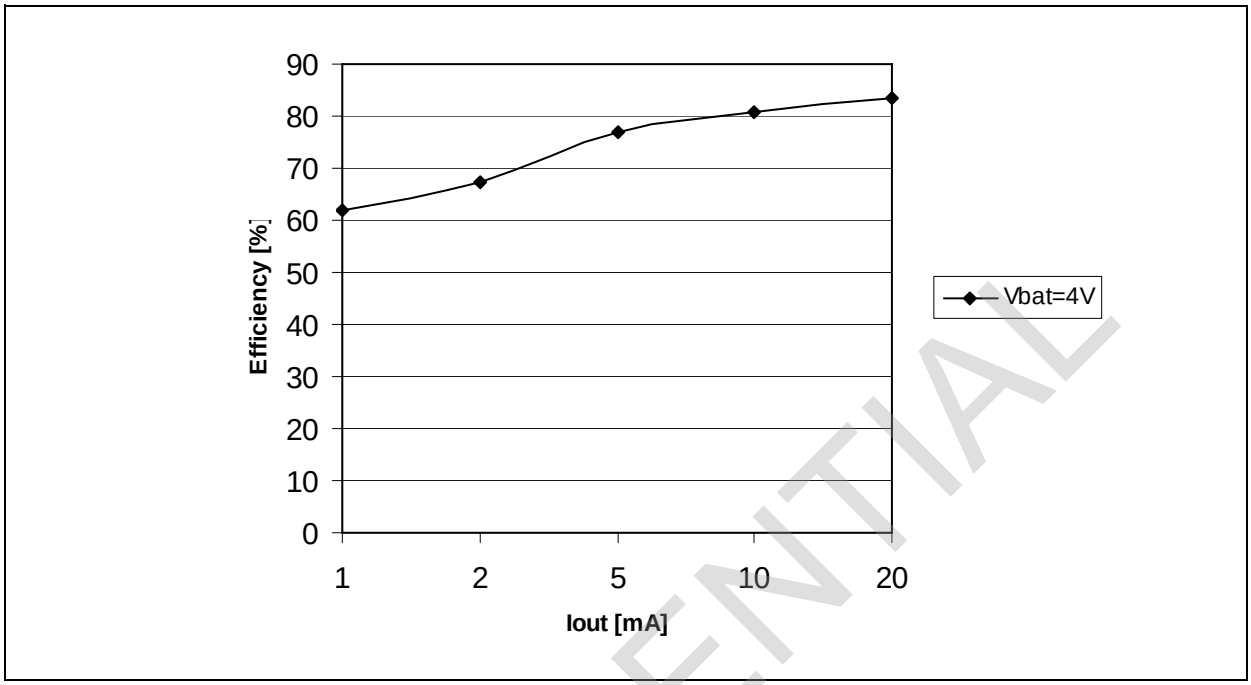
Addr: 00		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and AS3681 low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_on			(see ldo_on on page 8)
1	cp_oled_on			(see cp_oled_on on page 33)
2	cp_led_on			(see cp_led_on on page 17)
3	curr1_on			(see curr1_on on page 20)
5	curr2_on			(see curr2_on on page 20)
5	curr3_on			(see curr3_on on page 21)
6	step_up_on	0	R/W	0 = Disables the Step Up DC/DC Converter. 1 = Enables the Step Up DC/DC Converter.
7	low_power_mode			(see low_power_mode on page 8)

Addr: 12		DCDC Control		
		This register controls the Step Up DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_frequ	0	R/W	Defines the clock frequency of the Step Up DC/DC Converter. 0 = 1 MHz 1 = 500 kHz
1:2	step_up_fb	00	R/W	Controls the feedback source. 00 = DCDC_FB enabled (external resistor divider). 01 = $CURR_1$ feedback enabled (feedback via white LEDs. 10 = $CURR_2$ feedback enabled (feedback via white LEDs. 11 = Reserved.
3:6	step_up_vtuning	0000	R/W	Defines the tuning current at pin 29 (DCDC_FB). 0000 = 0 mA 0001 = 1 mA ... 1111 = 15 mA
7				N/A

Addr: 13		DCDC Test		
		This register controls the Step Up DC/DC Converter and low-voltage current sinks $CURR_{3x}$.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_res	0	R/W	Gain selection for Step Up DC/DC Converter. 0 = Select 0 if Step Up DC/DC Converter is used with current feedback ($CURR_1$, $CURR_2$) or if DCDC_FB is used with current feedback only – only R1, C1 connected (see Figure 6 on page 11). 1 = Select 1 if DCDC_FB is used with external resistor divider (2 resistors).
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active. 0 = Accurate output voltage, more ripple. 1 = Elevated output voltage, less ripple.
2	curr3_high			(see curr3_high on page 22)
3	curr3_mode			(see curr3_mode on page 22)
5:7				N/A

6.2.5 Efficiency of 15V Step Up DC/DC Converter

Figure 7. Efficiency of +15V Supply



6.3 Charge Pump

The Charge Pump uses two external flying capacitors (pins 2, 4, and pins 7, 8) to generate output voltages higher than the battery voltage.

There are three different modes:

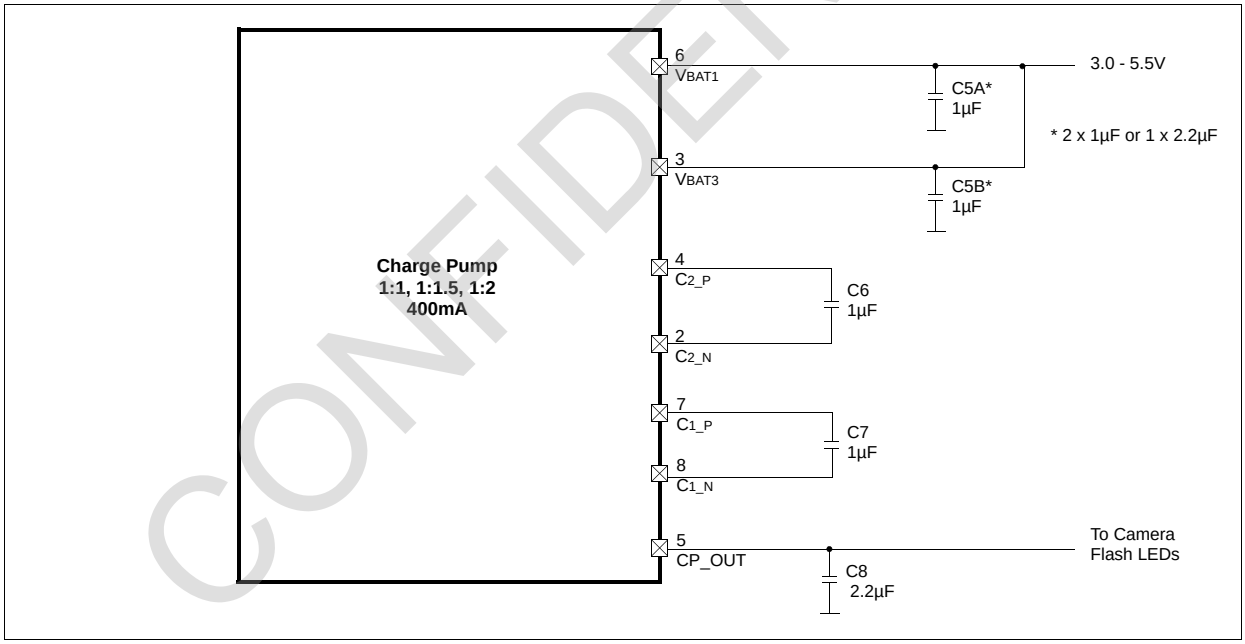
- 1:1 Bypass Mode – Battery input and output are connected by a low-impedance switch (0.5Ω); battery current = output current.
- 1:1.5 Mode – The output voltage is 1.5 times the battery voltage (without load); battery current = 1.5 times output current.
- 1:2 Mode – The output voltage is 2 times the battery voltage (without load); battery current = 2 times output current

Depending on the actual current in any of the active current sinks (see Efficiency of Charge Pump with Resistive Loads on page 18) the Charge Pump can be selected at a mode with the best overall efficiency.

Examples:

- Battery voltage = 3.7V, LED dropout voltage = 3.5V. The 1:1 mode will be selected and there is 100mV drop on the current sink and on the Charge Pump switch. Efficiency 95%.
- Battery voltage = 3.5V, LED dropout voltage = 3.5V. The 1:1.5 mode will be selected and there is 1.5V drop on the current sink and 250mV on the Charge Pump. Efficiency 66%.
- Battery voltage = 3.8V, LED dropout voltage = 4.5V (Camera Flash). The 1:2 mode will be selected and there is 600mV drop on the current sink and 2.5V on the Charge Pump. Efficiency 60%.

Figure 8. Charge Pump Pin Connections



The Charge Pump requires the external components listed in Table 6.

Table 6. Charge Pump External Components

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_{FLY1}, C_{FLY2}	External Flying Capacitor (2x)	0.8	1.0	1.2	µF	Ceramic low-ESR capacitor between pins $C1_P$ and $C1_N$, and between pins $C2_P$ and $C2_N$.
C_{STORE}, C_{Buffer}	External Storage Capacitor and Supply Buffer Capacitor	2.0	2.2	2.4	µF	Ceramic low-ESR capacitor between pins CP_OUT and V_{SS}, pins V_{BAT} and V_{BAT2} (in parallel) and V_{SS}.

Note: The connections of the two external capacitors should be kept as short as possible.

Table 7. Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{CPOUT_50ms}	Output Current 80ms	0.0		400	mA	With 1µF flying capacitors, 80ms pulse width, 10% duty cycle max.
I_{CPOUT}	Output Current Continuous	0.0		200	mA	With 1µF flying capacitors.
V_{CPOUT}	Output Voltage	5		5.5	V	Internally regulated.
η	Efficiency	60		90	%	Including current sink loss.
1:1 Mode	Power Consumption without Load		0.1		mA	f_{clk} = 1 MHz
1:1.5 Mode			4.5			
1:2 Mode			5			
f_{clk} Accuracy	Accuracy of Clock Frequency	-20		20	%	

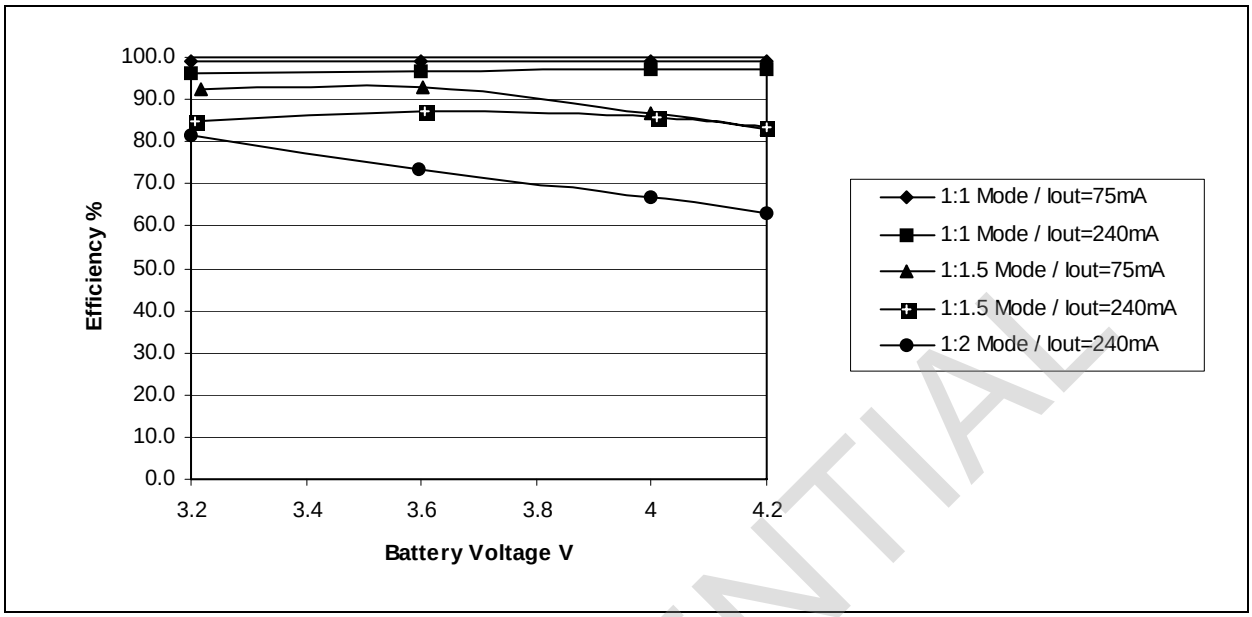
6.3.1 Charge Pump Registers

Addr: 00		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and AS3681 low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_on			(see ldo_on on page 8)
1	cp_oled_on	0	R/W	(see cp_oled_on on page 33)
2	cp_led_on	00	R/W	0 = Disable Charge Pump. 1 = Enable Charge Pump.
3	curr1_on			(see curr1_on on page 8)
5	curr2_on			(see curr2_on on page 8)
5	curr3_on			(see curr3_on on page 21)
6	step_up_on			(see step_up_on on page 13)
7	low_power_mode			(see low_power_mode on page 8)

Addr: 17		CP Control		
		This register controls the Charge Pump.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	cp_clk	0	R/W	Clock frequency selection. 0 = 1 MHz 1 = 500 kHz
1:2	cp_mode	0	R/W	Selection of Charge Pump mode. *X*0 = 1:1.5 mode *X*1 = 1:2 mode **Note:** Direct switching from 1:1.5 mode into 1:2 mode and vice versa is not allowed. Always switch over 1:1 mode.
3:7				N/A

6.3.2 Efficiency of Charge Pump with Resistive Loads

Figure 9. Efficiency of Charge Pump with Resistive Loads



6.4 Efficiency of Charge Pump with LED Loads

Figure 10 shows the Efficiency of the Charge Pump with white LEDs connected. The efficiency is dependent on the LED forward voltage given by:

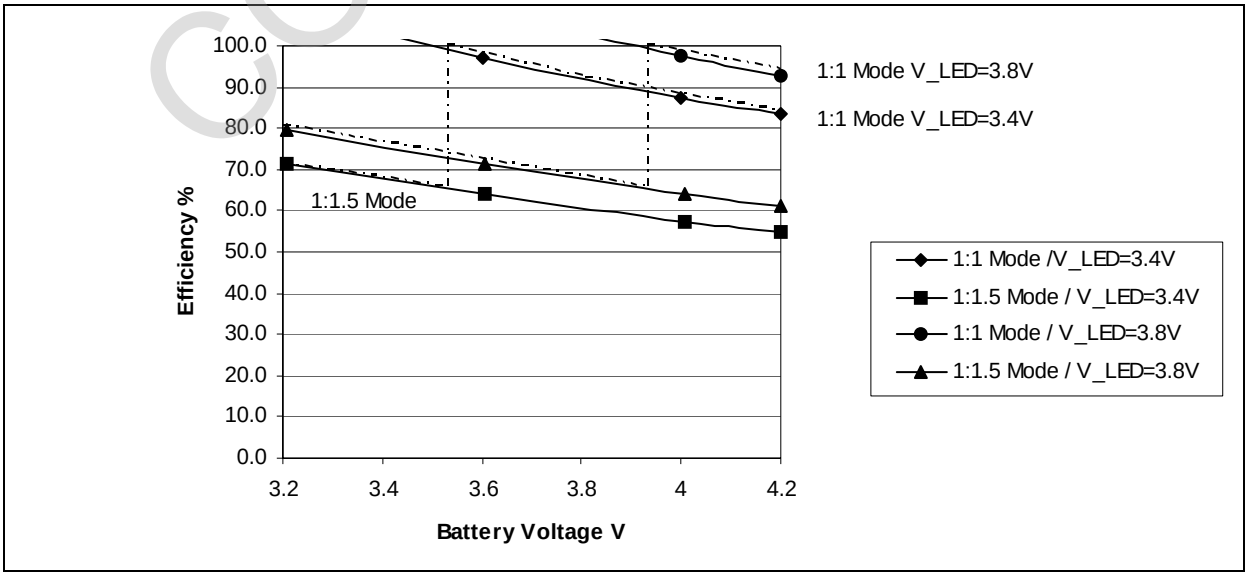
$$Eff=(V\_LED*I_{out})/(Uin*I_{in}) \quad (EQ\ 3)$$

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:1.5 mode, in order to provide enough supply for the current sinks.

Depending on which current sink is supplied by the Charge Pump, switching should take place, when a corresponding low voltage alert (bit currx_low_voltage, Register 23 (see pages 20, 23, and 28) is set. The respective bit is set to 1 when the voltage at the current sink (CURR1, CURR2, CURR30, CURR31, CURR32, CURR4, CURR51, CURR51, CURR52, or CURR53) drops below < 0.1 volts.

Note: 1:2 Mode should only be used for flash LEDs or if a high current Icp_out>200mA is required.

Figure 10. Efficiency of Charge Pump I_{out} = 240 mA



6.5 Current Sinks

The AS3681 contains general purpose current sinks intended to control backlights, buzzers, and vibrators. All current sinks have an integrated protection against overvoltage (see VPROTECT page 21) and can therefore also drive inductive loads.

CURR1 is also used as feedback for the Step Up DC/DC Converter (regulated to 0.8V in this configuration).

- Current sinks CURR1 and CURR2 are high-voltage (15V) current sinks, used e.g., for series of white LEDs
- Current sinks CURR3*x* (CURR30, CURR31, and CURR32) are parallel 5V, high-current current sinks, used e.g., for a photocamera flash LED.
- Current sinks CURR4 and CURR5*x* (CURR51, CURR52, and CURR53) are general purpose current sinks optionally used in place of the Step Up DC/DC Converter, e.g. for white LEDs.
- Current sinks RGB1, RGB2, and RGB3 are general purpose current sinks optionally in place of the External Charge Pump, used e.g., for an RGB LED.

Table 8. Current Sink Function Overview

Current Sink	Pin	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current Control	Hardware On/Off Control	Alternate Function
				(Bits)	(mA)			
CURR1	19	15	37.5	4	2.5	Separate	PWM at GPIO3	N/A
CURR2	20						N/A	
CURR30	9	VBAT (5.5V)	150 or 300	4	10/20	Combined	Flash LED Strobe & Preview at GPIO2	
CURR31	10							
CURR32	11					Combined or Separate		
RGB1	25	VBAT (5.5V)	37.5	4	2.5	Separate	N/A	External Charge Pump
RGB2	27							
RGB3	26							
CURR4	29	VBAT (5.5V)	37.5	4	2.5	Separate	N/A	Step Up DC/DC Converter (feedback at CURR1 or CURR2)
CURR51 N/A	28					Combined		
CURR52	23							
CURR53	24							

6.5.1 High-Voltage Current Sinks CURR1 and CURR2 (37.5mA)

High-voltage current sinks CURR1 and CURR2 can be controlled individually using Register 02 (page 20). They may be supplied by the Step Up DC/DC Converter with voltages up to15V.

PWM Control

Bit **curr1_pwm** (page 20) = 1 Current Sink CURR1 can also be controlled by an external PWM signal at pin GPIO3 (e.g., for buzzers, vibrators). To enable PWM control, bit **curr1_pwm** (page 20) must be set to =1.

Table 9. High-Voltage Current Sink Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
ICurr1, ICurr2	CURR1 and CURR2 Current, 0h-Fh	0		37.5	mA	For V(CURRx) > 0.45V resolution = 2.5mA.
Δm	Matching Accuracy	-10%		+10%		All current sinks.
Δ	Absolute Accuracy	-20%		+20%		All current sinks.
VCurr1, VCurr2	Voltage Compliance	0.45		15	V	During normal operation.

6.5.2 High-Voltage Current Sink Registers

Addr: 00		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and AS3681 low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_on			(see ldo_on on page 8)
1	cp_oled_on			(see cp_oled_on on page 33)
2	cp_led_on			(see cp_led_on on page 17)
3	curr1_on	0	R/W	Switches on/off CURR1 current sink.
5	curr2_on	0	R/W	Switches on/off CURR2 current sink.
5	curr3_on			(see curr3_on on page 21)
6	step_up_on			(see step_up_on on page 13)
7	low_power_mode			(see low_power_mode on page 8)

Addr: 02		Curr12_value		
		This register sets the current for high-voltage current sinks CURR1 and CURR2.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	curr1_current	0	R/W	Defines current into CURR1. 0h = Power down ...(LSB = 2.5mA) Fh = 37.5mA
4:7	curr2_current	0	R/W	Defines current into CURR2. 0h = Power down ...(LSB = 2.5mA) Fh = 37.5mA

Addr: 04		Current Sink1-2 Control		
		This register controls currents sinks CURR1, CURR2, RGBx, CURR52, and CURR53.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_pwm	0	R/W	Defines function of current sinks. 0 = Normal operation. 1 = PWM operation with external clock pulses on GPIO3; overrides the setting of bits **gpio3_mode** (page 36).
1				N/A. Must be set to 0.
2:4	curr_test			(see curr_test on page 25)
5	rgb_on			(see rgb_on on page 25)
6	curr52_on			(see curr52_on on page 28)
7	curr53_on			(see curr53_on on page 28)

Addr: 23		Curr_low_voltage_control		
		This register indicates low voltage on the current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_low_voltage	1	R	Bit is set to 1 if CURR1 output voltage is low (< VCurr1_min).
1	curr2_low_voltage	1	R	Bit is set to 1 if CURR2 output voltage is low (< VCurr2_min).
2	curr3_low_voltage			(see curr3_low_voltage on page 23)
3	curr4_low_voltage			(see curr4_low_voltage on page 28)
4	curr51_low_voltage			(see curr51_low_voltage on page 28)
5	curr52_low_voltage			(see curr52_low_voltage on page 28)
6	curr53_low_voltage			(see curr53_low_voltage on page 28)
7				N/A

6.5.3 Low-Voltage Current Sink CURR3x (3x300mA)

Low-voltage current sinks CURR3x (CURR30, CURR31, and CURR32) are individual high-current current sinks controlled by programmable Register 03 (page 21). Each current sink can sink up to 150mA. They may be connected in parallel to increase the driving capability, e.g. for a photocamera flash LED.

The flash LED may be supplied by the 5V Charge Pump to guarantee a stable high current even at low battery voltage. The driving capability can be further enhanced by setting bit **curr3_high** (page 22), which doubles the current set in Register 03.

Additionally, CURR32 may be controlled individually, using register 16 (page 22) when bit **curr3_mode** (page 22) = 1.

Table 10. Low Voltage Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{CURR3}	CURR30:CURR32 Current, 0h-Fh	0		150	mA	For V(CURRx) > 0.2V resolution = 10mA, each current sink.
				300		When **curr3_high** (page 22) = 1.
Δ	Absolute Accuracy	-20%		+20%		All current sinks.
$V_{PROTECT}$	Voltage above V_{BAT} for Driver Protection			V_{BAT} + 2.0	V	$I_{CURR3} \geq$ 20mA.
V_{Curr3}	Voltage Compliance	0.2		V_{BAT}+ 0.5	V	During normal operation (**curr3_high** = 0).
		0.4		V_{BAT} + 0.5	V	During normal operation (**curr3_high** = 1).

6.5.4 Low Voltage Current Sink Registers

Addr: 00		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and AS3681 low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_on			(see ldo_on on page 8)
1	cp_oled_on			(see cp_oled_on on page 33)
2	cp_led_on			(see cp_led_on on page 17)
3	curr1_on			(see curr1_on on page 20)
5	curr2_on			(see curr2_on on page 20)
5	curr3_on	0	R/W	Switches on/off current sink CURR3.
6	step_up_on			(see step_up_on on page 13)
7	low_power_mode			(see low_power_mode on page 8)

Addr: 03		Curr3_value		
		This register controls the current for low-voltage current sinks CURR30, CURR31, and CURR32.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	curr3_current_strobe	0	R/W	Defines current into pin CURR3 during Strobe Mode, when **curr3_on** (page 21) = 1 and GPIO2 = 1 (overrides **gpio2_mode** (page 36)). 0h = Power down. ...(LSB = 10mA) Fh = 150mA
4:7	curr3_current_preview	0	R/W	Defines current into pin CURR3 during Preview Mode, when **curr3_on** (page 21) = 1 and GPIO2 = 0. 0h = Power down. ...(LSB = 10mA) Fh = 150mA

Addr: 05		Current Sink3 Control		
		This register sets the flash LED strobe duration.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	strobe_control	0	R/W	Defines GPIO2 for Strobe Mode operation 0*XXX* = Camera Flash is synchronized with a rising edge of the “Strobe” input signal at GPIO2. Flash time depends on the GPIO2 pulse width, but is limited to max.160ms. 1000 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 20ms. 1001 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 40ms. 1010 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 60ms. 1011 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 80ms. 1100 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 100ms. 1101 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 120ms. 1110 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 140ms. 1111 = Camera Flash is synchronized with a rising edge of “Strobe” input signal 160ms.
4:7				N/A

Addr: 13		DCDC Test		
		This register controls the Step Up DC/DC Converter and low-voltage current sinks $CURR_{3x}$.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_res			(see step_up_res on page 13)
1	skip_fast			(see skip_fast on page 13)
2	curr3_high	0	R/W	0 = $CURR_3$ = Normal operation. 1 = Doubles the programmed sink current of $CURR_3$ as set in Register 03 (page 21).
3	curr3_mode	0	R/W	0 = Register 03 (page 21) controls $CURR_{30}$, $CURR_{31}$, and $CURR_{32}$. 1 = Register 03 controls $CURR_{30}$ and $CURR_{31}$; Register 16 (page 22) controls $CURR_{32}$.
4:7				N/A

Addr: 16		rgb3_current		
		This register controls current sink RGB_3. It controls current sink $CURR_{32}$ when bit **curr3_mode** (page 22) = 1.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	rgb3_current	0	R/W	Controls current into current sink RGB_3. If bit **curr3_mode** = 1, this register also controls current sink $CURR_{32}$. 0_h = Power down. ... LSB = 2.5mA F_h = 37.5mA.
4:7				N/A

Addr: 23		Curr_low_voltage_control		
		This register indicates low voltage on the current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_low_voltage			(see curr1_low_voltage on page 20)
1	curr2_low_voltage			(see curr2_low_voltage on page 20)
2	curr3_low_voltage	1	R	Set to 1 if CURR3*x* output voltage is low (< V_{Curr3_min}).
3	curr4_low_voltage			(see curr4_low_voltage on page 28)
4	curr51_low_voltage			(see curr51_low_voltage on page 28)
5	curr52_low_voltage			(see curr52_low_voltage on page 28)
6	curr53_low_voltage			(see curr53_low_voltage on page 28)
7				N/A

6.5.5 Preview and Strobe Operations

Settings in Register 03 (page 21) for Preview Mode and Strobe Mode operations are defined as:

- curr3_current_preview – Defines the brightness of the white LEDs when a camera is in Preview Mode. The programmable current range is 0 to 300mA with a step size is 20mA.

  Preview Mode may be selected when there is not enough ambient light to see the object in front of the camera e.g. during focusing. This mode is enabled as long as **curr3_on** (page 21) is high. The typical current should be less than 100mA.

- curr3_current strobe – Defines the maximum brightness (during flash operation) of the camera flash LED. The current range is 0 to 150mA (300mA) per current sink. This current is triggered by GPIO2 = 1 and is active for a predetermined duration between 20 and 160ms, programmable using Register 05 (page 22).

  Current sinks CURR30, CURR31, and CURR32 are programmable in 16 steps from 0 to 150mA (0 to 300mA when **curr3_high** =1) with a step size of 10mA (20mA) for each current sink.

  With **curr3_mode** (page 22) = 0, Register 03 sets the current for all 3 current sinks. With **curr3_mode** = 1, Register 03 sets the current for CURR30 and CURR31, while the current for CURR32 is set separately using Register 16 (page 22).

  The maximum current into all 3 current sinks combined (CURR30, CURR31, and CURR32) can be as high as 3x300mA, however with the configuration shown in Figure 11, it is limited by the driving capability of the current sink (400mA).

Figure 11. Camera Flash Driver Pin Connections

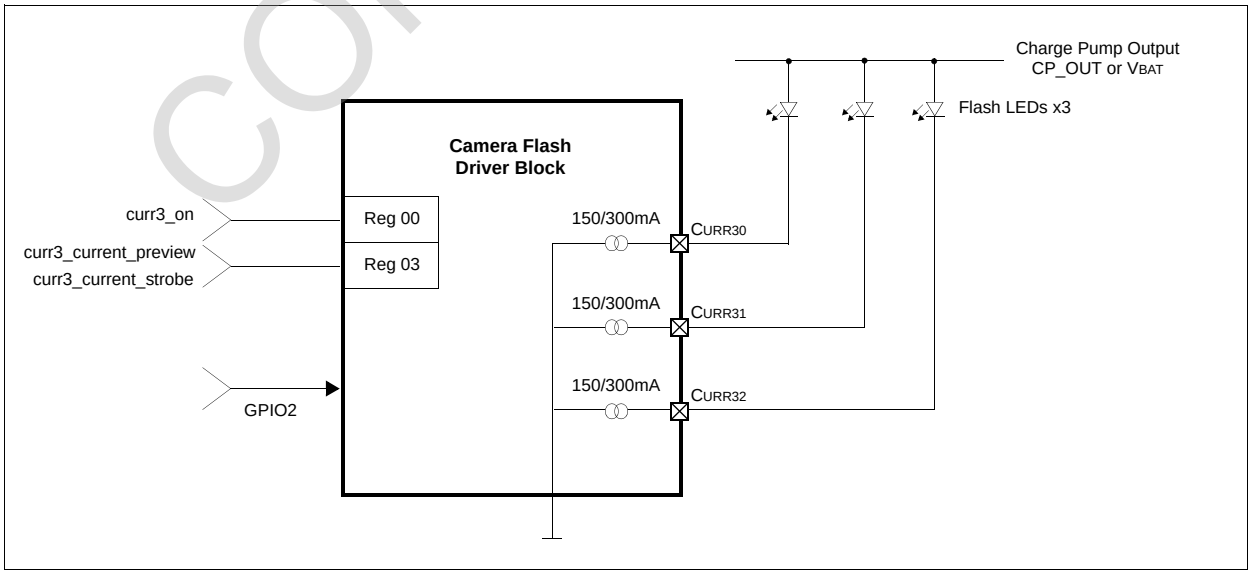
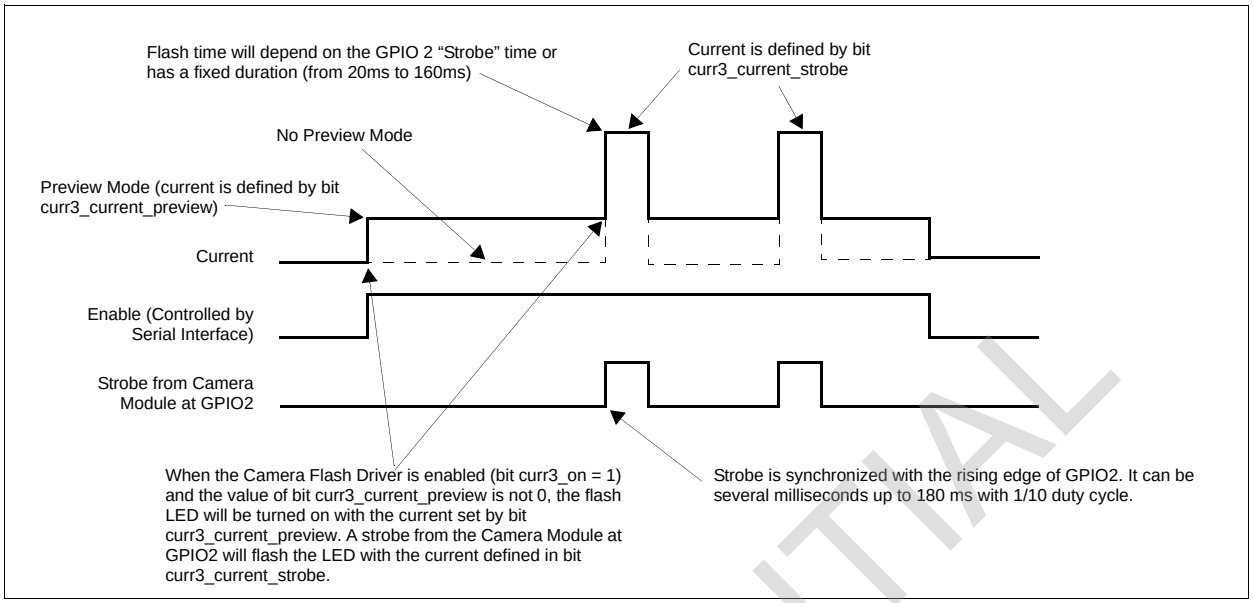


Figure 12. Preview Mode and Strobe Mode Timing Diagram



6.5.6 RGB Current Sinks (37.5mA)

Current sinks RGB*x* (RGB1, RGB2, and RGB3) are intended to control, for example, an RGB LED. They use the same pins as the External Charge Pump (pins 25:27) and can only be accessed if the External Charge Pump is not needed.

To enable current sinks RGBx, the External Charge Pump must be disabled (**cp_oled_on** (page 33) = 0) and the RGB current sinks must be enabled (**rgb_on** (page 28) = 1).

Figure 13. RGB Current Sink Pin Connections

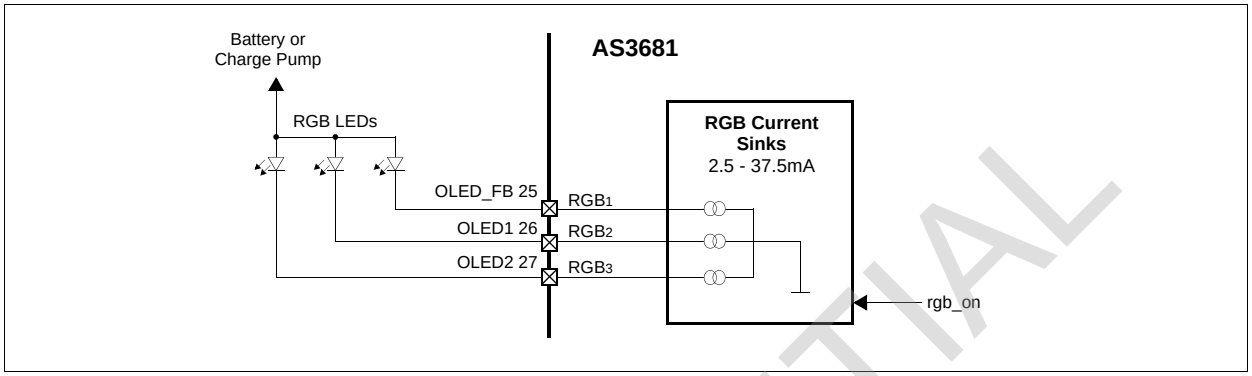


Table 11. RGB Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
IRGBx	RGBx Current, 0h-Fh	0		37.5	mA	For V(RGBx) > 0.2V resolution = 2.5mA each current sink.
Δm	Matching Accuracy	-10%		+10%		All current sinks.
Δ	Absolute Accuracy	-20%		+20%		All current sinks.
RGB1:3	Voltage Compliance	0.2		VBAT	V	During normal operation.

6.5.7 RGB Current Sink Registers

Addr: 04		Current Sink1-2 Control		
		This register controls currents sinks CURR1, CURR2, RGB*x*, CURR52, and CURR53.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_pwm			(see curr1_pwm on page 20)
1				N/A. Must be set to 0.
2:4	curr_test			For factory testing only; set to 00b.
5	rgb_on	0	R/W	Switches on/off all 3 RGB current sinks. Bit **cp_oled_on** (page 33) must be 0, if this bit = 1.
6	curr52_on			(see curr52_on on page 28)
7	curr53_on			(see curr53_on on page 28)

Addr: 15		rgb12_current		
		This register controls RGB current sinks RGB1 and RGB2.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	rgb1_current	00h	R/W	Defines current into RGB1. 0h = Power down. ...(LSB = 2.5mA) Fh = 37.5mA.
4:7	rgb2_current	00h	R/W	Defines current into RGB2. 0h = Power down. ...(LSB = 2.5mA) Fh = 37.5mA.

Addr: 16		rgb3_current		
		This register controls current sink RGB3. It controls current sink CURR32 when bit **curr3_mode** (page 22) = 1.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	rgb3_current	00h	R/W	Controls current into current sink RGB3 when bit **curr3_mode** = 0. 0h = Power down. ...(LSB = 2.5mA) Fh = 37.5mA.
4:7				N/A

6.5.8 General Purpose Current Sinks (37.5mA)

Current sinks CURR4 and CURR5x (CURR51, CURR52, and CURR53) are general purpose current sinks intended to control LEDs. They use the same pins as the external Step Up DC/DC Converter, and can only be accessed if the Step Up DC/DC Converter is not needed. To enable these current sinks, the Step Up DC/DC Converter must be disabled (**step_up_on** (page 13) = 0) and the general purpose current sinks must be enabled (**curr4_on** (page 27), = 1), **curr52_on** (page 28), and **curr53_on** (page 28)).

Although current sinks CURR5*x* are accessible on separate pins, they are all controlled by Register 14 (page 28).

Note: As CURR51 shares the same pin as the Step Up DC/DC Converter gate driver (pin 28, DCDC_GATE), some current is dissipated internally. Therefore it is not recommended to use CURR51 with the standard version of the AS3681.

Figure 14. General Purpose Current Sink Pin Connections

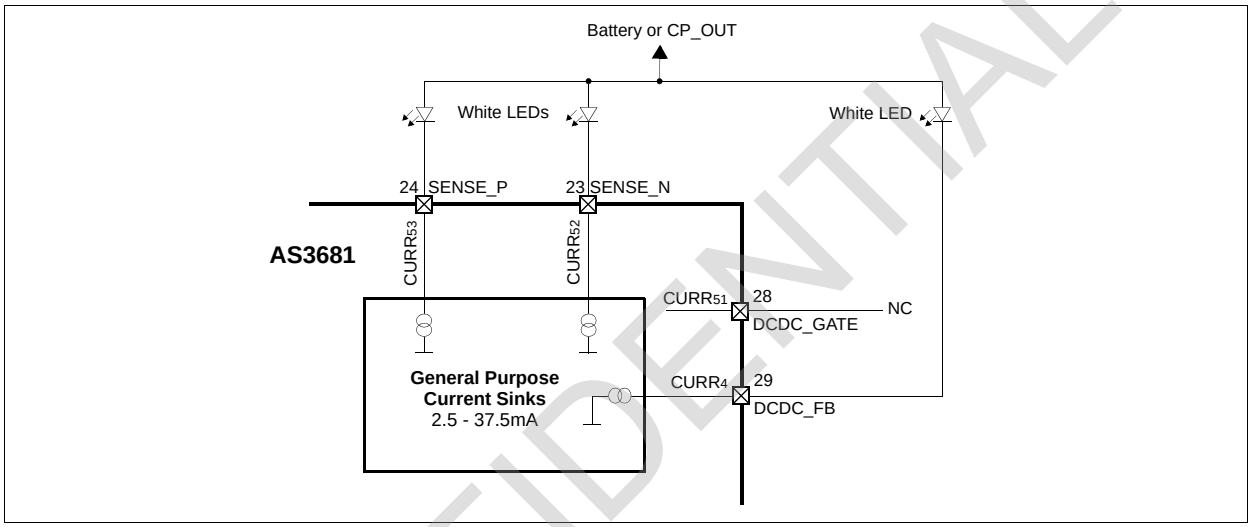


Table 12. General Purpose Current Sink Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
ICurr4, ICurr51, ICurr52, ICurr53	CURR4, CURR5x Current, 0h-Fh	0		37.5	mA	For V(CURR*x*) > 0.2V resolution = 2.5mA each current sink.
Δm	Matching Accuracy	-10%		+10%		All current sinks.
Δ	Absolute Accuracy	-20%		+20%		All current sinks.
VCurr4, VCurr51, VCurr52, VCurr53	Voltage Compliance	0.2		VBAT	V	During normal operation.

6.5.9 General Purpose Current Sink Registers

Addr: 01		GPIO Output Signal		
		This register controls GPIO outputs and enables current sinks CURR4 and CURR51.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_out			(see gpio0_out on page 35)
1	gpio1_out			(see gpio1_out on page 35)
2	gpio2_out			(see gpio2_out on page 35)
3	gpio3_out			(see gpio3_out on page 35)
4:5				N/A
6	curr4_on	0	R/W	Switches on/off current sink CURR4.
7	curr51_on	0	R/W	N/A. Must be set to 0.

Addr: 04		Current Sink1-2 Control		
		This register controls currents sinks CURR1, CURR2, RGBx, CURR52, and CURR53.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_pwm			(see curr1_pwm on page 20)
1				N/A. Must be set to 0.
2:4	curr_test			(see curr_test on page 25)
5	rgb_on			(see rgb_on on page 25)
6	curr52_on	0	R/W	Switches on/off current sink CURR52.
7	curr53_on	0	R/W	Switches on/off current sink CURR53.

Addr: 14		Curr45_current		
		This register controls general purpose current sinks CURR4, CURR52, and CURR53.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	curr4_current	0	R/W	Defines current into CURR4 (pin 29, DCDC_FB). Write protection: First write 9Bh into Register 31 (page 28) and then write to this register. 0h = Power down. ...(LSB = 2.5mA) Fh = 37.5mA.
4:7	curr5_current	0	R/W	Defines current into CURR52 (pin 23, SENSE_N). Defines current into CURR53 (pin 24, SENSE_P). Write protection: First write 9Bh into Register 31 (page 28) and then write to this register. 0h = Power down. ...(LSB = 2.5mA) Fh = 37.5mA.

Addr: 23		Curr_low_voltage_control		
		This register indicates low voltage on the current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_low_voltage			(see curr1_low_voltage on page 20)
1	curr2_low_voltage			(see curr2_low_voltage on page 20)
2	curr3_low_voltage			(see curr3_low_voltage on page 23)
3	curr4_low_voltage	1	R	Set to 1 if CURR4 output voltage is low (< VCurr4_min).
4	curr51_low_voltage	1	R	Set to 1 if CURR51 output voltage is low (< VCurr51_min).
5	curr52_low_voltage	1	R	Set to 1 if CURR52 output voltage is low (< VCurr52_min).
6	curr53_low_voltage	1	R	Set to 1 if CURR53 output voltage is low (< VCurr53_min).
7				N/A

Addr: 31		write_prot		
		This register controls write protection to prevent accidentally enabling CURR4 or CURR5x.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:7	write_prot	N/A	W	**curr4_current** (page 28) and **curr5_current** (page 28) can only be set by first writing 9Bh into this register.

6.6 External Charge Pump

This External Charge Pump uses external capacitors and Schottky diodes to generate low-current outputs in the range of -15 to +15V. The device delivers a square wave signal at pin 26 (OLED1) and an inverted square wave signal at pin 27 (OLED2) of 250kHz or 500kHz with full battery voltage swing. Depending on the external configuration, the battery voltage is multiplied and/or inverted. A feedback loop with a dedicated regulation pin controls the output voltage by modulating the duty circle.

Note: The recommended diode type for the External Charge Pump is the BAS40 (2 Schottky diodes in a single SOT666 package).

Table 13. External Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{fb00}	Negative Output Mode Feedback Voltage	-20	0	20	mV	Regulated, with internal current source, pin 25 (OLED_FB).
I_{fb}	Feedback Current	9.7	10	10.3	µA	Current sourced at feedback pin for negative mode.
V_{fb01}	Positive Output Mode Feedback Voltage	1.22	1.25	1.28	V	Regulated, with two external resistors.
V_{out00}	Output Voltage Mode 00b		-6		V	With external 600kΩ resistor.
V_{out01}	Output Voltage Mode 01b		15		V	With external 125kΩ resistor and 1.375 MΩ resistor.
η	Efficiency			85	%	Battery voltage = 3.5V
		70				Battery voltage = 4.2V
I_{out}	Output Current	10			mA	@ -6V
		5				@ +15V

Figure 15. Negative Regulation with 2 Flying Capacitors

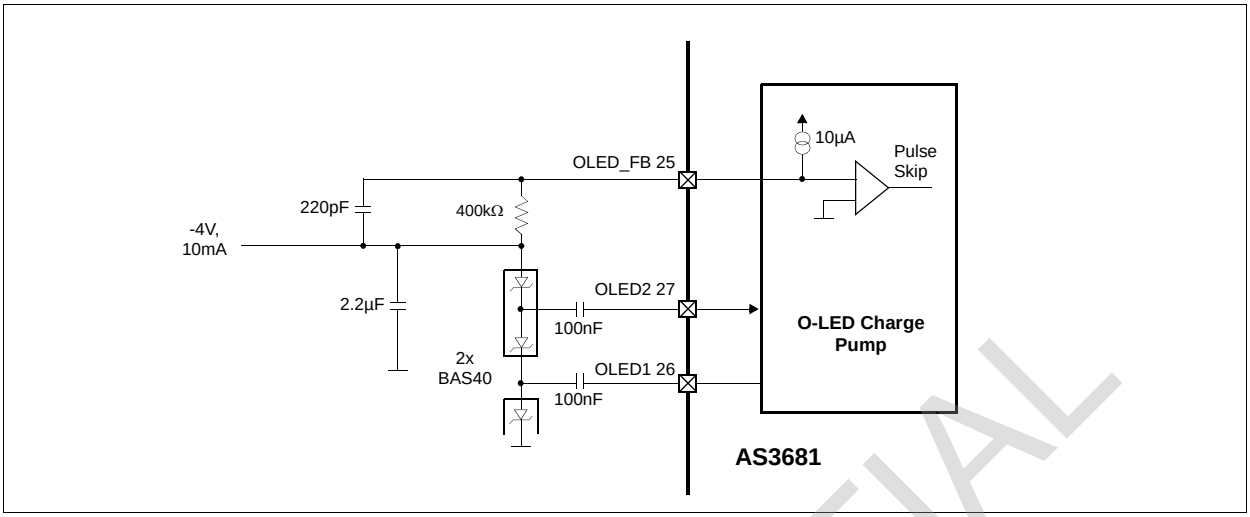


Figure 16. Minimum Output Voltage of Negative Charge Pump with 2 Flying Capacitors in Free-Running Mode (Unregulated, **cp_oled_mode** *(page 33) = 10b,* **low_power_mode** *(page 8) = 0)*

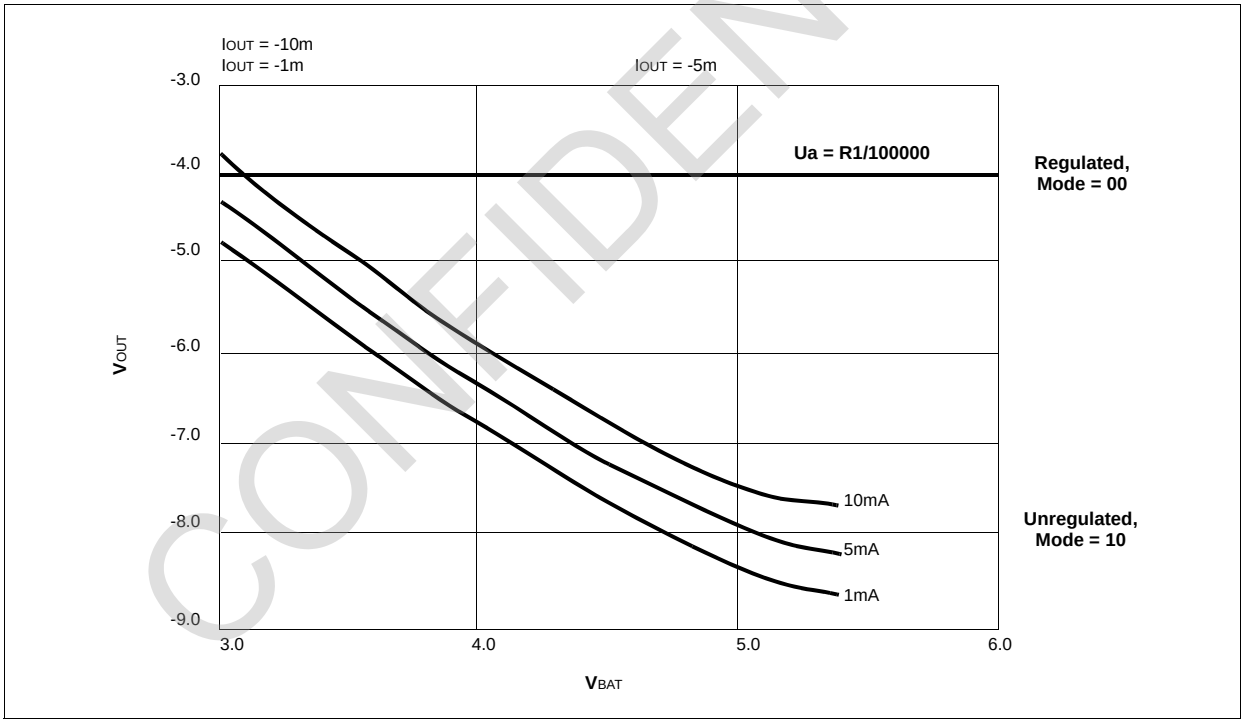


Figure 17. Negative Regulation with 3 Flying Capacitors

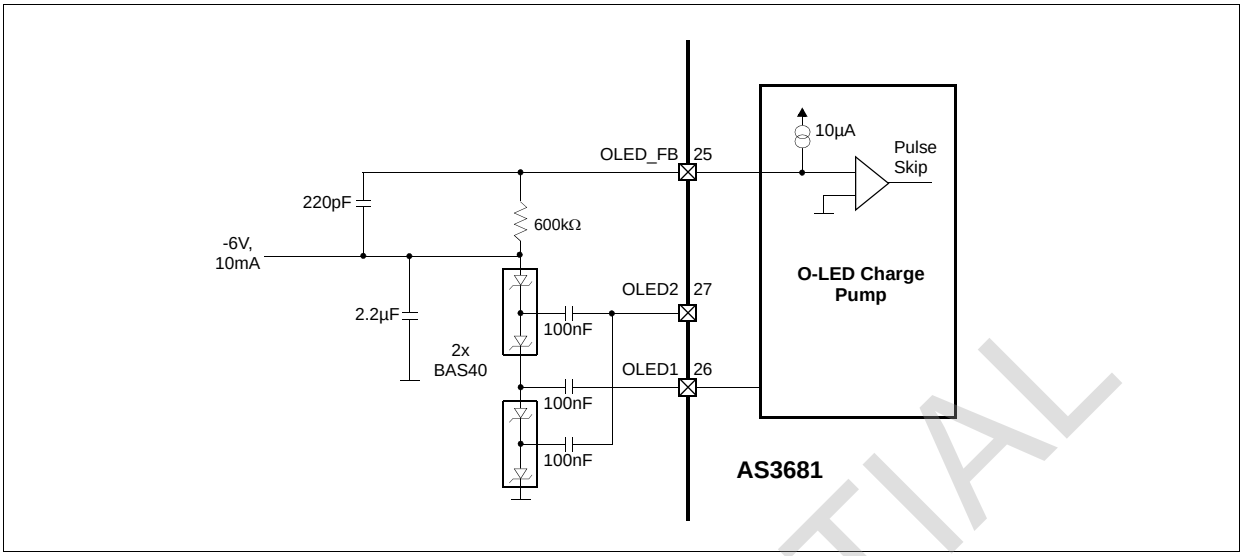


Figure 18. Minimum Output Voltage of Negative Charge Pump with 3 Flying Capacitors in Free-Running Mode (Unregulated, **cp_oled_mode** *(page 33) = 10b,* **low_power_mode** *(page 8) = 0)*

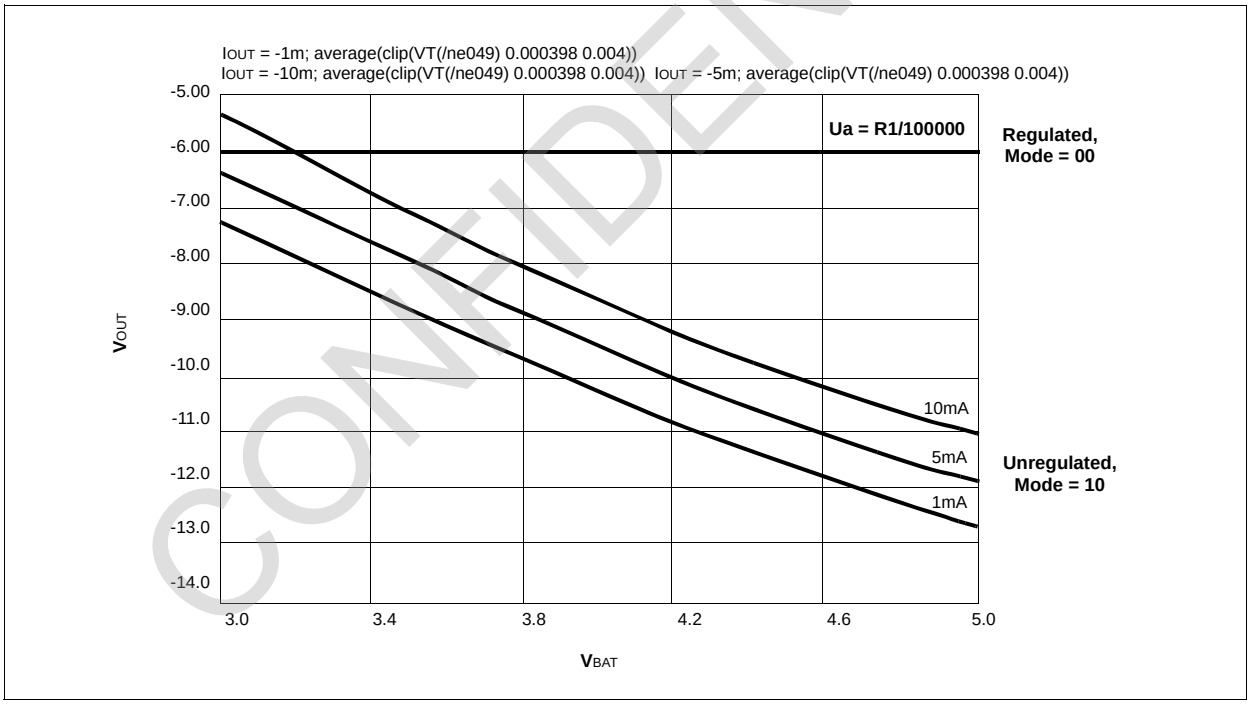


Figure 19. Positive Regulation

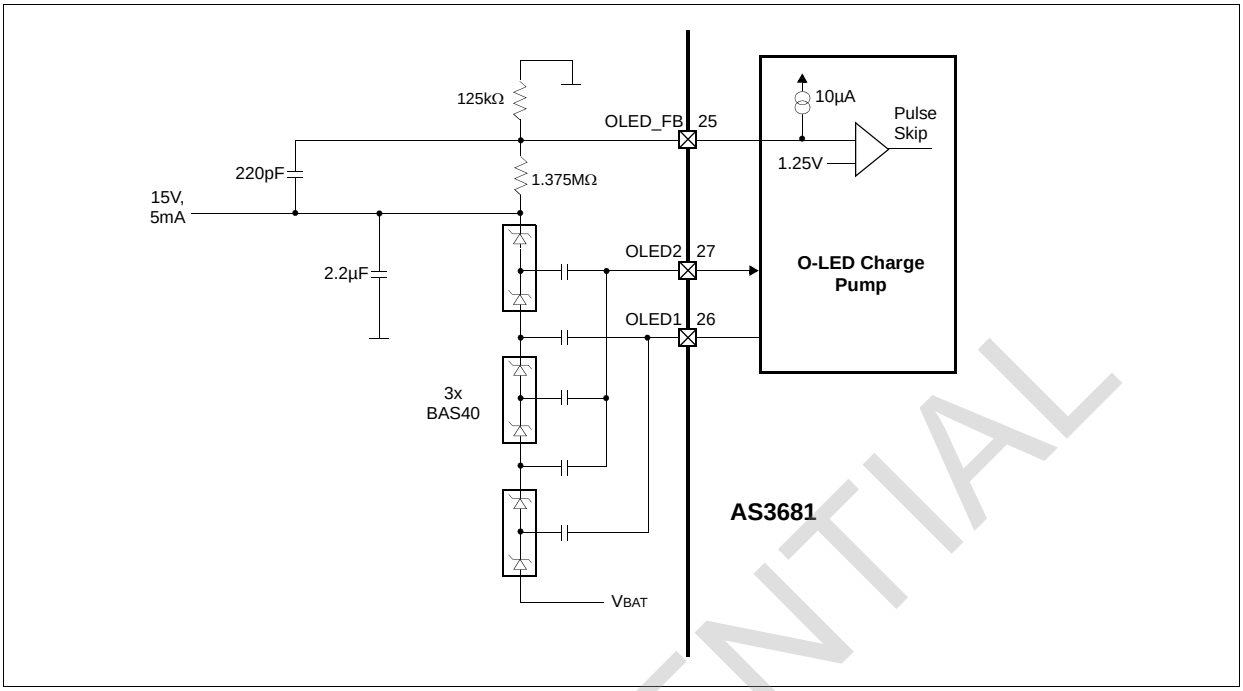
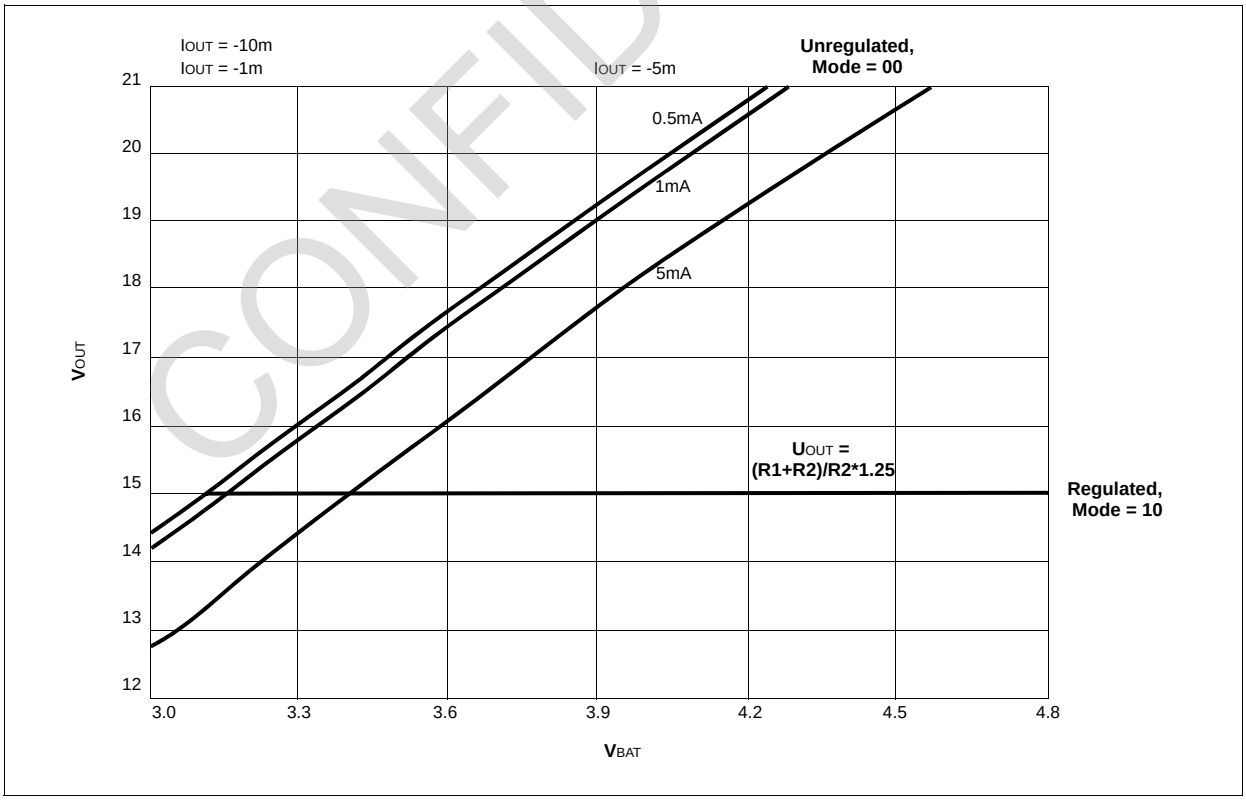


Figure 20. Minimum Output Voltage of Positive Charge Pump with 5 Flying Capacitors in Free-Running Mode (Unregulated, **cp_oled_mode** *(page 33) = 10b,* **low_power_mode** *(page 8) = 0)*



6.6.1 Charge Pump Registers

Addr: 00		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and AS3681 low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_on			(see ldo_on on page 8)
1	cp_oled_on			Controls the OLED Charge Pump. 0 = OLED Charge Pump off (1:1 mode). 1 = OLED Charge Pump on (1:1.5 or 1:2 mode).
2	cp_led_on	00	R/W	(see cp_led_on on page 17)
3	curr1_on			(see curr1_on on page 20)
5	curr2_on			(see curr2_on on page 20)
5	curr3_on			(see curr3_on on page 21)
6	step_up_on			(see step_up_on on page 13)
7	low_power_mode			(see low_power_mode on page 8)

Addr: 07		O-LED Charge Pump Mode		
		This register controls the O-LED External Charge Pump.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:1	cp_oled_mode	0	R/W	Defines the mode of the O-LED External Charge Pump. 00 = Regulate to negative voltage (e.g., -6V). 01= Regulate to positive voltage (e.g.,+15V). 10 = Unregulated (free-running). 11 = N/A
2	cp_oled_clk	0	R/W	Defines the switching frequency. 0 = 250kHz 1 = 500kHz
3	cp_oled_lowcurr	0	R/W	Driving capability of O-LED External Charge Pump. 0 = Normal current = I_{out} 1 = Reduced current = I_{out} /4 (reduces noise on supply and outputs).
4:7				N/A

6.7 General Purpose Inputs/Outputs

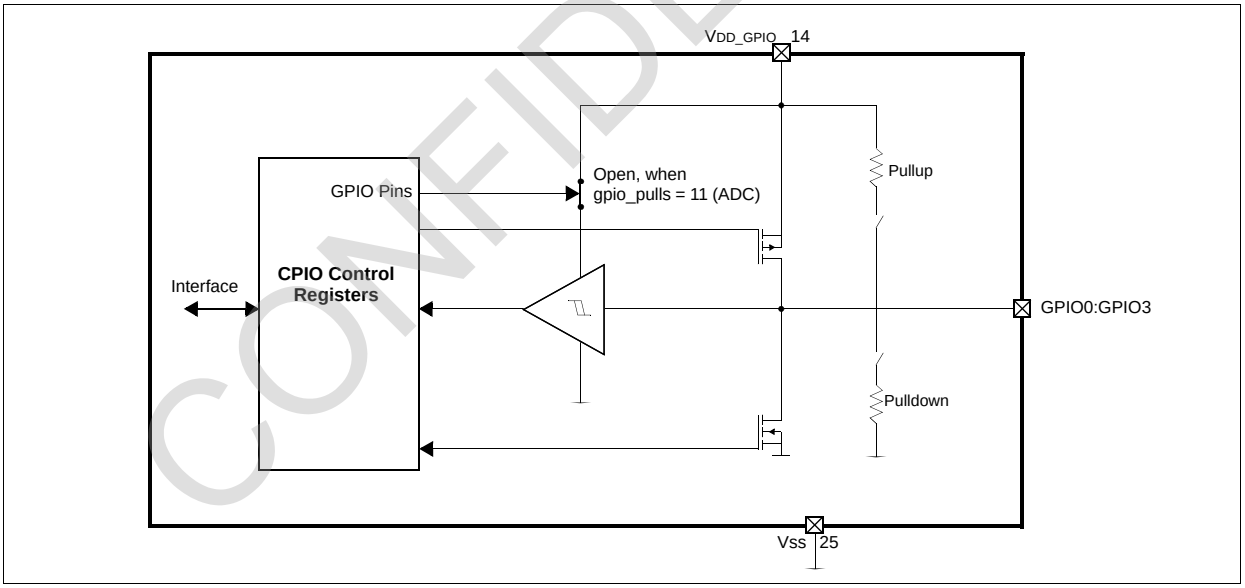
GPIO0:GPIO3 are four highly-configurable general purpose input/output pins which can be used for the following functionality (each GPIO pin is independent from the other GPIO pins):

- Digital Schmitt-Trigger Input
- Digital Output with 4mA Driving Capability at 2.8V Supply (V_{gpio})
- Tristate Output
- Analog Input to the ADC (GPIO0 and GPIO1)
- Strobe for Camera Flash Current Sink (GPIO2)
- PWM operation with Current Sink $CURR_1$ (GPIO3)
- Default Mode for GPIO2 and GPIO3 is Input (Pull-Down)
- Default Mode for GPIO0 and GPIO1 is ADC Input

Table 14. GPIO Pin Function Summary

GPIO Pin	Pin #	Configuration	Additional Function
GPIO0	16	Digital Input, Totem-Pole Output (Push/Pull), Open Drain (PMOS or NMOS), High-Z, Pull-Down or Pull-Up Resistor	ADC Input
GPIO1	15		ADC Input
GPIO2	13		Strobe Input for Photocamera Flash LED ($CURR_{3x}$)
GPIO3	12		PMW Control for $CURR_1$

Figure 21. GPIO Pin Connections



6.7.1 GPIO Characteristics

V_{gpio} is used as the supply voltage for all GPIOs.

Table 15. GPIO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{gpio}	Supply Voltage	1.5	3.3	V	
V_{IH}	High Level Input Voltage	0.7·V_{gpio}		V	
V_{IL}	Low Level Input Voltage		0.3·V_{gpio}	V	
V_{HYS}	Hysteresis	0.1·V_{gpio}		V	
I_{LEAK}	Input Leakage Current	-5	5	µA	To V_{gpio} and V_{SS}
V_{OH}	High Level Output Voltage	0.8·V_{gpio}		V	at -I_{out}
V_{OL}	Low Level Output Voltage		0.2·V_{gpio}	V	at I_{out}
I_{out}	Driving Capability	4		mA	V_{gpio} = 2.8V, **gpiox_low_curr** = 1 (page 37)
		16			V_{gpio} = 2.8V, **gpiox_low_curr** = 0
		1			V_{gpio} = 1.5V, **gpiox_low_curr** = 0 guaranteed by design.
		4			V_{gpio} = 1.5V, **gpiox_low_curr** = 1 guaranteed by design.
C_{LOAD}	Capacitive Load		50	pF	

6.7.2 GPIO Registers

Addr: 01		GPIO Output Signal		
		This register controls GPIO outputs and enables current sinks $CURR_4$ and $CURR_{51}$.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_out	0	R/W	Writes a logic signal to pin GPIO0; this is independent of any other bit setting e.g., **gpio0_mode**.
1	gpio1_out	0	R/W	Writes a logic signal to pin GPIO1; this is independent of any other bit setting e.g., **gpio1_mode**.
2	gpio2_out	0	R/W	Writes a logic signal to pin GPIO2; this is independent of any other bit setting e.g., **gpio2_mode**.
3	gpio3_out	0	R/W	Writes a logic signal to pin GPIO3; this is independent of any other bit setting e.g., **gpio3_mode**.
4:7				N/A
6	curr4_on	0	R/W	(see curr4_on on page 27)
7	curr51_on	0	R/W	(see curr51_on on page 27)

Addr: 08		GPIO01_control		
		This register controls GPIO0 and GPIO1 pin functions.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:1	gpio0_mode	00	R/W	Defines the direction for pin GPIO0. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
2:3	gpio0_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO0; this is independent of setting of bits **gpio0_mode**. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (**gpio0_mode** = XX); recommended for analog signals.
4:5	gpio1_mode	00	R/W	Defines the direction for pin GPIO1. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
6:7	gpio1_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO1; this is independent of setting of bits **gpio1_mode**. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (**gpio1_mode** = XX); recommended for analog signals.

Addr: 09		GPIO23_control		
		This register controls pins GPIO2 and GPIO3 pin functions.		
Bit	**Bit Name**	**Default**	**Access**	**Description.**
0:1	gpio2_mode	00	R/W	Defines the direction for pin GPIO2. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
2:3	gpio2_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO2; this is independent of setting of bits **gpio2_mode**. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (**gpio2_mode** = XX); recommended for analog signals.
4:5	gpio3_mode	00	R/W	Defines the direction for pin GPIO3. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
6:7	gpio3_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO3; this is independent of setting of **gpio3_mode** bits. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (**gpio3_mode** = XX); recommended for analog signals.

Addr: 11		GPIO_driving_cap		
		This register enables low current mode for GPIOs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_low_curr	0	R/W	Defines the driving capability of pin GPIO0. 0 = I_{out} 1 = $I_{out}/4$
1	gpio1_low_curr	0	R/W	Defines the driving capability of pin GPIO1. 0 = I_{out} 1 = $I_{out}/4$
2	gpio2_low_curr	0	R/W	Defines the driving capability of pin GPIO2. 0 = I_{out} 1 = $I_{out}/4$
3	gpio3_low_curr	0	R/W	Defines the driving capability of pin GPIO3. 0 = I_{out} 1 = $I_{out}/4$
4:7				N/A

Addr: 21		GPIO Input Signal		
		This register reads from the GPIO pins.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_in	N/A	R	Reads a logic signal from pin GPIO0; this is independent of any other setting e.g., bits **gpio0_mode**.
1	gpio1_in	N/A	R	Reads a logic signal from pin GPIO1; this is independent of any other setting e.g., bits **gpio1_mode**.
2	gpio2_in	N/A	R	Reads a logic signal from pin GPIO2; this is independent of any other setting e.g., bits **gpio2_mode**.
3	gpio3_in	N/A	R	Reads a logic signal from pin GPIO3; this is independent of any other setting e.g., bits **gpio3_mode**.
4:7				N/A

6.8 Analog-to-Digital Converter

The AS3681 has a built-in 10-bit successive approximation analog-to-digital converter (ADC). It is internally supplied by V_{2_5}, which is also the full-scale input range. Consequently, the resolution is:

$$V_{LSB} = \frac{V_{2\_5}}{2^{10}} = 2.44mV \quad \text{(EQ 4)}$$

Table 16. ADC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Resolution	10			Bit	
V_{in}	Input Voltage Range	V_{SS}		V_{supply}	V	$V_{supply} = V_{2\_5}$
D_{NL}	Differential Non-Linearity		±0.25		LSB	
I_{NL}	Integral Non-Linearity		±0.5		LSB	
V_{os}	Input Offset Voltage		±0.25		LSB	
R_{in}	Input Impedance	100			MΩ	
C_{in}	Input Capacitance			9	pF	
$V_{supply}(V_{2\_5})$	Power Supply Range		2.5		V	±2%, internally trimmed.
I_{dd}	Power Supply Current		500		µA	During conversion only.
I_{dd}	Power Down Current		100		nA	
Transient Parameters (2.5V, 25ºC)						
T_c	Conversion Time		11		µs	
f_c	Clock Frequency			1	MHz	
Dc	Clock Duty Cycle	40		60	%	
t_s	Settling Time of S&H		4		µs	

6.8.1 ADC Registers

Addr: 18		ADC_control		
		This register input source selection and initialization of ADC.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:3	gpio_select	0	R/W	Selects GPIO pin as ADC input. 0000 = GPIO0 0001 = GPIO1 0010 = $CURR_1$ voltage (up to 1V only). 0011 = $CURR_2$ voltage (up to 1V only). 0100 = $CURR_{30}$ voltage (up to 1V only). 0101 = $CURR_4$ voltage (up to 1V only). 0110 = RGB_1 voltage (up to 1V only).
4:6				N/A
7	start_conversion	N/A	W	Writing a 1 into this bit starts one ADC conversion cycle.

Addr: 19		ADC_MSB Result		
		Together with Register 20, this register contains the results (MSB) of an ADC cycle.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:6	D3:D9	N/A	R	ADC results register.
7	result_not_ready	N/A	R	Indicates end of ADC conversion cycle. 0 = Result is ready. 1 = Conversion is running.

Addr: 20		ADC_LSB Result		
		Together with Register 19, this register contains the results (LSB) of an ADC cycle		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0:2	D0:D2	N/A	R	ADC result register.
3:7				N/A

Figure 22. ADC Timing Diagrams

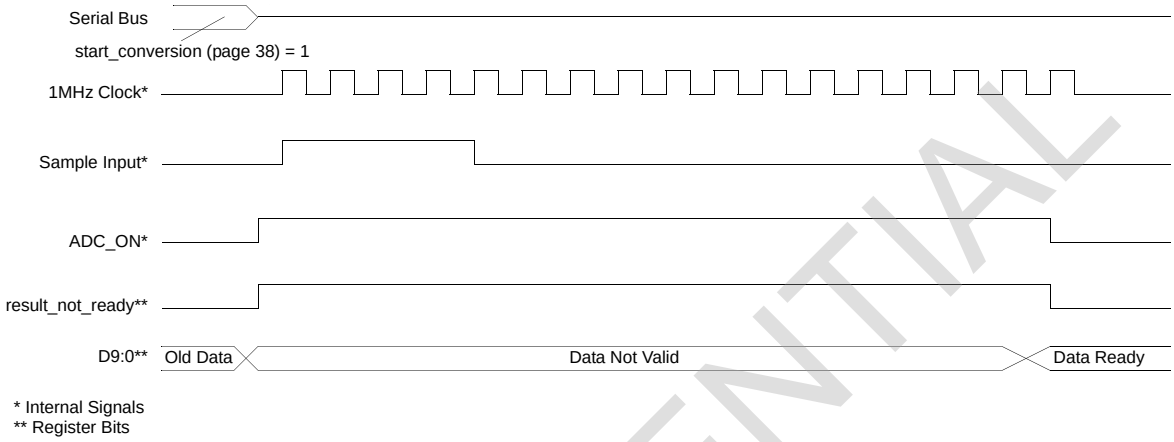
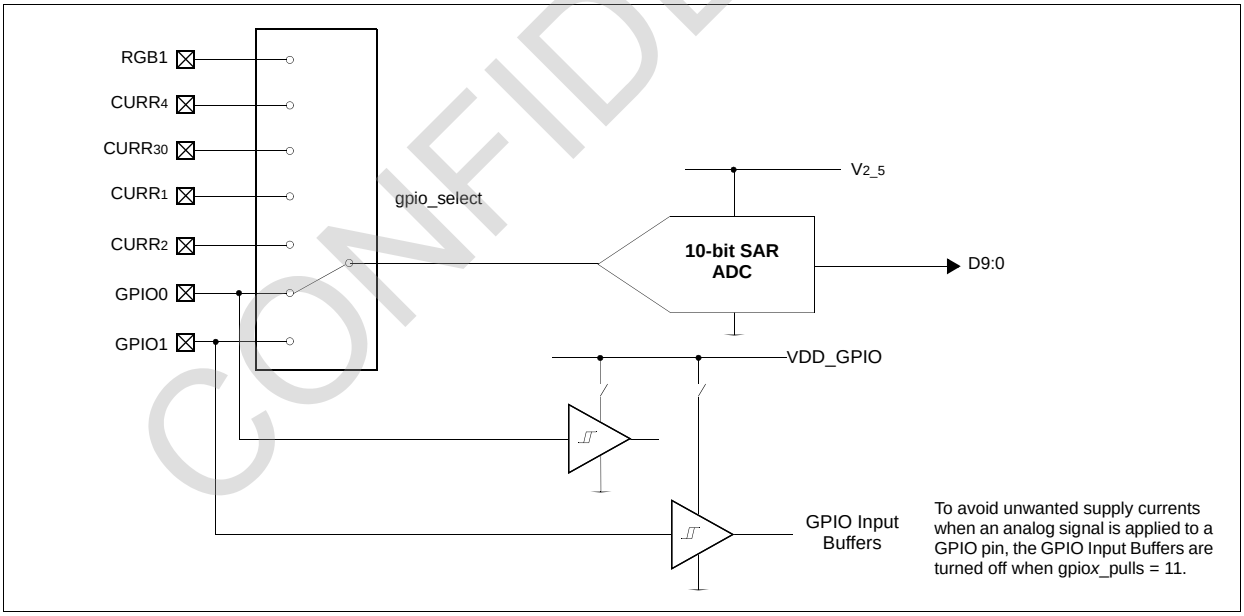


Figure 23. ADC Pin Connections



6.9 Power-On Reset

The internal reset is controlled by two sources:

- V_{BAT3} Supply
- V_{DD_GPIO} Voltage

If one of the voltages is lower than its limit, the internal reset is forced.

Table 17. Reset Levels

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{POR_VBAT}	Overall Power-On Reset		2.0		V	Monitor voltage on V_{2_5}; power-on reset for all internal functions.
$V_{GPIO\_Vdd\_TH\_RISING}$	Reset Level for V_{DD_GPIO} Rising		1.3		V	Monitor voltage on V_{DD_GPIO}; rising level.
$V_{GPIO\_vdd\_TH\_FALLING}$	Reset Level for V_{DD_GPIO} Falling		1.0		V	Monitor voltage on V_{DD_GPIO}; falling level.

6.9.1 Reset Control

The reset levels control the state of all registers. As long as V_{BAT} and V_{DD_GPIO} are below their reset thresholds, the register contents are set to default. Access by serial interface is possible once the reset thresholds are exceeded (see Table 18).

Table 18. Reset Control

Reset Control	Register State (All Registers)	Register 00, Bit ldo_on =
$V_{BAT} < V_{POR\_VBAT}$ and $V_{DD\_GPIO} < V_{GPIO\_vdd\_TH}$	Default	0
$V_{BAT} < V_{POR\_VBAT}$ and $V_{DD\_GPIO} > V_{GPIO\_vdd\_TH}$	Default	0
$V_{BAT} > V_{POR\_VBAT}$ and $V_{DD\_GPIO} < V_{GPIO\_vdd\_TH}$	Default	0
$V_{BAT} > V_{POR\_VBAT}$ and $V_{DD\_GPIO} > V_{GPIO\_vdd\_TH}$	Default	1
	Access via Serial Interface Possible	

Where:

$V_{GPIO\_vdd\_TH}$ = Use rising or falling threshold levels, depending on the slope of V_{DD_GPIO} (power up/power down).

6.10 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3681. This sensor generates a flag if the device temperature reaches the overtemperature threshold of 140º. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the 140º threshold all bits in Register 00 are set to 00h and the **ov_temp** flag is set. After decreasing the temperature by 5º, typically the previous state is reloaded into Register 00.

The **ov_temp** flag can only be reset by first writing a 1 and then a 0 to the (bit **rst_ov_temp**).

Bit **ov_temp_on** = 1 activates temperature supervision.

Table 19. Overtemperature Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{140}	ov_temp Rising Threshold		140		ºC	
T_{hyst}	ov_temp Hystersis		5		ºC	

6.10.1 Temperature Supervision Registers

Addr: 22		Overtemp Control		
		This register reads and resets the overtemperature flag.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ov_temp_on	N/A	W	Activates/deactivates device temperature supervision. Default: Off – all other bits are only valid if this bit is set to 1. 0 = Temperature supervision is disabled. No reset will be generated if the device temperature exceeds 140ºC. 1 = Temperature supervision is enabled.
1	ov_temp	N/A	R	1 = Indicates that the overtemperature threshold has been reached; this flag is not cleared by an overtemperature reset. It has to be cleared using bit **rst_ov_temp**.
2	rst_ov_temp	0	R/W	The **ov_temp** flag is cleared by first setting this bit to 1, and then setting this bit to 0.
3:7				N/A

6.11 Serial Interface

The AS3681 is controlled using serial interface pins 17 (CLK) and 18 (DATA).

6.11.1 Serial Interface Features

- Fast Mode Capability (Maximum Clock Frequency is 400 kHz)
- 7-bit Addressing Mode
- Write Formats
  - Single-Byte Write
  - Page-Write
- Read Formats
  - Current-Address Read
  - Random-Read
  - Sequential-Read
- DATA Input Delay and CLK Spike Filtering by Integrated RC Components

6.11.2 Device Address Selection

The serial interface address of the AS3681 can be selected between two fixed settings:

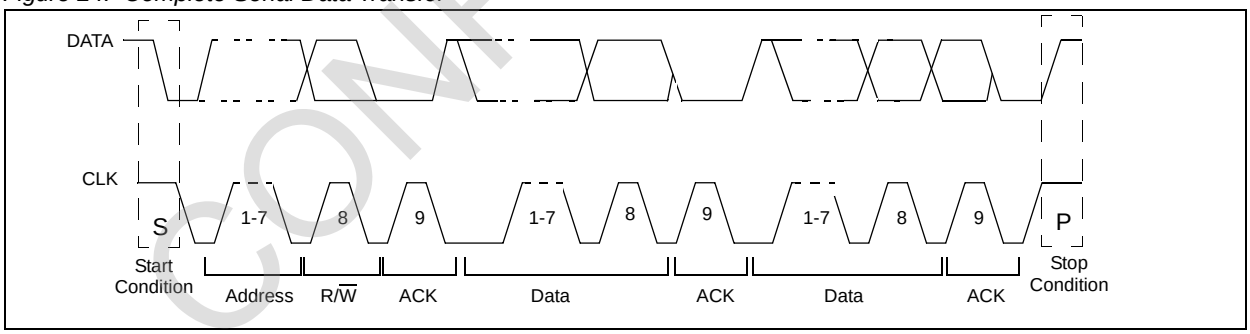
- 80h or 82h – Write Commands
- 81h or 83h – Read Commands

The address is selected by connecting ADDR (pin 1) to either VSS (pin 33) or to V2_5 (pin 30) as indicated in Table 20.

Table 20. AS3681 Device Address Selection

ADDR Connected To	Serial Interface Address		Notes
	Write	Read	
VSS (Pin 33)	80h	81h	
V2_5 (pin 30)	82h	83h	Maximum Voltage = 2.5V

Figure 24. Complete Serial Data Transfer



Serial Data Transfer Formats

Definitions used in the serial data transfer format diagrams (Figures 25 - 29) are listed in Table 21.

Table 21. Serial Data Transfer Byte Definitions

Symbol	Definition	R/W (AS3681 Slave)	Notes
S	Start Condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW1	Device Address for Write	R	10000010b (80h); pin 1 connected to VSS.
DW2	Device Address for Write	R	10000010b (82h); pin 1 connected to V2_5.
DR1	Device Address for Read	R	10000011b (81h); pin 1 connected to VSS.

Table 21. Serial Data Transfer Byte Definitions (Continued)

Symbol	Definition	R/W (AS3681 Slave)	Notes
DR2	Device Address for Read	R	10000011b (83h); pin 1 connected to V_{2_5}.
WA	Word Address	R	8 bits
A	Acknowledge	W	1 bit
N	Not Acknowledge	R	1 bit
reg_data	Register Data/Write	R	8 bits
data (n)	Register Data/read	R	1 bit
P	Stop Condition	R	8 bits
WA++	Increment Word Address Internally	R	During Acknowledge

Figure 25. Serial Interface Byte Write

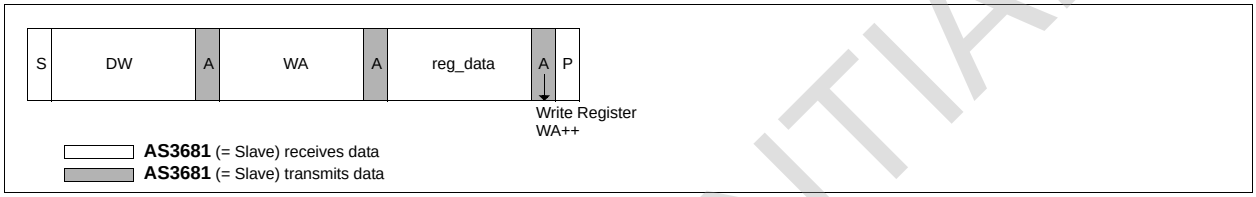
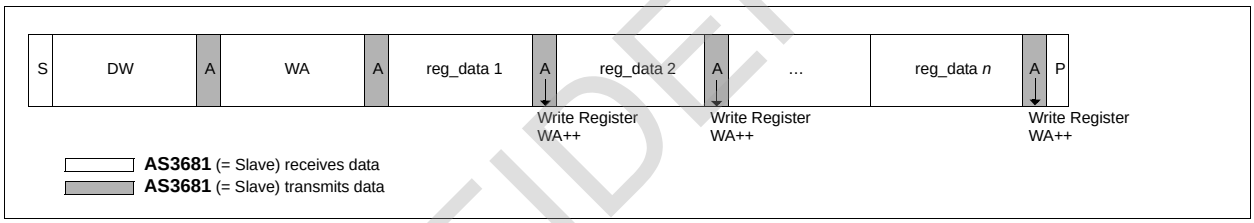


Figure 26. Serial Interface Page Write



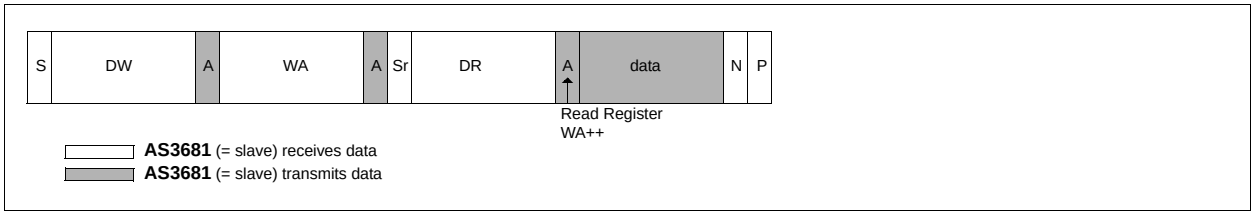
Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The following diagrams show the serial read formats supported by the AS3681.

Figure 27. Serial Interface Random Read

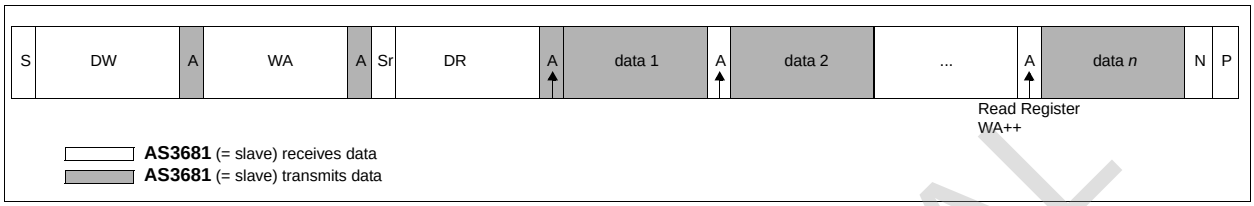


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st CLK pulse after the ACKNOWLEDGE bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a NOT ACKNOWLEDGE, and issues a STOP condition on the bus.

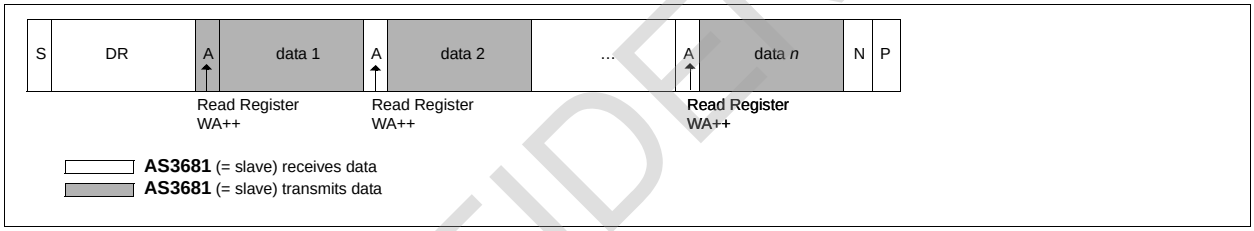
Figure 28. Serial Interface Sequential Read



Sequential Read is the extended form of Random Read, as multiple register-data bytes are subsequently transferred.

In contrast to the Random Read, in a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a NOT ACKNOWLEDGE following the last data byte and subsequently generate the STOP condition.

Figure 29. Serial Interface Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address.

Analogous to Random Read, a single byte transfer is terminated with a NOT ACKNOWLEDGE after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes must be responded to with an ACKNOWLEDGE from the master.

For termination of the transmission the master sends a NOT ACKNOWLEDGE following the last data byte and a subsequent STOP condition.

7 Register Map

The AS3681 control register addresses, default values, and pages where they are described are listed in Table 22.

Table 22. AS3681 Register Map

Register Name	Addr.	Def.	B7	B6	B5	B4	B3	B2	B1	B0	Page
Reg. Control	00		low_power_mode	step_up_on	curr3_on	curr2_on	curr1_on	cp_led_on	cp_oled_on	ldo_on	8, 13, 17, 20, 21, 33
GPIO Output Signal	01	00h	curr51_on	curr4_on	gpio5_out	gpio4_out	gpio3_out	gpio2_out	gpio1_out	gpio0_out	27, 35
Curr12_value	02	00h	curr2_current				curr1_current				20
Curr3_value	03	00h	curr3_current_preview				curr3_current_strobe				21
Current Sink1-2 Control	04	00h	curr53_on	curr52_on	rgb_on	curr_test			N/A	curr1_pwm	20, 25, 28
Current Sink3 Control	05	00h	N/A				strobe_control				22
Ldo_voltage_control	06	13h	N/A			ldo_v					9
O-LED Charge Pump Mode	07	00h	N/A				cp_oled_lowcurr	cp_oled_clk	cp_oled_mode		33
GPIO01_control	08	44h	gpio1_pulls		gpio1_mode		gpio0_pulls		gpio0_mode		36
GPIO23_control	09	44h	gpio3_pulls		gpio3_mode		gpio2_pulls		gpio2_mode		36
GPIO_driving_cap	11	00h	N/A				gpio3_low_curr	gpio2_low_curr	gpio1_low_curr	gpio0_low_curr	37
DCDC Control	12	00h	N/A	step_up_vtuning				step_up_fb		step_up_frequ	13
DCDC Test	13	00h	N/A				curr3_mode	curr3_high	skip_fast	step_up_res	13, 22
Curr45_current	14	00h	curr5_current				curr4_current				28
rgb12_current	15	00h	rgb2_current				rgb1_current				26
rgb3_current	16	00h	N/A				rgb3_current				22, 26
CP Control	17	00h	N/A					cp_mode		cp_clk	17
ADC_control	18	00h	start_conversion	N/A			gpio_select				38
ADC_MSB Result	19	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3	38
ADC_LSB Result	20	NA	N/A					D2	D1	D0	39
GPIO Input Signal	21	NA	N/A				gpio3_in	gpio2_in	gpio1_in	gpio0_in	37
Overtemp Control	22	00h	N/A					rst_ov_temp	ov_temp	ov_temp_on	41
Curr_low_voltage_control	23		N/A	curr53_low_voltage	curr52_low_voltage	curr51_low_voltage	curr4_low_voltage	curr3_low_voltage	curr2_low_voltage	curr1_low_voltage	20, 23, 28
Test_enable*	24	NA	test_en_code	N/A							
Testmux_control*	25	00h	test	N/A							
Testmode_control*	26	00h	N/A	fuse_force_readout	fuse_test_on	fuse_testmode	testmode	atpg_mode	N/A		
Fuse Reg1*	27	NA	VrefTrim	RefOsc1 Mhz1	N/A						
Fuse Reg2*	28	NA	Spare	N/A							
ASIC ID1*	29	tbd	1	1	0	0	1	1	0	1	
ASIC ID2*	30	tbd	0	1	0	1	revision				
write_prot	31	N/A	write_prot								28

Read-Only
Write

Note: * These registers are for internal use only.

8 External Components

8.1 Capacitor Selection

It is recommended to use low ESR ceramic capacitors with X7R or X5R dielectric as they provide good filtering and have a wide temperature range.

Note: For 100nF capacitors it is possible to use ceramic capacitors arrays.

All other capacitors are available in 0603 package for 1µF and 2.2µF.

The output of the Step Up DC/DC Converter may be buffered using two 1µF capacitors in a 0805 package or one 2.2µF capacitor in a 1206 package (up to 16VDC).

Caution: All capacitors must be placed as close as possible to the AS3681.

8.2 Diode Selection

A Schottky diode is recommended for the Step Up DC/DC Converter, for example:

- CMDSH2-3 in SOD-232 Package – Central Semiconductor
- MBR0520 in SOD-123 Package – ON Semiconductor

It is also possible to use normal high speed silicon diodes with reduced efficiency (0.3V higher forward-voltage results in 2% lower efficiency at 15V output voltage), for example:

- CMOD4448 in SOD-523 Package – Various Vendors

8.3 Inductor Selection

Table 23 lists some inductors that can be used with the Step Up DC/DC Converter, although there are many other suitable inductors available.

Note: For high efficiency the serial resistance DCR should be as low as possible.

Table 23. Example Inductors

Part number	Inductance	Dimension	DCR	I_{sat}	I_{rms}	Manufacturer	Maximum Output Power @V_{BAT}>3.2V (Preliminary)
976AS-100M	10µH	3.6 x 3.6 x 1.2mm	0.8Ω	0.5A		Toko www.toko.com	0.5W(16V x 30mA)
SD12-100M	10µH	5 x 5 x 1.2mm	0.3Ω	0.8A	0.9A	Coiltronics www.coiltronics.com	1W(16V x 60mA)
							1W(25V x 40mA)
LPO1704-103	10µH	6.6 x 5.5 x 1.0mm	0.41Ω	0.8A	1.1A	Coilcraft www.coilcraft.com	1W(16V x 60mA)
							1W(25V x 40mA)
CDRH2D11-100NC	10µH	3.2 x 3.2 x 1.2mm	0.4Ω	0.3A		Sumida www.sumida.com	0.5W(16V x 30mA)

8.4 Transistor Selection

For optimum efficiency use a NMOSFET transistor with a small R_{on} resistance, low V_{G-S} threshold, and a small gate charge, for example:

- Si1304 NMOSFET TrenchFET, R_{on} = 0.35Ω, Vds=25V (Vishay Siliconix, www.vishay.com) for 1W Output Load
- Si1012 NMOSFET TrenchFET, R_{on} = 0.7Ω, Vds=20V (Vishay Siliconix, www.vishay.com) for 0.5W Output Load

8.5 Resistor Selection

All resistors should have a tolerance of ±1%.

For the DCDC shunt resistor (0.15Ω) ±5% will be sufficient.

8.6 External Component Specifications

Table 24. External Components List

Part Number	Value			Tol (Min)	Rating (Max)	Notes	Package (Min)
	Min	Typ	Max				
C1		100nF		±20%	6.3V	Ceramic, X5R (CREF)	0402
C2	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (SENSE_P or VBAT3)	0603
C3		2.2µF		±20%	6.3V	Ceramic, X5R (VANA)	0603
C4	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (V2_5)	0603
C5		2.2µF		±20%	6.3V	Ceramic, X5R (VBAT1, VBAT2)	0603
C6		1µF		±20%	6.3V	Ceramic, X5R (Charge Pump)	0603
C7		1µF		±20%	6.3V	Ceramic, X5R (Charge Pump)	0603
C8		2.2µF		±20%	6.3V	Ceramic, X5R (Charge Pump Output)	0603
C9		2.2µF		±20%	25V	Ceramic, X5R, X7R (Step Up DC/DC Converter)	1206
C10		1.5nF		±20%	25V	Ceramic, X5R (Step Up DC/DC Converter Feedback)	0402
C11		15nF		±20%	6.3V	Ceramic, X5R (Step Up DC/DC Converter Feedback)	0402
C12		100nF		±20%	6.3V	Ceramic, X5R (External Charge Pump)	0402
C13		100nF		±20%	6.3V	Ceramic, X5R (External Charge Pump)	0402
C14		100nF		±20%	6.3V	Ceramic, X5R (External Charge Pump)	0402
C15		2.2µF		±20%	25V	Ceramic, X5R (External Charge Pump Output)	0603
R1		240kΩ		±1%		Bias Resistor	0201
R2		150mΩ		±5%		Shunt Resistor	0805
R3		1MΩ		±1%		Step Up DC/DC Converter Voltage Feedback	0201
R4		100kΩ		±1%		Step Up DC/DC Converter Voltage Feedback	0201
R5	400kΩ		1.5MΩ	±1%		External Charge Pump Feedback	0201
R6	1kΩ		10kΩ	±1%		Bias Resistor	0201
L1		10µH		±20%		Recommended Type: Coiltronics SD-12-100	
D1	CMDSH2-3 or similar					Shottky Diode; Central Semiconductor	SOD232
D2:D22	LED					LEDs as required by application	
Q1	Si1304 or similar					NMOS switching transistor; Vishay	SOT-323

9 Pinout and Packaging

9.1 Pin Descriptions

Table 25. Pinlist QFN32

Pin	Name	Type	Description
1	ADDR	DI	Input pin to select serial interface address; apply fuse-programming voltage here. Maximum voltage during normal operation = 2.5V.
2	$C2_N$	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 1µF (±20%) to this pin.
3	V_{BAT2}	S	Charge Pump supply pad. **Note:** Always connect this pin to V_{BAT}.
4	$C2_P$	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 2.2µF (±20%) to this pin.
5	CP_OUT	AIO	Output voltage of the Charge Pump; connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
6	V_{BAT1}	AIO	Supply pad for Charge Pump. **Note:** Always connect this pin to V_{BAT}.
7	$C1_P$	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 2.2µF (±20%) to this pin.
8	$C1_N$	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 1µF (±20%) to this pin.
9	$CURR_{30}$	AI	Analog current sink input (intended for LED flash).
10	$CURR_{31}$	AI	Analog current sink input (intended for LED flash).
11	$CURR_{32}$	AI	Analog current sink input (intended for LED flash).
12	GPIO3	DIO3	General purpose input/output.
13	GPIO2	DIO3	General purpose input/output.
14	V_{DD_GPIO}	S	Supply pad for GPIOs and serial interface.
15	GPIO1	DIO3	General purpose input/output, ADC input.
16	GPIO0	DIO3	General purpose input/output, ADC input.
17	CLK	DI3	Clock input for serial interface.
18	DATA	DIO3	Serial interface data input/output.
19	$CURR_1$	AI_HV	Analog current sink input (intended for LED).
20	$CURR_2$	AI_HV	Analog current sink input (intended for LED).
21	V_{BAT3}	S	Supply pad; always connect to V_{BAT}.
22	V_{ANA}	AO	Output voltage of the Analog LDO. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
23	SENSE_N	AIO	Negative sense input of shunt resistor for Step Up DC/DC Converter.
24	SENSE_P	AIO	Positive sense input of shunt resistor for Step Up DC/DC Converter.
25	OLED_FB	AI	Feedback input of O-LED Charge Pump. Connect this pin to a resistor string.
26	OLED1	AO	OLED1 driver.
27	OLED2	AO	OLED2 driver.
28	DCDC_GATE	AO	DCDC gate driver.
29	DCDC_FB	AI	DCDC feedback. Connect to resistor string.
30	$V2_5$	AO3	Output voltage of the Low-Power LDO; always connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%). **Caution:** Do not load this pin during device startup.
31	C_{REF}	AIO	Bypass capacitor for the internal voltage reference; always connect a capacitor of 100nF. **Caution:** Do not load this pin.

Table 25. Pinlist QFN32 (Continued)

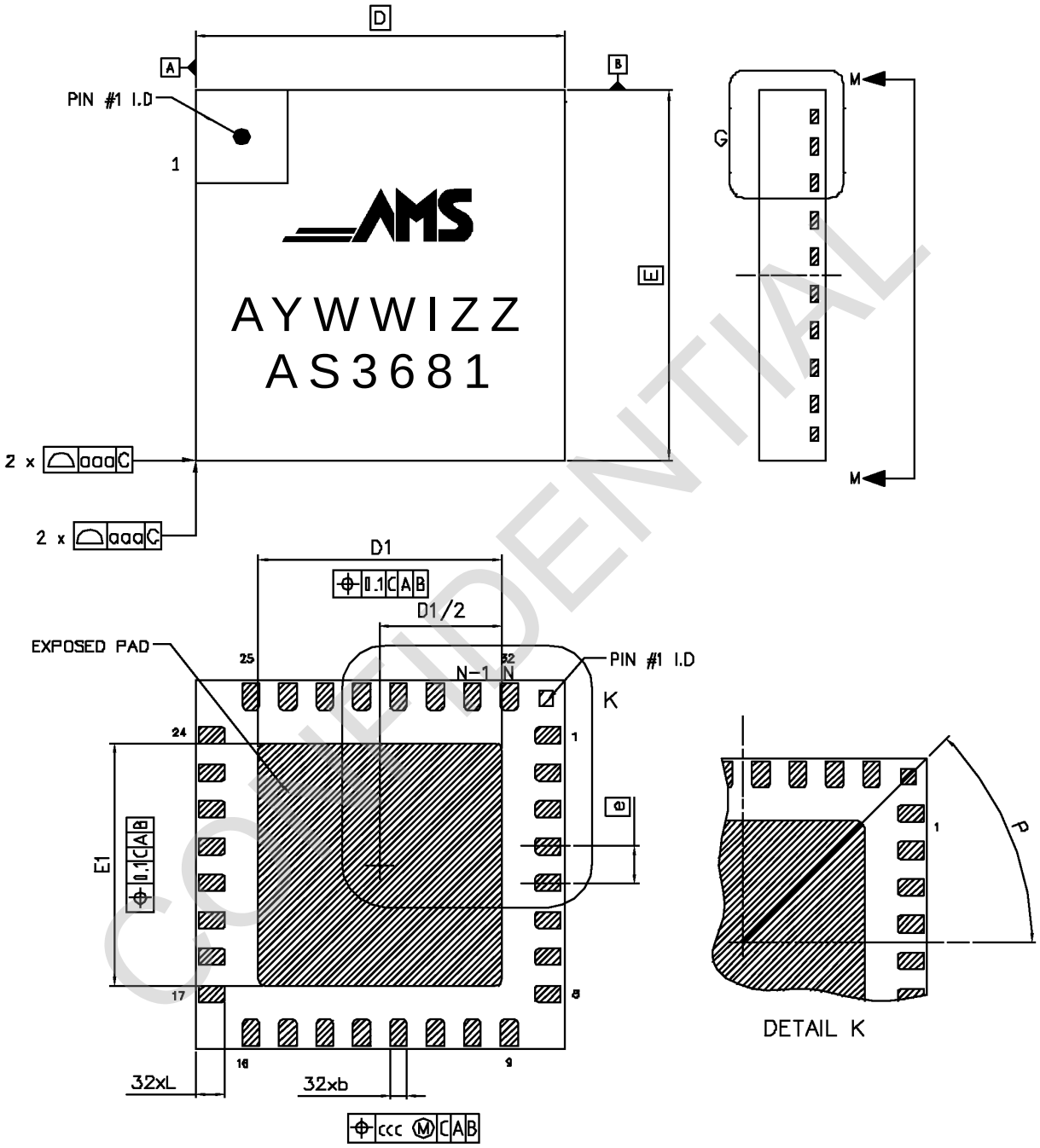
Pin	Name	Type	Description
32	RBIAS	AIO	External resistor; always connect a resistor of 240kΩ (±1%) to ground. **Caution:** Do not load this pin.
33	VSS	VSS	Ground pad (QFN32: exposed paddle).

Table 26. Pin Type Definitions

Type	Description
DI	Digital Input
DI3	3.3V Digital Input
DO	Digital Output
DIO	Digital Input/Output
DIO3	3.3V Digital Input/Output
OD	Open Drain (the device can only pulldown this type of pin)
AIO	Analog Pad
AI	Analog Input
AI_HV	High-Voltage (15V) Pin
AO	Analog Output (5V)
AO3	Analog Output (3.3V)
S	Supply Pad
GND	Ground Pad

9.2 Package Drawings and Markings

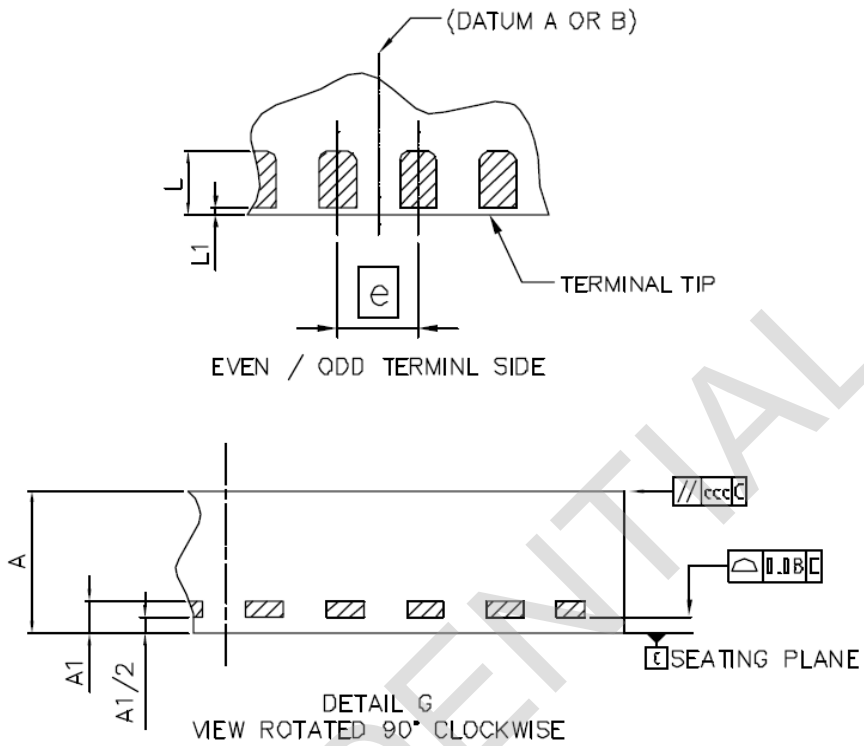
Figure 30. QFN 32 – 5x5mm with Exposed Paddle



JEDEC Package Outline Standard: MO-220 VHHD-5 – Lead Finish: 100% Sn "Matte Tin".

Marking: AYWWIZZ
A: Pb-Free Identifier
Y: Last Digit of Manufacturing Year
WW: Manufacturing Week
I: Plant Identifier
ZZ: Traceability Code

Figure 31. QFN 32 – Detail Diagram



DIM	MIN	NOM	MAX
A	0.80		1.00
A1		0.203 REF	
b	0.18	0.23	0.30
D		5.00 BSC	
E		5.00 BSC	
D1	3.50	3.60	3.70
E1	3.50	3.60	3.70
e		0.50 BSC	
L	0.30	0.40	0.50
L1			0.10
P		45° BSC	
aaa		0.15	
ccc		0.10	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCE	REFERENCE DOCUMENT
Millimeter(mm)	ASME Y14.5M	JEDEC MO-220

10 Ordering Information

Device ID	Part Number	Package Type	Delivery Form*	Description
AS3681-*PDR*-Z	AS3681-EAA-Z	QFN 32	Tape and Reel	5 x 5mm, Pitch = 0.5mm
	AS3681-EBA-Z	QFN 32	Tube	5 x 5mm, Pitch = 0.5mm

Where:

P = **Package Type**:
E = QFN 5 x5 x 1mm

D = **Delivery Form**:
A = Tape and Reel
B = Tube

R = **Revision**

Z = **Pb-Free IC Package**

* Dry-pack sensitivity level = 3 in accordance with *IPC/JEDEC J-STD-033A.*

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Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

e-mail: info@austriamicrosystems.com

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