AS3810

16 Channel White LED Driver for LCD Backlight

General Description

The AS3810 is a 16 channels precision LED driver for use in LCD backlight panels.

Dynamic power feedback controls the external power supply to guarantee best efficiency. Built-in safety features include thermal shutdown as well as open and short LED detection. The device is programmable via serial interface.

Key Benefits & Features

The benefits and features of AS3810, 16 Channel White LED Driver for LCD Backlight are listed below:

Figure 1:
Added Value of Using A3810

Benefits	Features
• Optimum power savings through local dimming	• 16 fully flexible 12 bit PWM generators (period, high time, delay, reverse) • Global dimming through VSYNC input possible
• Highest brightness uniformity	• One global high accurate 8 bit IDAC which sets the LED current (±1% accuracy)
• Synchronization with TV frame	• VSYNC and HSYNC inputs available to synchronize the PWM generators (1)
• Lowest BOM	• Due to integrated FETs and current set resistors. 8kV ESD at current outputs to avoid external ESD protection.
• Digital enhanced DC-DC feedback	• Feedback function is compatible to every DC-DC architecture and configurable via SPI (1)
• On-chip safety features	• SHORT/OPEN LED detection, temperature shutdown, register lock/unlock,
• Highest contrast ratios	• Due to very fast current output stage (minimum PWM on time)
• Easy scalable system	• Devices programmable through SPI and daisy chaining of several devices possible

Note(s):

1. System patent

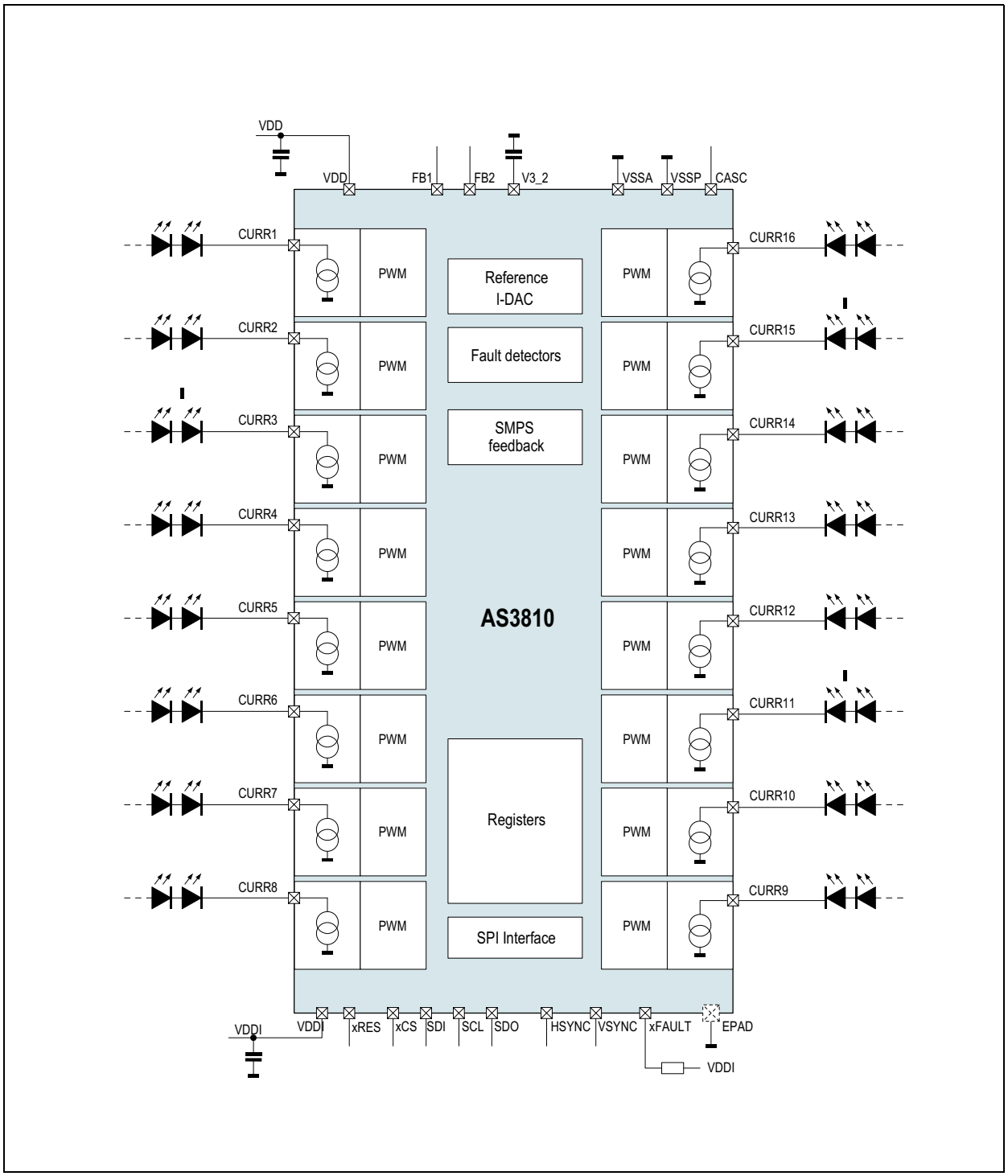
Applications

The AS3810 is suitable for LED backlighting for LCD such as TV sets and monitors

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS3810 Block Diagram



Pin Assignment

Figure 3:
Pin Diagram (Top View)

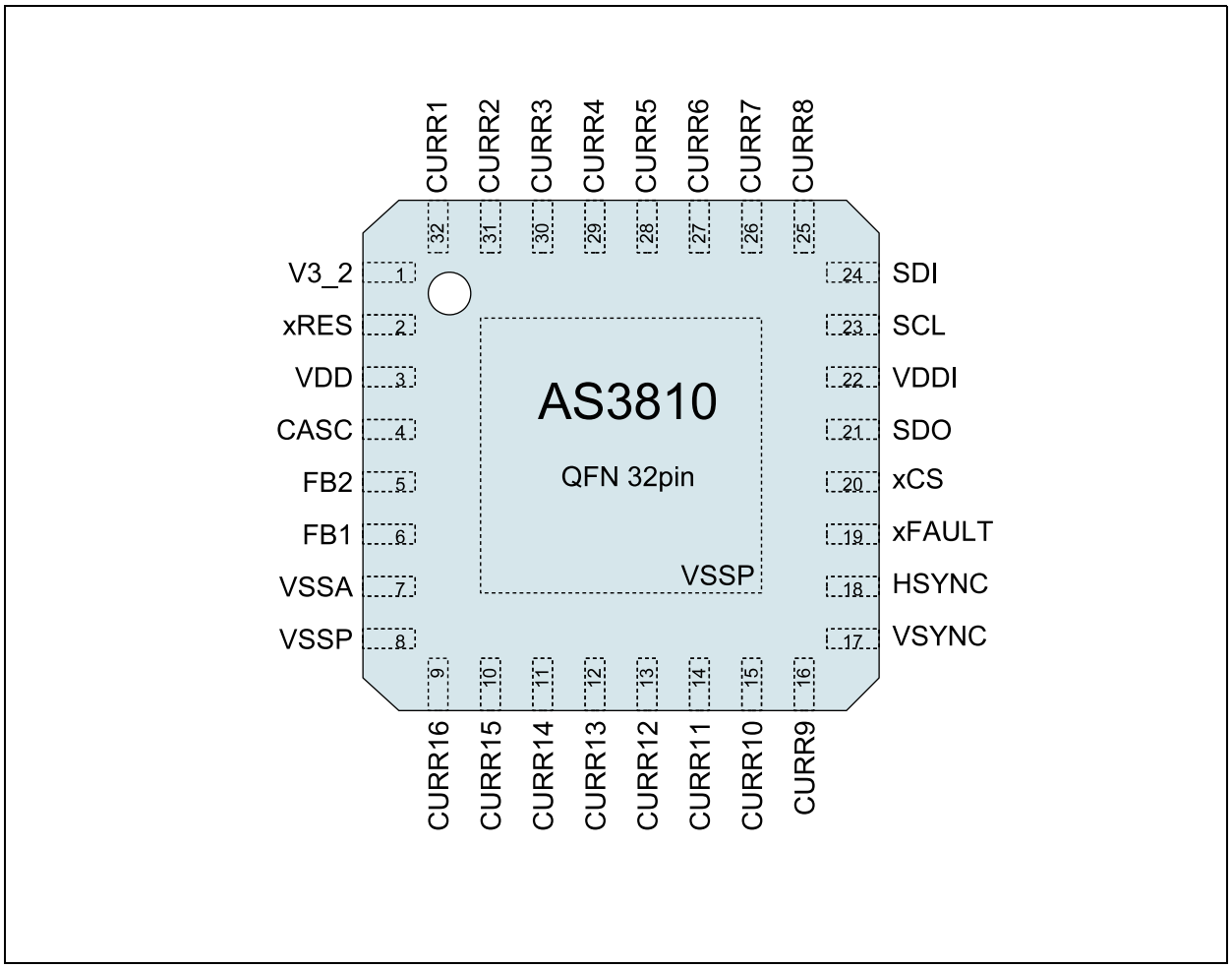


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	V3_2	Analog pin	Digital supply output. Connect 2.2µF bypass capacitor to GND
2	xRES	Digital input	Reset input active low

Pin Number	Pin Name	Pin Type	Description
3	VDD	Analog pin	Power supply. Connect 4.7µF bypass capacitor to GND
4	CASC		Connect to external cascode circuit
5	FB2		Power supply feedback output2
6	FB1		Power supply feedback output1
7	VSSA		GND
8	VSSP		GND
9	CURR16		LED current output
10	CURR15		LED current output
11	CURR14		LED current output
12	CURR13		LED current output
13	CURR12		LED current output
14	CURR11		LED current output
15	CURR10		LED current output
16	CURR9		LED current output
17	VSYNC	Digital input with pulldown resistor	Vertical sync frequency
18	HSYNC		Clock input for PWM generators
19	xFAULT	Digital output open drain	Fault output. Open drain. Connect pullup to VDDI
20	xCS	Digital input with pullup resistor	SPI interface chip select
21	SDO	Digital output	SPI interface data output. Tristate output.
22	VDDI	Analog pin	Power supply of digital input/output cells
23	SCL	Digital input with pulldown resistor	SPI interface clock
24	SDI		SPI interface data input

Pin Number	Pin Name	Pin Type	Description
25	CURR8	Analog pin	LED current output
26	CURR7		LED current output
27	CURR6		LED current output
28	CURR5		LED current output
29	CURR4		LED current output
30	CURR3		LED current output
31	CURR2		LED current output
32	CURR1		LED current output
EP	VSSP		Exposed PAD. Connect to VSSP.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDDMAX	Supply voltage	-0.3	7	V	Applicable for pin VDD
VIN_5V	Maximum voltage	-0.3	VDD+0.3	V	Applicable for 5V pins(1)
VIN_30V		-0.3	30	V	Applicable for 30V pins(2)
VIN_3V2		-0.3	3.6	V	Applicable for V3_2 pin
Ilatch	Latch-up immunity	-100	+100	mA	JEDEC 78
Electrostatic Discharge					
VESD_LV	Electrostatic discharge on all 5V pins(1)	±2000		V	MIL 883 E Method 3015
VESD_HV	Electrostatic discharge on 30V pins against GND(2)	±8000		V	MIL 883 E Method 3015
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuos power dissipation		1.5	W	See note (3) for QFN32 Package
P_{DERATE}	Continuos power dissipation derating factor		33	mW / °C	See note (4)

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_J	Junction temperature		150	°C	
T_{STRG}	Storage temperature range	-55	150	°C	
T_{BODY}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor life time of 168h

Note(s):

1. Pins xRES, SDI, SCLK, SDO, xCS, VSYNC, HSYNC, xFault, FB1, FB2, V3_2, VDDI
2. Pins CURR1 – CURR16, CASC
3. Depending on actual PCB layout and PCB used
4. PDERATE derating factor changes the total continuous power dissipation (PT) if the ambient temperature is not 70°C. Therefore for e.g. T_A=85°C calculate PT at 85°C = PT - PDERATE x (85°C - 70°C)

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
General

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Rthca	Thermal resistance case – ambient	See Thermal Characteristics				°C/W
Tcase	Case temperature		-20		85	°C
T_J	Junction temperature		-20		115	°C

Figure 7:
Power Supply

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Supply voltage		4.0		5.5	V
V3_2	Voltage regulator output	I_{LOAD}=20mA	3.0	3.2	3.4	V
VDDI	Interface voltage	VDDI must not be larger than VDD	3.0	3.2	5.5	V
VDD_POR	Power on reset level		1.95		3.6	V
IDD_q	Quiescent current	VDD=5V, Default setting, PWM=0, IDAC = 100µA		12		mA
IDD_r	Supply current	VDD=5V, HSYNC=1MHz, VSYNC=480Hz, Duty=50%, IDAC = 100µA		13		mA
Icasc	Current in CASC pin				2	mA

Figure 8:
Current Outputs

Symbol	Parameter	Comments	Min	Typ	Max	Units
Vcurrx	Output voltage pins CURRx				30	V
Icurrx_High	Output current range	IDAC= 0-255, Irange500, 1LSB=0.5mA	50		177.5	mA
Icurrx_LOW		IDAC= 0-255, Irange200, 1LSB=0.2mA	20		71	mA
Rcurrx	Input resistance in CURRx	PWM=0, VCURRx>4V	10			MΩ
Iled_100_500	Trimmed Current accuracy at 25°C	Trimmed during production ILED=100mA, Temp=25°C, VDD=5V Irange500,VCURR=2V	-1		+1	%
Iled_40_200	Trimmed Current accuracy	Trimmed during production ILED=40mA, Temp=25°C, VDD=5V Irange200,VCURR=2V	-1.3		+1.3	%
Ich_100_500	Channel to channel current accuracy	ILED =100mA, Temp=25°C, VDD=5V, Irange500, VCURR=2V		0.9		%
Ich_40_200		ILED=40mA, Temp=25°C, VDD=5V, Irange200, VCURR=2V		1.1		%
Iled_500	Current accuracy at 25°	ILED= 50mA to 177.5mA, Temp=25°C, Irange500, VCURR=2V	-1.3		+1.3	%
Iled_200		ILED= 20mA to 71mA, Temp=25°C, Irange200, VCURR=2V	-1.7		+1.7	%
$I_{led\_500\_all}$ FET	Current accuracy overall	Tjunction = -20°C to 115°C ILED = 50mA to 177.5mA Irange500,VCURR=2V	-2.5		+2.5	%
$I_{led\_200\_all}$ FET	Current accuracy overall	Tjunction = -20°C to 115°C ILED = 20mA to 71mA Irange200,VCURR=2V	-2.9		+2.9	%

Figure 9:
Feedback Circuit, Fault Detectors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IFBmax	Feedback current maximum	V_{FB_X}>0.25V		255		µA
FB_IDAC_LSB	FB_IDAC LSB			1		µA
VFB	Feedback voltage trip point	See Figure 20				
Vshort	Short LED detection voltage at Pin CURRx	Programmable, tolerance ±5%		2 3 4 5 6 7 8 9 10 11 12 13		V V V V V V V V V V V V
Tovtemp	Overtemperature limit		130	140	150	°C
Thyst	Overtemperature hysteresis			10		°C

Figure 10:
PWM Generators

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Internal clock for PWM		450	500	550	kHz
fHSYNC	HSYNC frequency				10	MHz
fVSYNC	VSYNC frequency		60		480	Hz

Figure 11:
Digital Pins

Symbol	Parameter	Min	Typ	Max	Units	Note
VIH	High level input voltage	1.3		VDDI	V	See note (1)
VIL	Low level input voltage	-0.3		0.8	V	
VoH	High level output voltage	VDDI-0.3			V	I=2mA (1)
VoL	Low level output voltage			0.3	V	I=2mA (1)
VoL_PD	Low level output voltage open drain outputs			0.3	V	I=2mA (1)
R_pu	Input resistance pullup inputs		300		kΩ	
R_pd	Input resistance pulldown inputs		300		kΩ	

Note(s):

1. Pins xRES has VSS/VDD level all other digital pins have VSS/VDDI level.

Timing Characteristics

Figure 12:
SPI Timings

Symbol	Parameter	Min	Typ	Max	Units	Note
fsclk	SCLK frequency	0		10	MHz	
t1	xCS setup time	50			ns	
t2	xCS hold time	100			ns	
t3	xCS disable time	100			ns	
t4	SDI setup time	5			ns	
t5	SDI hold time	5			ns	
t6	SCLK rise time	5			ns	
t7	SCLK fall time	5			ns	
t8	SCLK low time	40			ns	
t9	SCLK high time	40			ns	
t10	Output valid from SCLK low	10			ns	

Timing Diagrams

Figure 13:
SPI Input Timing

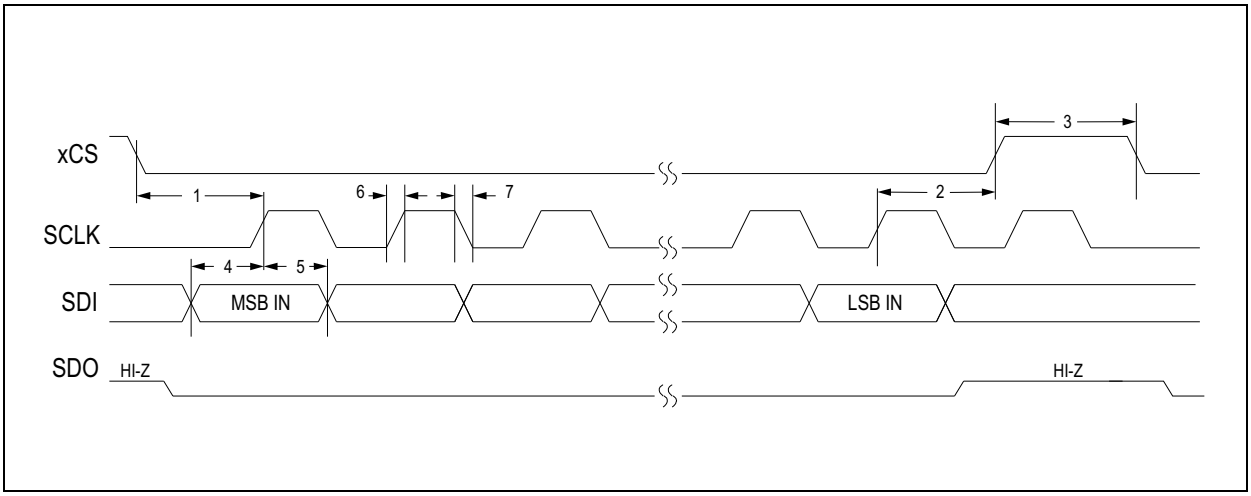
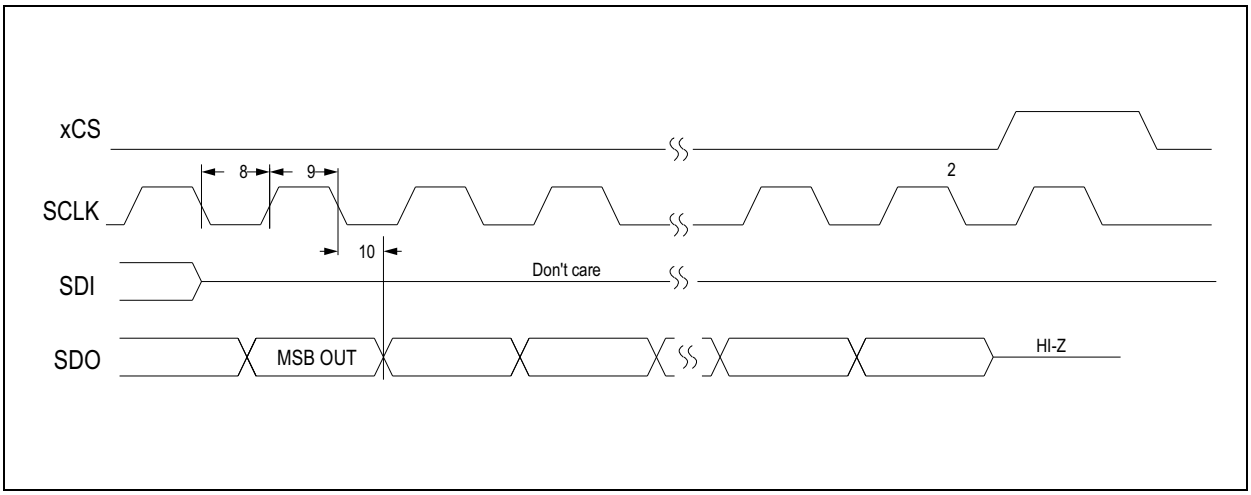
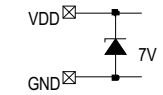
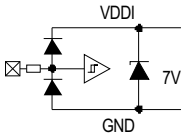
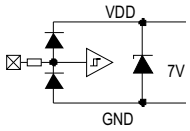
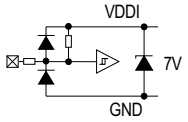
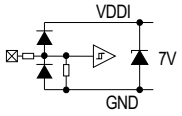
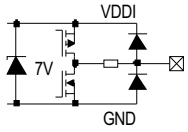
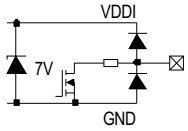


Figure 14:
SPI Output Timing



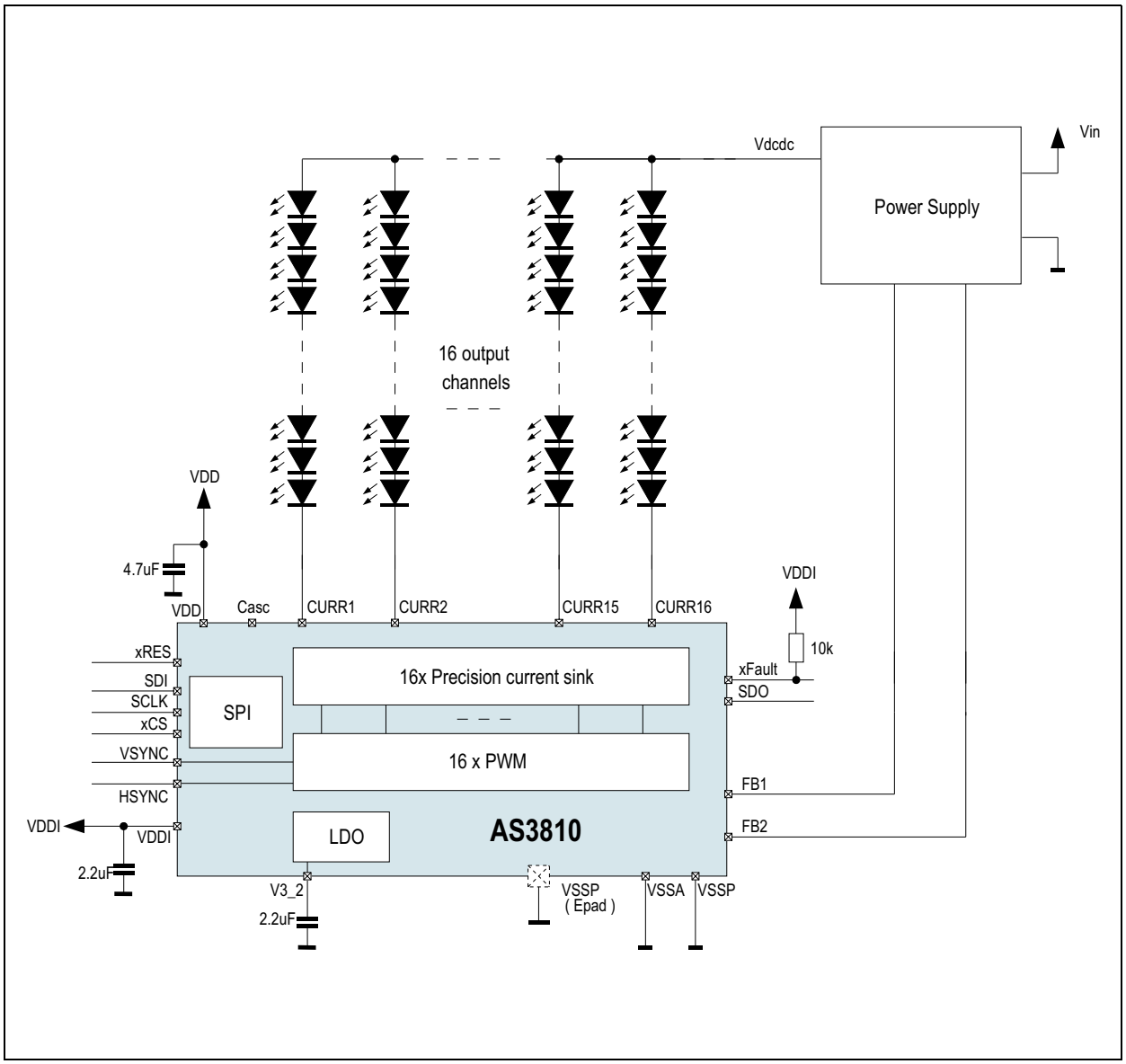
Pins Equivalent Circuit

Figure 15:
Pin Equivalent Circuits

VDD	
Digital Inputs (except xRES)	
Digital Inputs xRES	
Digital Inputs Pullup	
Digital Inputs Pulldown	
Digital Outputs Push/Pull	
Digital Output Open Drain	

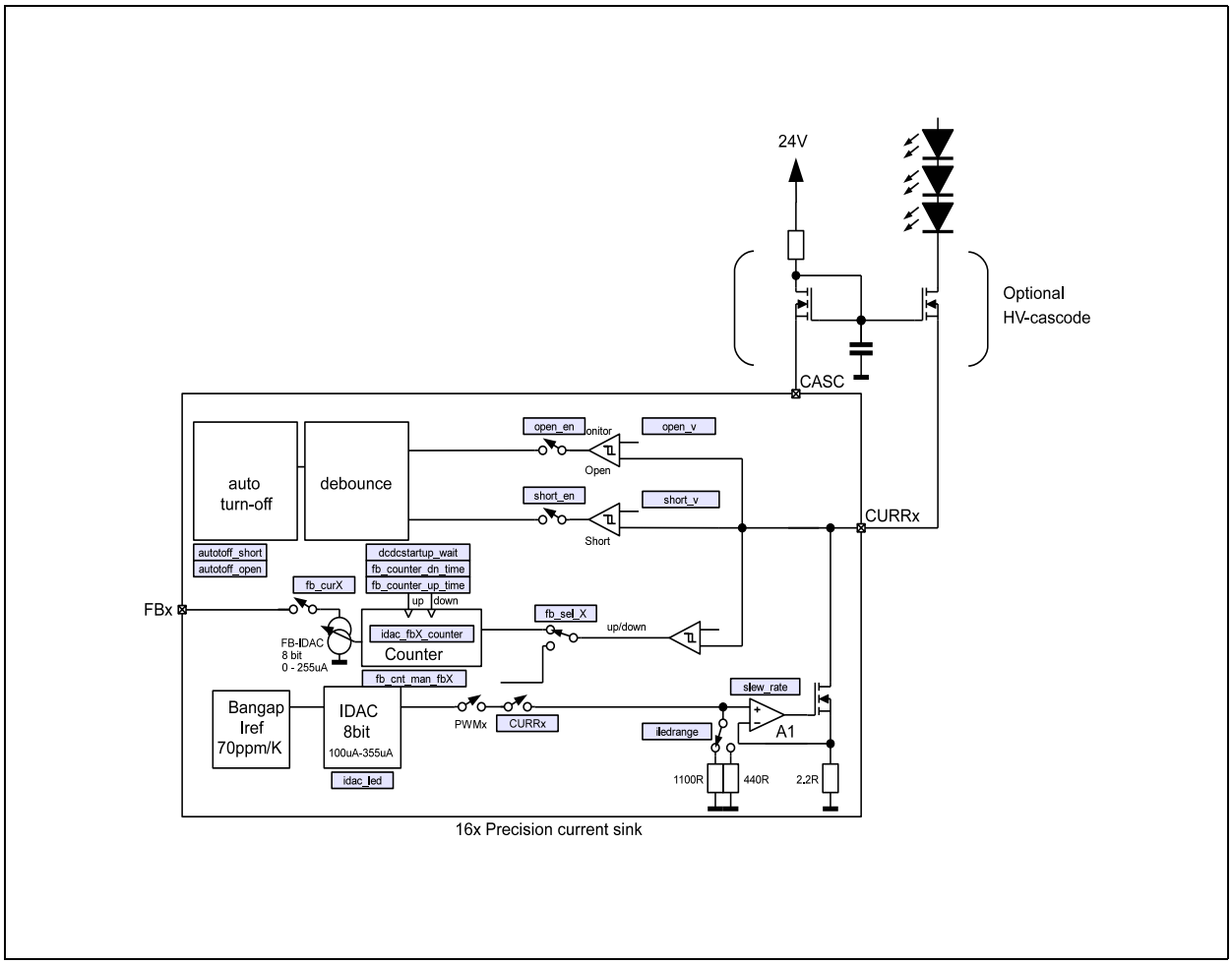
Detailed Description

Figure 16:
Typical Application Diagram



Current Outputs

Figure 17:
Precision Current Sink



Precision Current Sink

All current sinks are built with an internal error amplifier A1 and an internal power transistor. For low EMI radiation the slew rate (3* τ) of the amplifier output voltage can be adjusted between 1µs and 9µs.

Power Supply Feedback

The voltage on the pins “CURRx” is monitored to adjust the power supply output. If this voltage is lower than the internal Vtrip voltage a comparator enables counting up of the “idac_fbX_counter” with 32µs clock speed. This increases the output current of the FB-IDAC and so the output voltage of the external power supply can be increased via pin FB1 or pin FB2. The feedback function of every CURRx can be assigned to either FB1 or FB2. The power supply feedback can be turned off for every current channel separately.

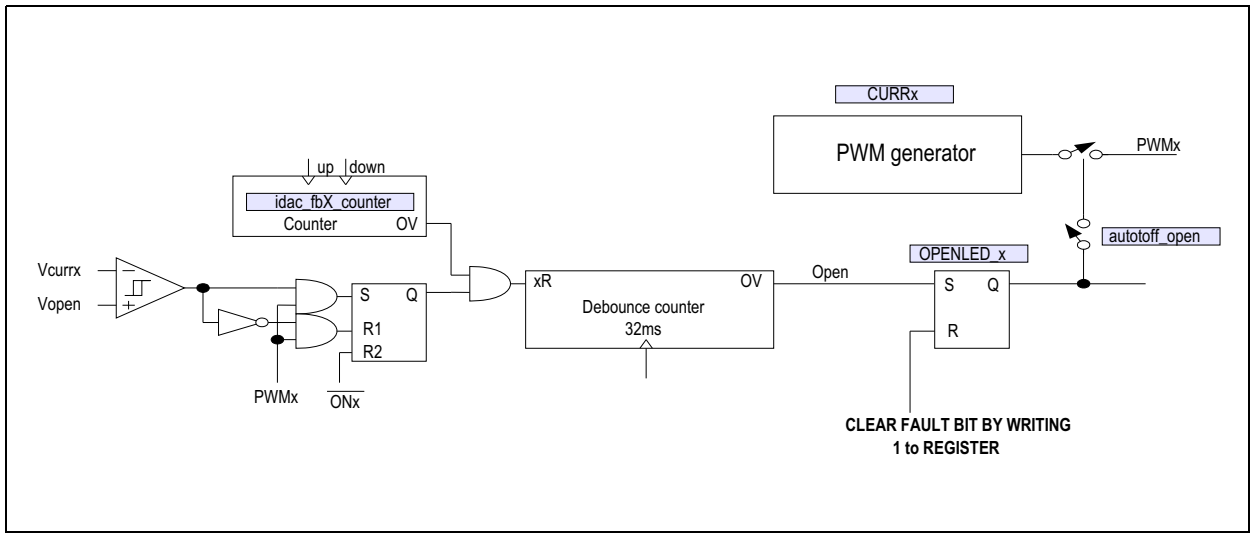
Manual Control of External Power Supply

The counter value “idac_fbX_counter” can also be preset by software if “fbcounter_man_fx” =1. This enables software control of the external power supply output voltage.

Open LED Detection

If open led detection is enabled a broken LED-string is detected during PWM=1. If a LED-string is broken and the feedback function is enabled, the “idac_fbx_counter” will count up in order to increase the power supply output voltage. After the “idac_fbx_counter” has reached its maximum the corresponding “OPENLED_x” bit is set after additional 32ms debounce.

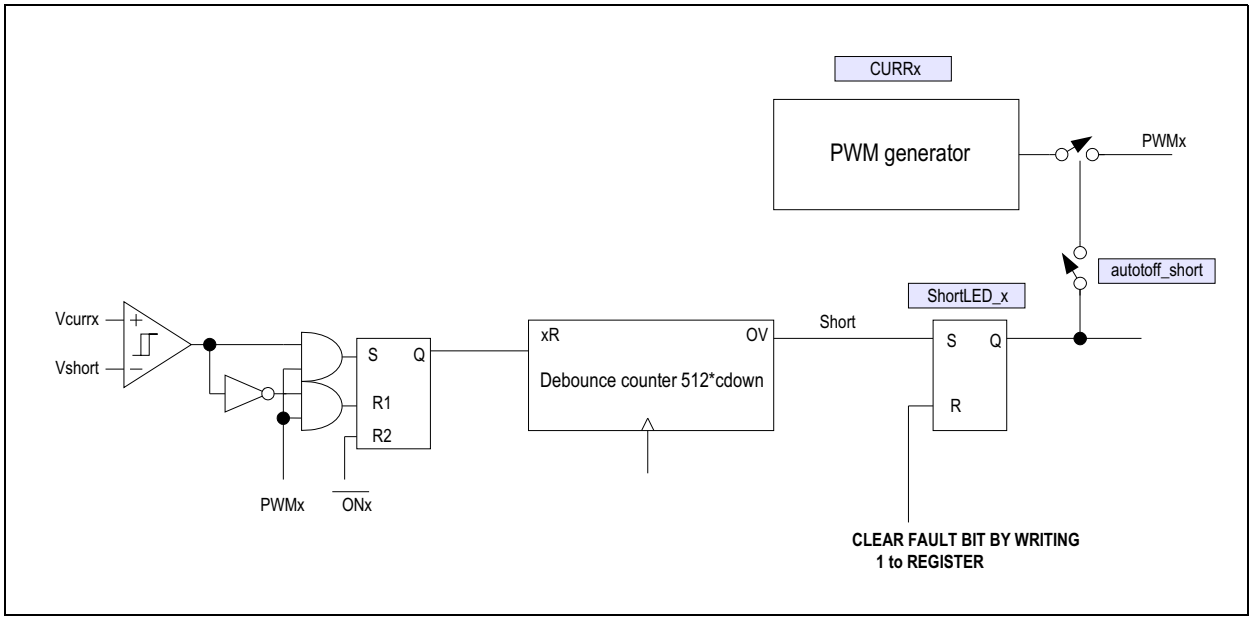
Figure 18:
Open LED Detection



Short LED Detection

If short LED detection is enabled a shorted LEDs are detected during PWM=1. The corresponding “SHORTLED_x” bit is set after 512*DownClock debounce.

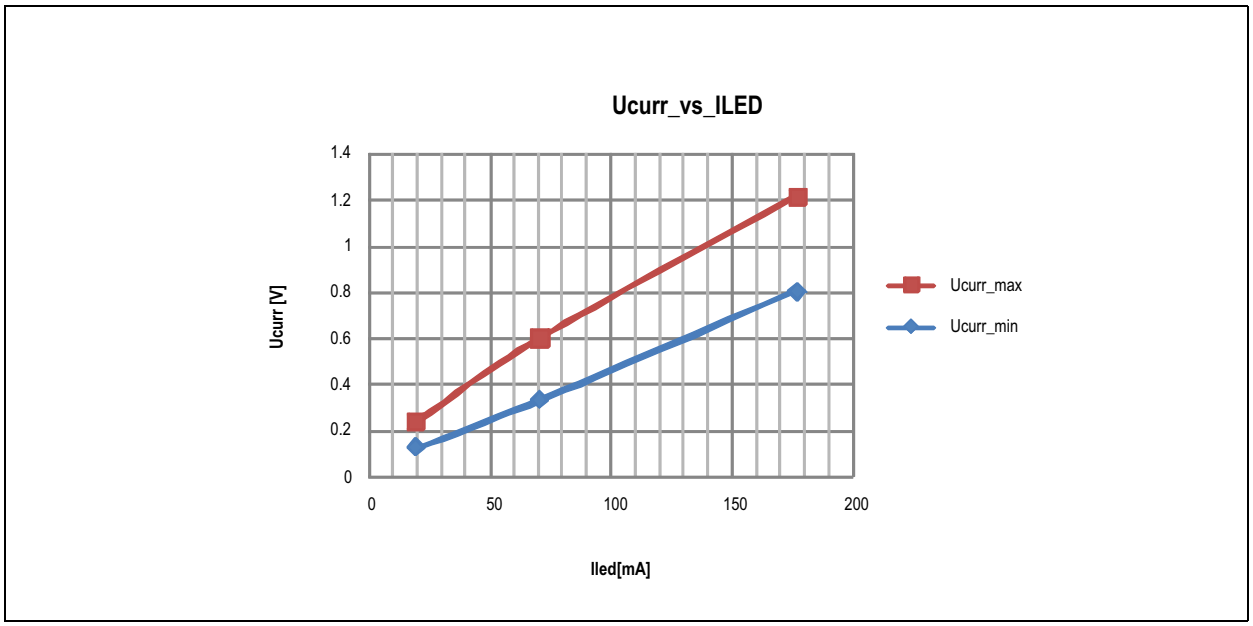
Figure 19:
Short COMP Block Diagram



Vcurr Trip Voltage

The minimum required output voltage at CurrX is depending on the output current. The trip voltage for the DC-DC feedback is adjusted according to the output current ILED.

Figure 20:
Output Voltage vs. Output Current



IDAC

The 8-bit IDAC is biased by a temperature compensated bias current and its output current is set with "idac_led" from 100µA to 355µA. The step size is 1µA. Depending on the "iledrange" the output current is multiplied by 500 or 200 to get the required ILED current in the range 50mA to 177.5mA (step size 0.5mA) respectively 20mA to 71mA (step size 0.2mA).

The LED output current at pin CURRx can be calculated:

Iledrange = 0: ILED = (100 + IDAC_LED) x 0.5 [mA]
(50mA – 177.5mA, ΔI = 0.5mA)

Iledrange = 1: ILED = (100 + IDAC_LED) x 0.2 [mA]
(20mA – 71.0mA, ΔI = 0.2mA)

Registers in Current Output Stage

ACCESS: R: read, W: write, AS: async set, AC: async clear, WC: write clear

Figure 21:
CUR_ON_1 Register

RegAddr: 0x01		CUR_ON_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CURR1 – CURR8	00000000	RW_AC	Enables or disables current outputs. 0: Output OFF 1: Output ON

Figure 22:
CUR_ON_2 Register

RegAddr: 0x02		CUR_ON_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CURR9 – CURR16	00000000	RW_AC	Enables or disables current outputs. 0: Output OFF 1: Output ON

Figure 23:
Fault_1 Register

RegAddr: 0x03		Fault_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Autotoff_uv	1	RW	1: Undervoltage lockout: If VDD <4V channels are turned off
6		0	R	Not used
5		0	R	Not used
4	Retrial_short	0	RW	1: Retrial short detection after autotoff_short was triggered
3	Retrial_open	0	RW	1: Retrial open detection after autotoff_open was triggered
2	Autotoff_ot	1	RW	Automatic Output turn off at overtemperature 0: Do not turn off current outputs on overtemperature 1: Turn off current outputs on overtemperature
1	Autotoff_short	0	RW	Automatic Output turn off on short LED detection 0: Do not turn off current outputs on short LED detection 1: Turn off current outputs on short LED detection
0	Autotoff_open	0	RW	Automatic Output turn off on open LED detection 0: Do not turn off current outputs on open LED detection 1: Turn off current outputs on open LED detection

Figure 24:
Fault_2 Register

RegAddr: 0x04		Fault_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	R	Not used
6		0	R	Not used

RegAddr: 0x04		Fault_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:2	Short_volt	0000	RW	Trigger voltage for SHORT LED detection 0000: 2V 0001: 3V 0010: 4V 0011: 5V 0100: 6V 0101: 7V 0110: 8V 0111: 9V 1000: 10V 1001: 11V 1010: 12V 1011 to 1111: 13V
1	Short_en	0	RW	Enable short LED detection 0: SHORT detection OFF 1: SHORT detection ON
0	OPEN_en	0	RW	Enable open LED detection 0: OPEN detection OFF 1: OPEN detection ON

Figure 25:
CASC_EXT Register

RegAddr: 0x05		CASC_EXT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Cascbias_en	1	RW	0: Bias for external Cascode OFF 1: Bias for external Cascode ON
6		0	R	Not used
5		0	R	Not used
4		0	R	Not used

RegAddr: 0x05		CASC_EXT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	casc	0000		Cascode bias voltage 0000: Vtrip + 0.00V 0001: Vtrip + 0.25V 0010: Vtrip + 0.50V 0011: Vtrip + 0.75V 0100: Vtrip + 1.00V 0101: Vtrip + 1.25V 0110: Vtrip + 1.50V 0111: Vtrip + 1.75V 1000: Vtrip + 2.00V 1001: Vtrip + 2.25V 1010: Vtrip + 2.50V 1011: Vtrip + 2.75V 1100: Vtrip + 3.00V 1101: Vtrip + 3.25V 1110: Vtrip + 3.50V 1111: Vtrip + 3.75V

Figure 26:
FB_SEL1 Register

RegAddr: 0x06		FB_SEL1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Fb_sel_1 – Fb_sel_8	00000000	RW	Select FB-channel for current outputs 1 to 8 0: Select FB channel FB1 1: Select FB channel FB2

Figure 27:
FB_SEL2 Register

RegAddr: 0x07		FB_SEL2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Fb_sel_9 – Fb_sel_16	00000000	RW	Select FB-channel for current outputs 9 to 16 0: Select FB channel FB1 1: Select FB channel FB2

Figure 28:
CURR_CTRL Register

RegAddr: 0x08		CURR_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	R	Not used
6		0	R	Not used
5		0	R	Not used
4	Iledrange	0	RW	Set output current range 0: Mode irange500: ILED= 50mA – 177.5mA, Stepsize 0.5mA 1: Mode irange200: ILED= 20mA – 71mA, Stepsize 0.2mA
3		0	R	Not used
2		0	R	Not used
1:0	Slew_rate	00	RW	Select slew rate of output drivers 00: 3µs 01: 2µs 10: 1µs 11: 0.33µs

Figure 29:
SHORTLED_1 Register

RegAddr: 0x09		SHORTLED_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SHORTLED_1 – SHORTLED_8	00000000	AS/WC	Indicates short LED condition on outputs 1 to 8 0: No short LED detected 1: Short LED detected

Figure 30:
OPENLED_1 Register

RegAddr: 0x0B		OPENLED_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	OPENLED_1 – OPENLED_8	00000000	AS/WC	Indicates open LED condition on outputs 1 to 8 0: No open LED detected 1: Open LED detected

Figure 31:
OPENLED_2 Register

RegAddr: 0x0C		OPENLED_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	OPENLED_9 – OPENLED_16	00000000	AS/WC	Indicates open LED condition on outputs 9 to 16 0: No open LED detected 1: Open LED detected

Figure 32:
FB_ON_1 Register

RegAddr: 0x0E		FB_ON_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FB_CURR_1 – FB_CURR _8	00000000	RW	Enables or disables feedback function of output channels 0: No feedback function on CURRx 1: Function on CURRx

Figure 33:
FB_ON_2 Register

RegAddr: 0x0F		FB_ON_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FB_CURR_9 – FB_CURR _16	00000000	RW	Enables or disables feedback function of output channels 0: No feedback function on CURRx 1: Function on CURRx

Figure 34:
IDAC_LED Register

RegAddr: 0x0D		IDAC_LED		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IDAC_LED	00000000	RW	Defines LED output current 50mA to 177.5mA or 20mA to 71mA Depending on *iledrange* bit

Figure 35:
IDAC_FB1_COUNTER Register

RegAddr: 0x10		IDAC_FB1_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IDAC_FB1_ COUNTER	00000000	RW	Feedback 1 counter value. Can be overwritten if Fb_cnt_man_fb1 = 1 0x00: FB-current 0µA 0xFF: FB-current 255µA

Figure 36:
IDAC_FB2_COUNTER Register

RegAddr: 0x11		IDAC_FB2_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IDAC_FB2_ COUNTER	00000000	RW	Feedback 2 counter value. Can be overwritten if Fb_cnt_man_fb2 = 1 0x00: FB-current 0µA 0xFF: FB-current 255µA

Figure 37:
FBLOOP_CTRL Register

RegAddr: 0x12		FBLOOP_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	R	Not used
6	Fb_cnt_man_ fb2	0	RW	0: FB2 counter runs automatically in feedback loop 1: FB2 counter is set manual.
5	Fb_cnt_man_ fb1	0	RW	0: FB1 counter runs automatically in feedback loop 1: FB1 counter is set manual.
4		0	R	Not used
3:2	Fbcount_dn_ time	01	RW	FB1 and FB2 counter down counting clock cycle 00: 512µs 01: 2048µs 10: 4096µs 11: 8192µs

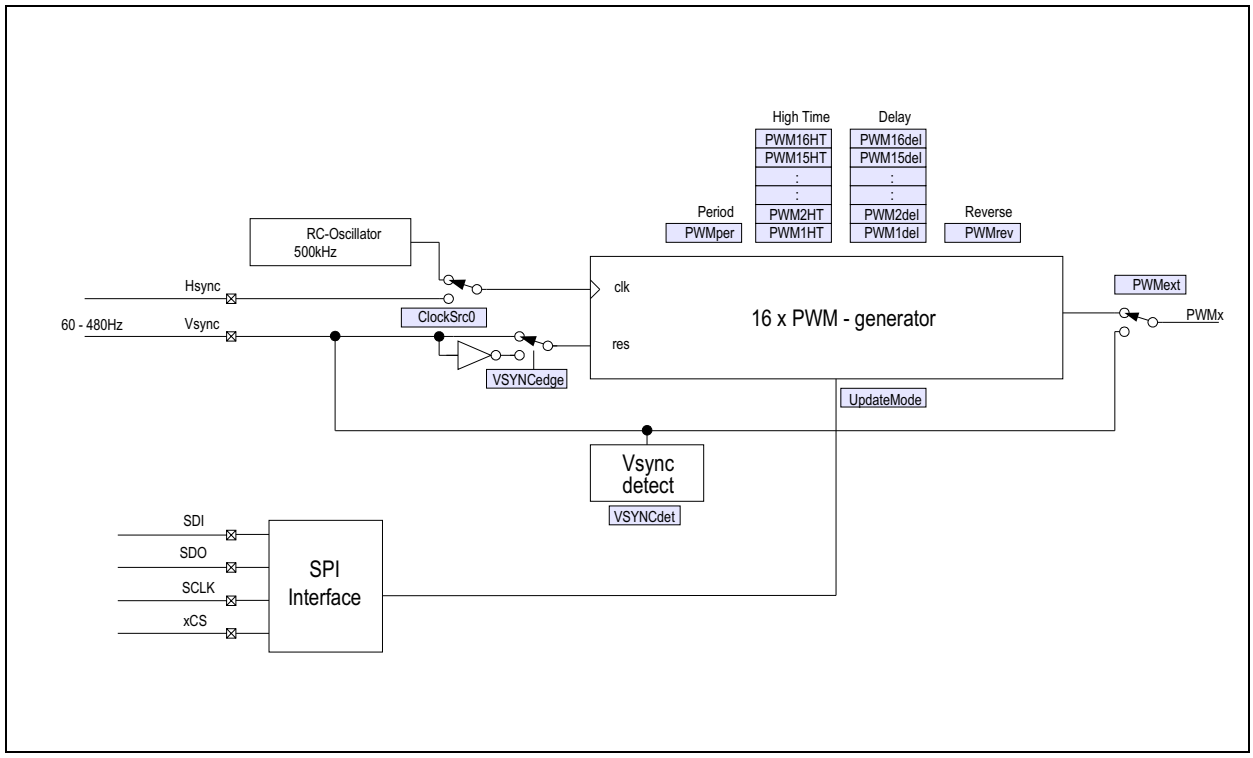
RegAddr: 0x12		FBLOOP_CTRL		
Bit	Bit Name	Default	Access	Bit Description
1:0	Fbcount_up_time	01	RW	FB1 and FB2 counter up counting clock cycle 00: 1024µs 01: 256µs 10: 64µs 11: 16µs

Figure 38:
STATUS Register

RegAddr: 0x60		STATUS		
Bit	Bit Name	Default	Access	Bit Description
7	STAT novsync	0	R	1: Indicates missing Vsync signal for longer than 100ms
6	STAT OT	0	R	1: Indicates overtemperature fault happened
5	STAT Open	0	R	1: Indicates open detection fault happened
4	STAT Short	0	R	1: Indicates short detection fault happened
3		0	R	Not used
2	STATuvlockout	0	R	1: Indicates under voltage lockout
1:0	Power_good	00	R	Indicates power status of the device 00: No power supply 01: Power rising up 10: Power good 11: Not used

PWM Generators

Figure 39:
PWM Generators



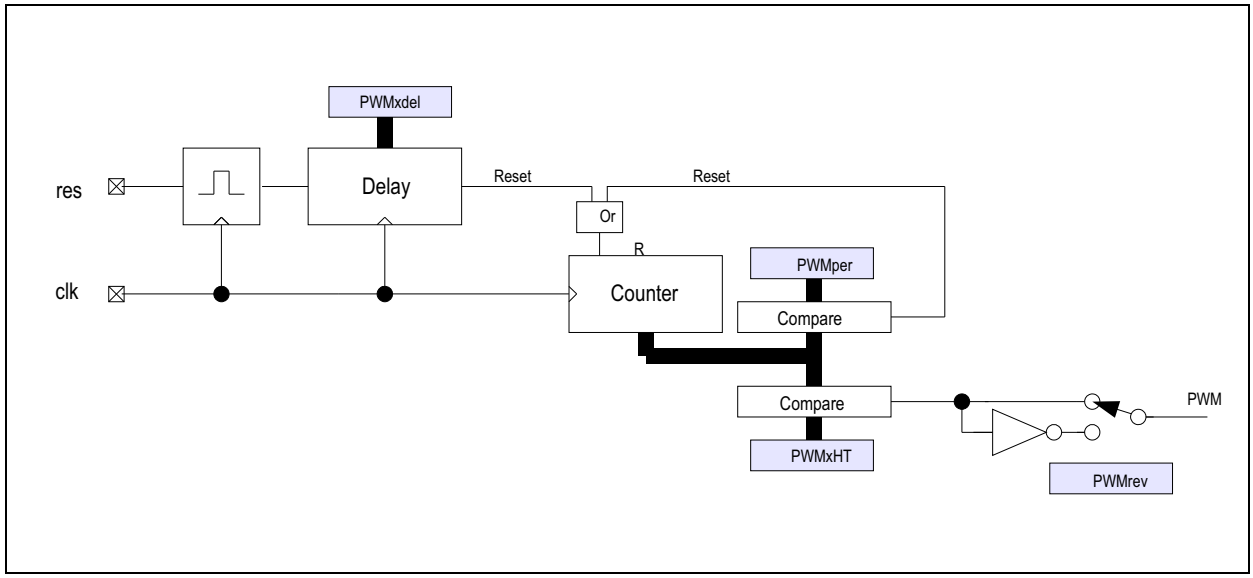
Clock and Reset

The clock for the built-in PWM generators can be one of three different sources listed below:

1. Internal RC oscillator with 500KHz
2. External Clock signal. This is usually the HSYNC signal of the TV.

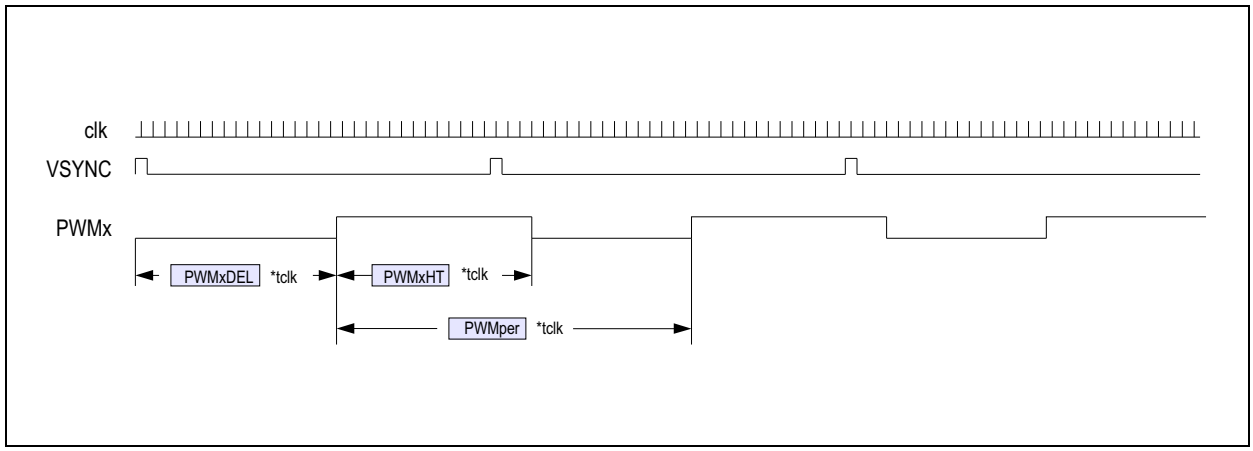
PWM Counter

Figure 40:
PWM Counter



Each PWM-generator is built with a 12-bit counter and digital comparators. The counter is counting up with tclk until the value stored in “PWMper” is reached. This resets the counter and starts the next period. While the counter value is below “PWMxHT” the PWM-signal is “1”, the rest of the period the PWM-signal is “0”. The output of each PWM-generator can also be inverted by means of the “PWMrev”.

Figure 41:

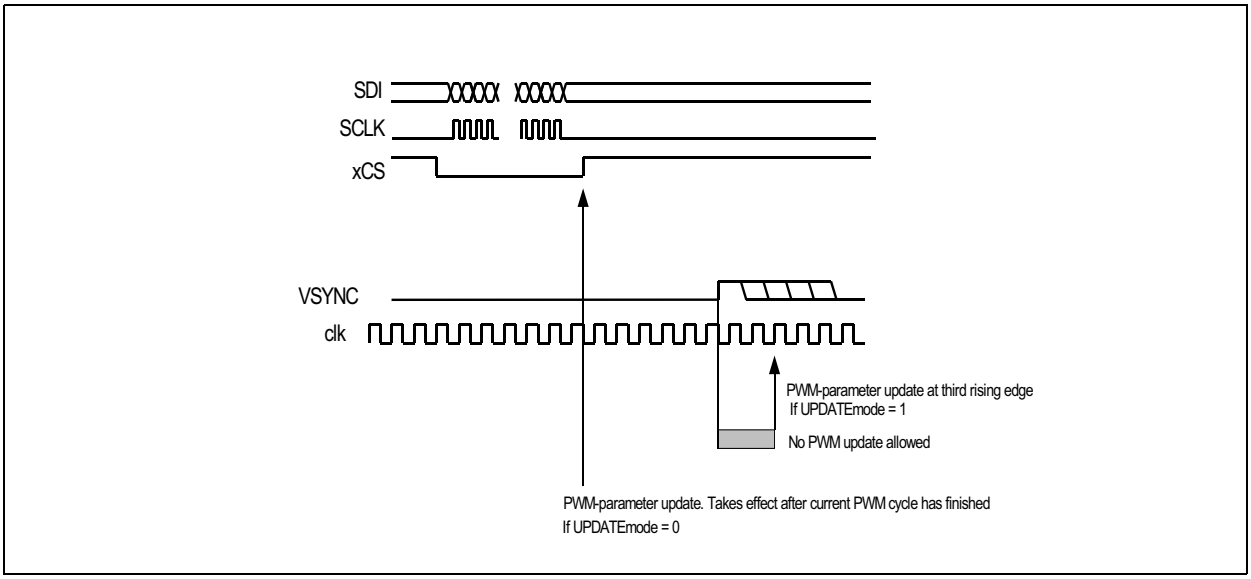


SPI Data Update, UPDATEmode Bit

The PWM-settings that are programmed via the SPI-Interface take effect depending on the status of the “UPDATEmode”-bit. If UPDATEmode =1 new data from the serial interface are stored at the next rising edge of VSYNC.

If UPDATEmode =0 new data from the serial interface are stored immediately after xCS goes high and will take effect after current PWM cycle is finished. In this mode the values in the PWMxdel registers are ignored. There will be no Delay on the PWM signals.

Figure 42:
UPDATEmode



The PWMxHT-values are double buffered. HighTime values for the next VSYNC can be written even when the current HighTime is not finished.

Direct PWM Mode

The internal signals PWMx can also be direct applied at the VSYNC input if the bit Direct_PWM =1.

In this mode the default driver has the following configuration:

- All current outputs are ON
- All feedback controls are enabled. CURR1-CURR8 are connected to FB1,CURR9-CURR16 are connected to FB2
- Short and open LED detection are enabled
- Short LED detection voltage = 9V
- Short and open LED detection auto turn off function is enabled
- Short and open LED detection retrial function is enabled
- Undervoltage lockout and overtemperature detection are enabled

- LED current = 20mA to 69.6mA set by factory trimming (resolution 1.6mA) or 50mA to 174mA set by factory trimming (resolution 4mA)

VSYNC Detect

The VSYNCdet=1 the VSYNC detector monitors the presence of a VSYNC signal. If the VSYNC signal is missing for more than 100ms current outputs are temporary turned off.

VSYNC Duration

Since the VSYNC input is connected to an edge detector, there is no restriction on the duration of the VSYNC pulse.

Registers in PWM Generators

Figure 43:
PWM_CTRL Register

RegAddr: 0x13		PWM_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0	R	Not used
6		0	R	Not used
5	Pwm_rev	0	RW	0: Normal PWM operation 1: PWM signals are inverted
4	VSYNCdet	0	RW_AS	Enable VSYNC detection 0: VSYNC-detection OFF 1: VSYNC-detection ON. All current outputs are turned off if VSYNC signal is missing for 100ms
3	VSYNCedge	0	RW	Defines VSYNC trigger edge 0: VSYNC trigger on rising edge 1: VSYNC trigger on falling edge
2	Direct_PWM	0	RW_AS	Select external or internal PWM signal 0: PWM signal is generated internally 1: PWM signal is applied externally at pin VSYNC Factory trim bit is read during startup. See section Direct PWM Mode
1	Update_Mode	0	RW	Defines when internal registers are updated 0: Registers updated with rising edge of xCS 1: Registers updated with next VSYNC-edge
0	Clock_Src	0	RW	Clock source for internal PWM-generators 0: Internal RC oscillator 1: External Pin HSYNC

Figure 44:
PWMperiod Register

RegAddr: 0x15	RegAddr: 0x14	PWMperiod		
Bit	Bit	Default	Access	Bit Description
4:0	7:0	0x00, 0x00	RW	PWMper[12:0] sets PWM period

Figure 45:
PWM1delay Register

RegAddr: 0x17	RegAddr: 0x16	PWM1delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM1del[11:0] sets PWM1 delay

Figure 46:
PWM2delay Register

RegAddr: 0x19	RegAddr: 0x18	PWM2delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM2del[11:0] sets PWM2 delay

Figure 47:
PWM3delay Register

RegAddr: 0x1B	RegAddr: 0x1A	PWM3delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM3del[11:0] sets PWM3 delay

Figure 48:
PWM4delay Register

RegAddr: 0x1D	RegAddr: 0x1C	PWM4delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM4del[11:0] sets PWM4 delay

Figure 49:
PWM5delay Register

RegAddr: 0x1F	RegAddr: 0x1E	PWM5delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM5del[11:0] sets PWM5 delay

Figure 50:
PWM6delay Register

RegAddr: 0x21	RegAddr: 0x20	PWM6delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM6del[11:0] sets PWM6 delay

Figure 51:
PWM7delay Register

RegAddr: 0x23	RegAddr: 0x22	PWM7delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM7del[11:0] sets PWM7 delay

Figure 52:
PWM8delay Register

RegAddr: 0x25	RegAddr: 0x24	PWM8delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM8del[11:0] sets PWM8 delay

Figure 53:
PWM9delay Register

RegAddr: 0x27	RegAddr: 0x26	PWM9delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM9del[11:0] sets PWM9 delay

Figure 54:
PWM10delay Register

RegAddr: 0x29	RegAddr: 0x28	PWM10delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM10del[11:0] sets PWM10 delay

Figure 55:
PWM11delay Register

RegAddr: 0x2B	RegAddr: 0x2A	PWM11delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM11del[11:0] sets PWM11 delay

Figure 56:
PWM12delay Register

RegAddr: 0x2D	RegAddr: 0x2C	PWM12delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM12del[11:0] sets PWM12 delay

Figure 57:
PWM13delay Register

RegAddr: 0x2F	RegAddr: 0x2E	PWM13delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM13del[11:0] sets PWM13 delay

Figure 58:
PWM14delay Register

RegAddr: 0x31	RegAddr: 0x30	PWM14delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM14del[11:0] sets PWM14 delay

Figure 59:
PWM15delay Register

RegAddr: 0x33	RegAddr: 0x32	PWM15delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM15del[11:0] sets PWM15 delay

Figure 60:
PWM16delay Register

RegAddr: 0x35	RegAddr: 0x34	PWM16delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM16del[11:0] sets PWM16 delay

Figure 61:
LOCKUNLOCK Register

RegAddr: 0x36		LOCKUNLOCK		
Bit	Bit Name	Default	Access	Bit Description
7:0	LOCKUNLOCK	0x00	RW	MagicByte to lock and unlock writing and reading of registers Writing into register: 0xCX: Unlock register Group1. Writing enabled 0xXA: Unlock register Group2. Writing enabled 0xCA: Unlock register Group1 and Group2. Writing enabled 0xAX: Lock register Group1. Writing disabled 0xXC: Lock register Group2. Writing disabled 0xAC: Lock register Group1 and Group2. Writing disabled X: Do not care. All other values do not change the status of LOCKUNLOCK. Reading from register: 0x00: Group1 and Group2 are locked 0x01: Group1 is unlocked 0x02: Group2 is unlocked 0x03: Group1 and Group2 are unlocked

Figure 62:
PWM1hightime Register

RegAddr: 0x38	RegAddr: 0x37	PWM1hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM1HT[11:0] sets PWM1 high time

Figure 63:
PWM2hightime Register

RegAddr: 0x3A	RegAddr: 0x39	PWM2hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM2HT[11:0] sets PWM2 high time

Figure 64:
PWM3hightime Register

RegAddr: 0x3C	RegAddr: 0x3B	PWM3hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM3HT[11:0] sets PWM3 high time

Figure 65:
PWM4hightime Register

RegAddr: 0x3E	RegAddr: 0x3D	PWM4hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM4HT[11:0] sets PWM4 high time

Figure 66:
PWM5hightime Register

RegAddr: 0x40	RegAddr: 0x3F	PWM5hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM5HT[11:0] sets PWM5 high time

Figure 67:
PWM6hightime Register

RegAddr: 0x42	RegAddr: 0x41	PWM6hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM6HT[11:0] sets PWM6 high time

Figure 68:
PWM7hightime Register

RegAddr: 0x44	RegAddr: 0x43	PWM7hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM7HT[11:0] sets PWM7 high time

Figure 69:
PWM8hightime Register

RegAddr: 0x46	RegAddr: 0x45	PWM8hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM8HT[11:0] sets PWM8 high time

Figure 70:
PWM9hightime Register

RegAddr: 0x48	RegAddr: 0x47	PWM9hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM9HT[11:0] sets PWM9 high time

Figure 71:
PWM10hightime Register

RegAddr: 0x4A	RegAddr: 0x49	PWM10hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM10HT[11:0] sets PWM10 high time

Figure 72:
PWM11hightime Register

RegAddr: 0x4C	RegAddr: 0x4B	PWM11hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM11HT[11:0] sets PWM11 high time

Figure 73:
PWM12hightime Register

RegAddr: 0x4E	RegAddr: 0x4D	PWM12hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM12HT[11:0] sets PWM12 high time

Figure 74:
PWM13hightime Register

RegAddr: 0x50	RegAddr: 0x4F	PWM13hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM13HT[11:0] sets PWM13 high time

Figure 75:
PWM14hightime Register

RegAddr: 0x52	RegAddr: 0x51	PWM14hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM14HT[11:0] sets PWM14 high time

Figure 76:
PWM15hightime Register

RegAddr: 0x54	RegAddr: 0x53	PWM15hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM15HT[11:0] sets PWM15 high time

Figure 77:
PWM16hightime Register

RegAddr: 0x56	RegAddr: 0x55	PWM16hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM16HT[11:0] sets PWM16 high time

PWM Examples

Figure 78:
PWM Example 1

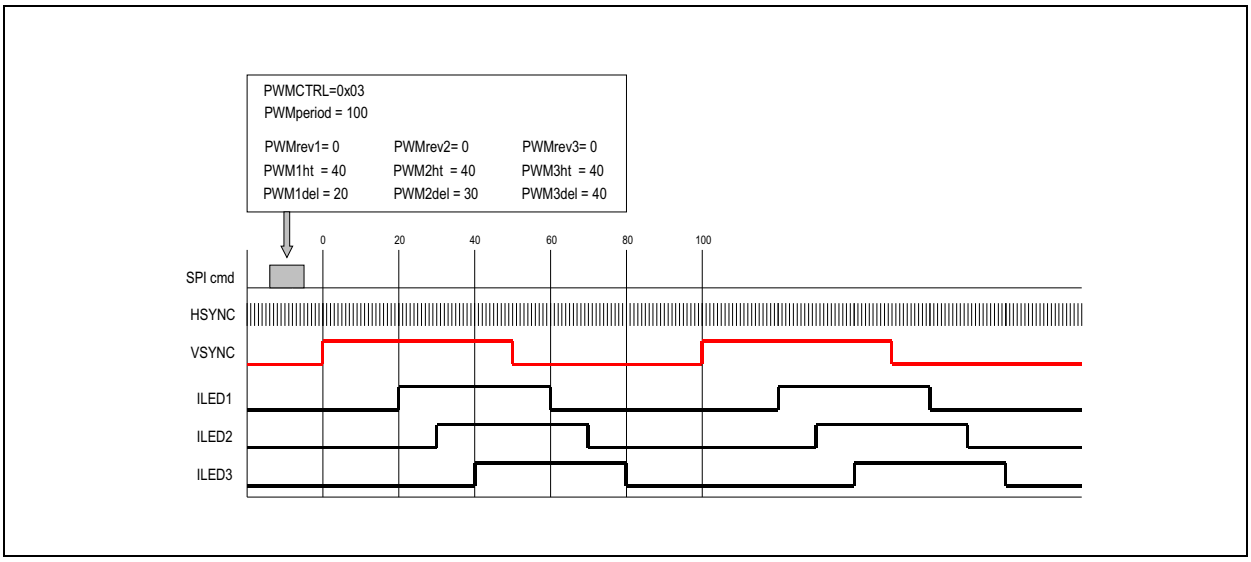


Figure 79:
PWM Example 2

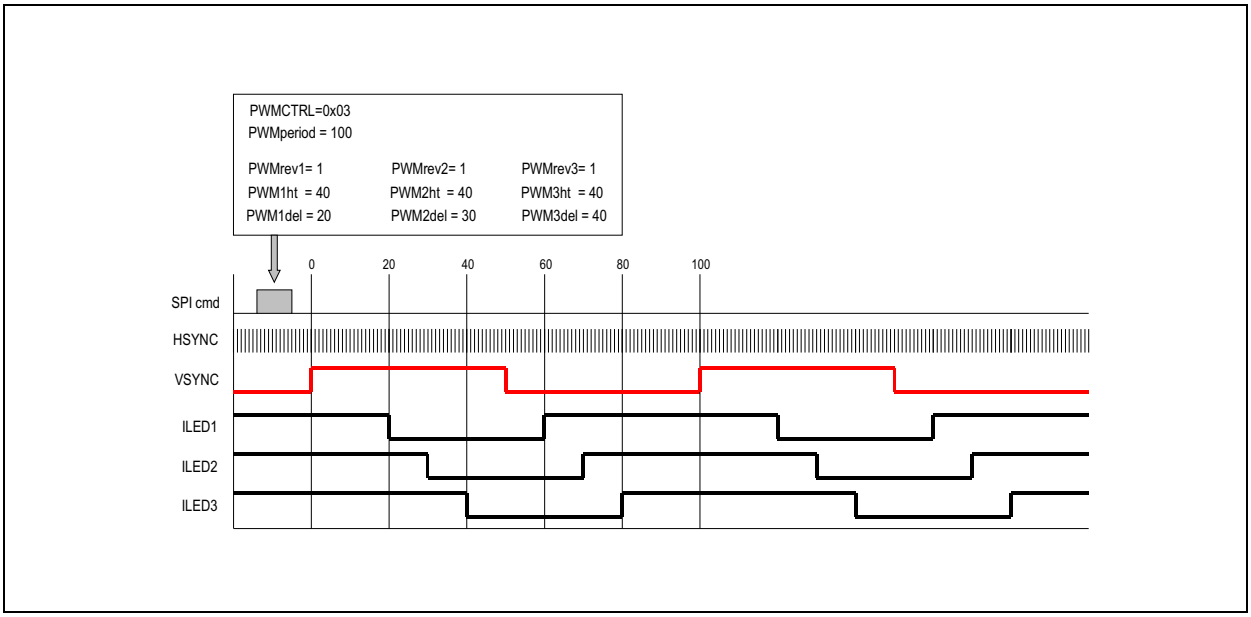


Figure 80:
PWM Example 3

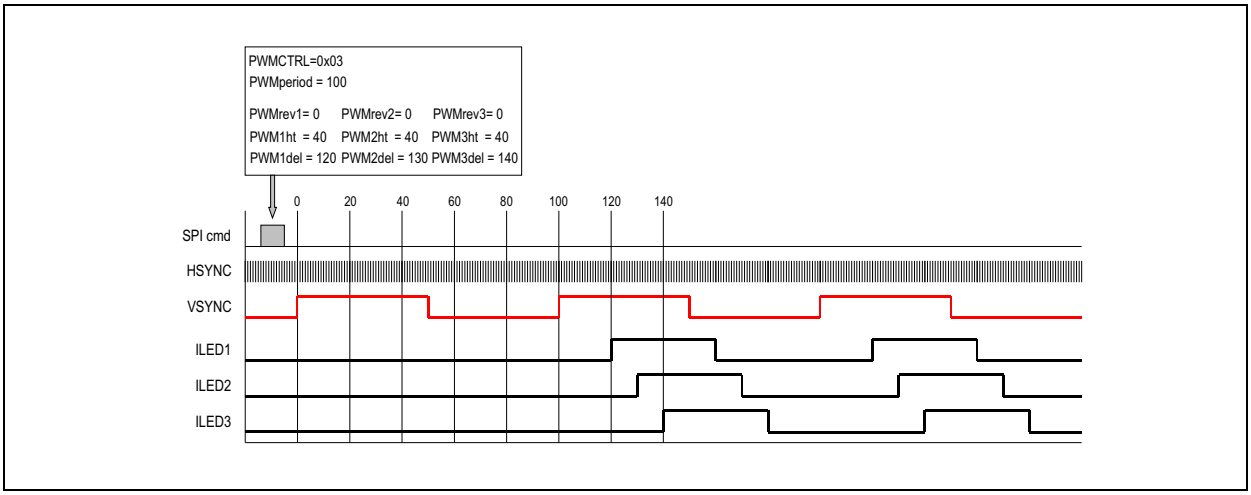


Figure 81:
PWM Example 4

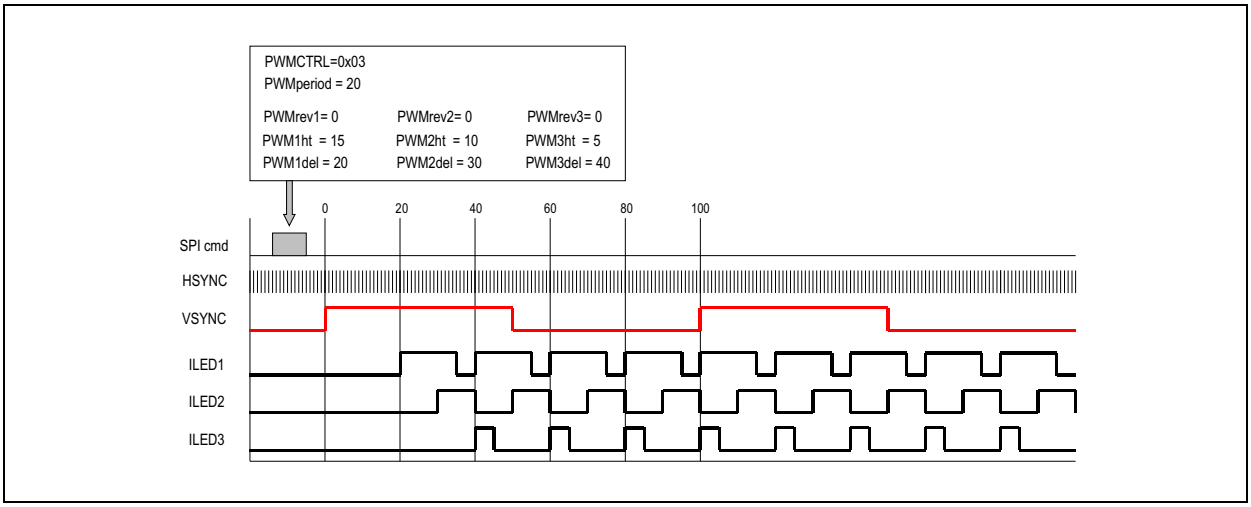
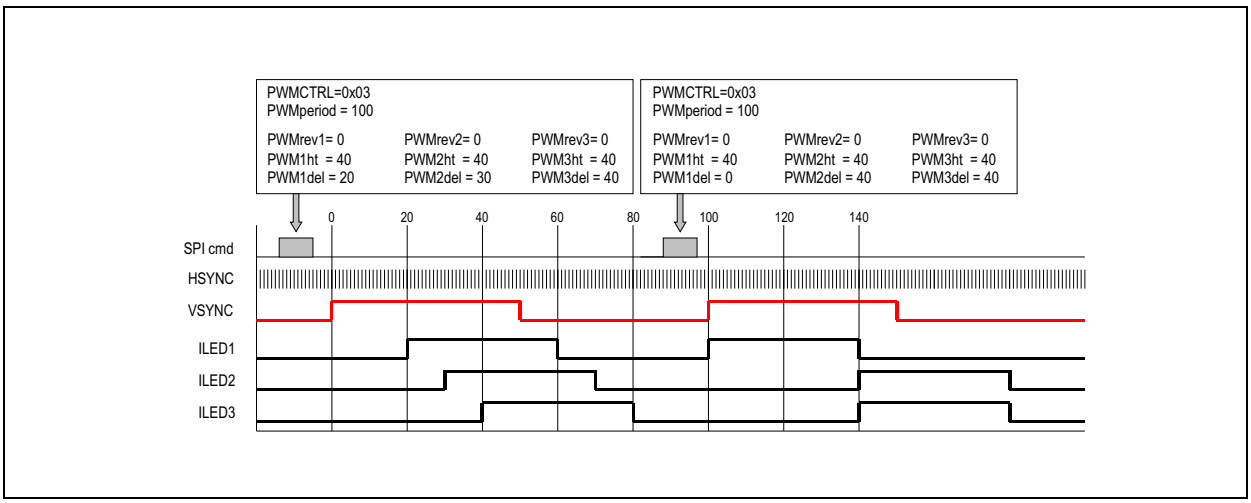


Figure 82:
PWM Example 5



Power Supply

Voltage Regulator V3_2

A built-in linear voltage regulator provides 3.2V supply voltage for external devices at pin V3_2. A 2.2uF blocking capacitor should be connected to pin V3_2.

Shunt Regulator CASC

A built-in shunt regulator is provided at pin CASC. The voltage of this electronic Zener-diode can be programmed to be 0V to 3.75V higher than the internal trip voltage Vtrip.

Interface Power Supply VDDI

Pin VDDI supplies all digital inputs/outputs. This enables connecting the device to different logic levels.

Safety Features

Temperature Shutdown

If OTturnoff = 1 the outputs of the device are turned off when the die temperature reaches 140°C. If the die temperature goes below 130°C the outputs are turned on again.

xRES Input

In addition to the built-in power on reset circuit there is an external reset input “xRES” available. This gives the possibility to keep the outputs turned off until all blocks of the LED-driver circuits are fully working (DC-DC, MCU...).

Register Lock / Unlock

To prevent wrong writing to registers due to noise on the serial interface a lock/unlock mechanism is implemented.

Registers 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x0E, 0x0F, 0x10, 0x11, 0x12, 0x13 belong to Group1 and can only be written if:

Group1 is unlocked by the “LOCKUNLOCK”-byte (Reg: 0x36)

Registers 0x0D, 0x14, 0x15 belong to Group2 and can only be written if Group2 is unlocked by the “LOCKUNLOCK”-byte (Reg: 0x36).

The default value of the Groups is locked.

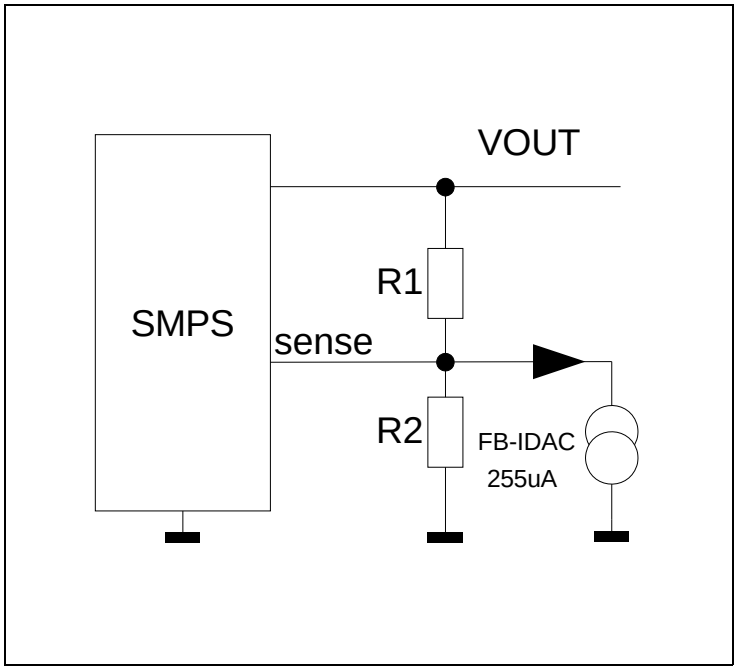
Dynamic Feedback Control

The output of pins “FB1” and “FB2” can be used to control any external power supply for best power efficiency.

Every power supply senses its output voltage with a resistive voltage divider. This voltage divider can be modified to set the output voltage between a minimum output voltage VMIN and a maximum output voltage VMAX. The design of the dynamic feedback control is done in 2 steps.

Step 1: Calculate resistors R1 in order to achieve the desired voltage range (VMAX – VMIN) with 255µA maximum current DAC output.

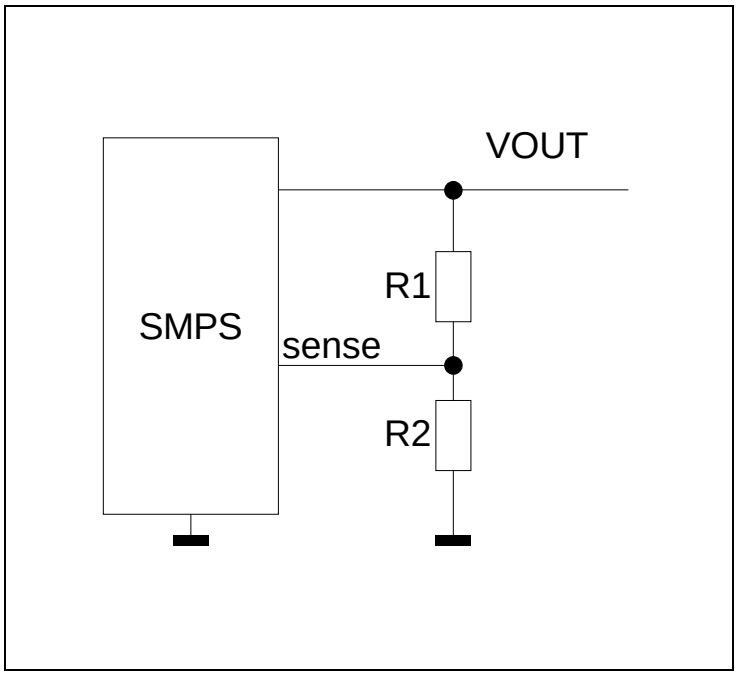
Figure 83:
Step 1



$$R1 = \frac{Vout_{MAX} - Vout_{MIN}}{255\mu A} \quad \text{(EQ1)}$$

Step 2: Calculate resistor R2 for minimum output voltage with 0µA minimum current DAC output.

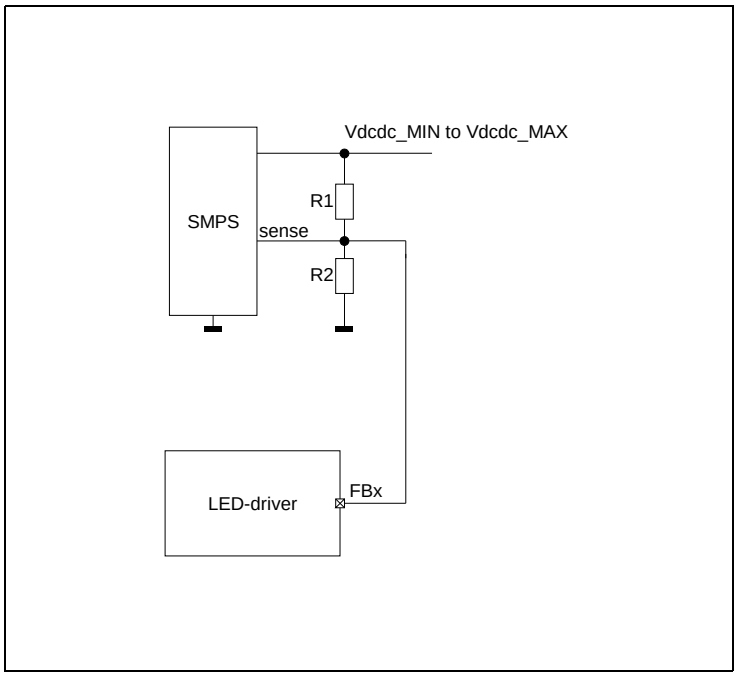
Figure 84:
Step 2



(EQ2)
$$R2 = \frac{R1}{\left(\frac{Vout_{MIN}}{V_{sense}} - 1\right)}$$

The output voltage VOUT can also be adjusted manually by writing the "*idac_FBx_counter*" value ("FB_cnt_man_fbx"=1). In this case the output voltage can be calculated as follows:

Figure 85:
Step 3



(EQ3) $VOUT = \left(1 + \frac{R1}{R2}\right) x\ V_{sense} + R1\ x\ \text{“idac\_fbx\_counter”}\ x\ 1\mu A$

Example: Voutmin = 60V, Voutmax = 80V, Vsense = 1.25V

(EQ4) $$R1 = \frac{(Vout_{MAX} - Vout_{MIN})}{255\mu A} = \frac{(80V - 60V)}{255\mu A} = 78k\Omega$$

(EQ5) $$R2 = \frac{R1}{\left(\frac{Vout_{MIN}}{V_{sense}} - 1\right)} = \frac{78k\Omega}{\left(\frac{60V}{1.25V} - 1\right)} = 1.66k\Omega$$

Application Information

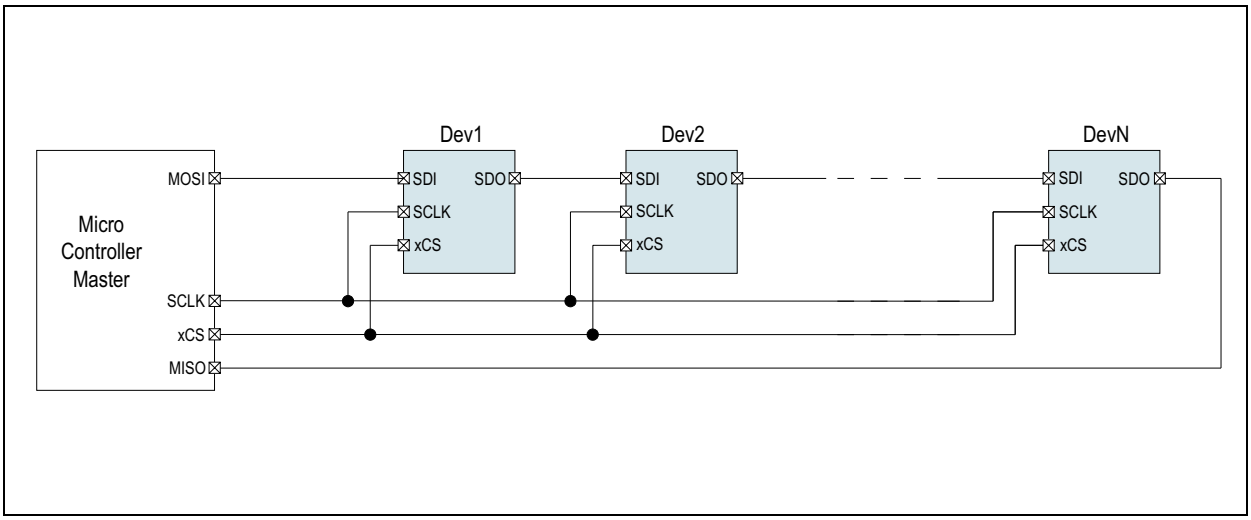
SPI Interface

For the data transfer a serial peripheral interface (SPI) is used. The SPI is configured to work only as SPI slave. If more than one driver is connected to a SPI master, they can be connected in a “Daisy Chain”-structure or a parallel structure.

SPI Daisy Chain Structure

All SPI slaves share the same clock (SCLK) and chip select (xCS) signal. In that configuration all devices can be treated as one big shift register. The devices are automatically enumerated as described in the next section.

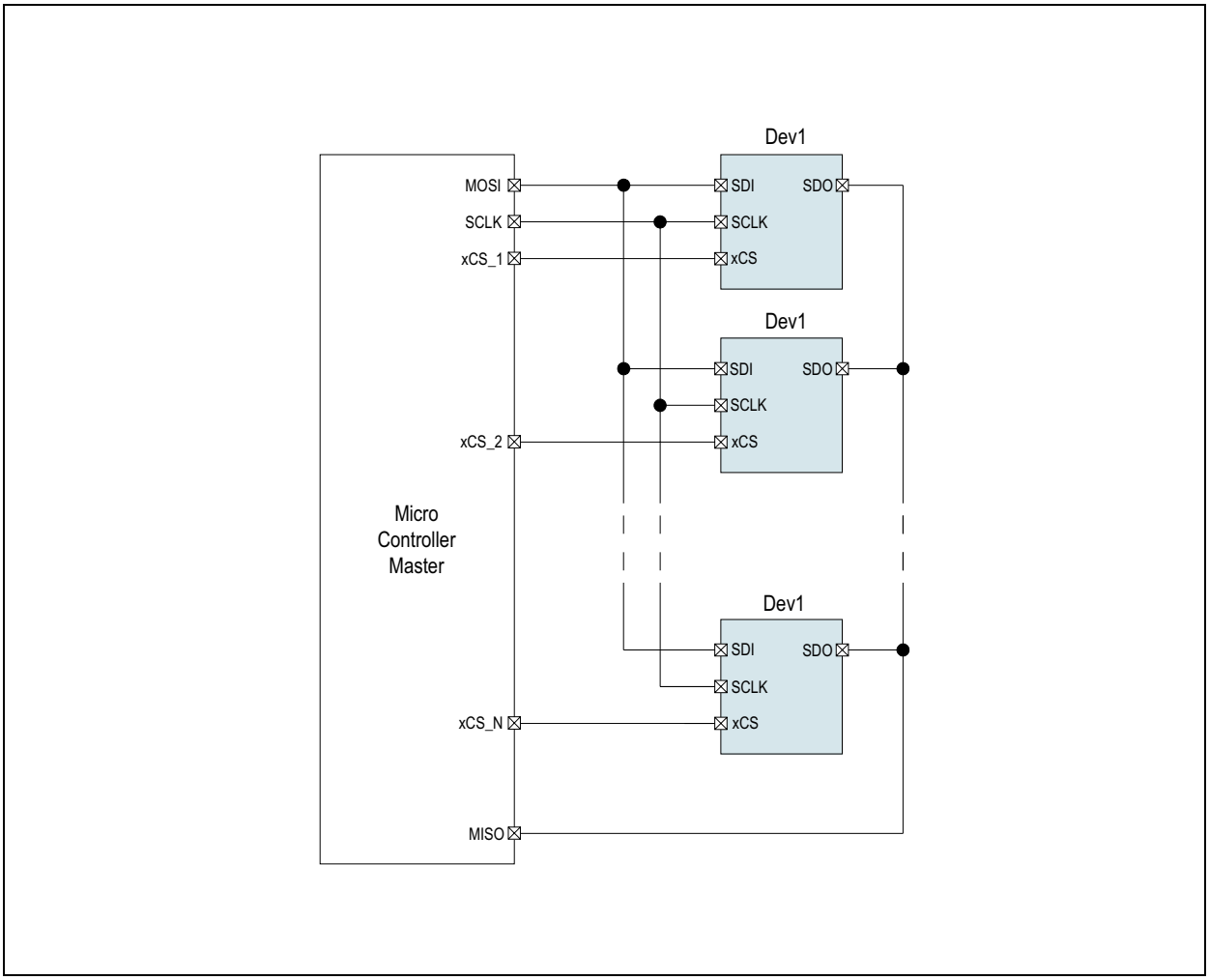
Figure 86:
SPI Daisy Chain Structure



SPI Parallel Structure

All SPI slaves share the same input (SDI) output (SDO) and clock (SCLK) signal. Every single device can be addressed via the chip select (xCS) signal. In this configuration every device has DevAddr = 0x01.

Figure 87:
SPI Parallel Structure



SPI Device Address Enumeration

The device address of each driver is automatically set by the position of the device in the chain.

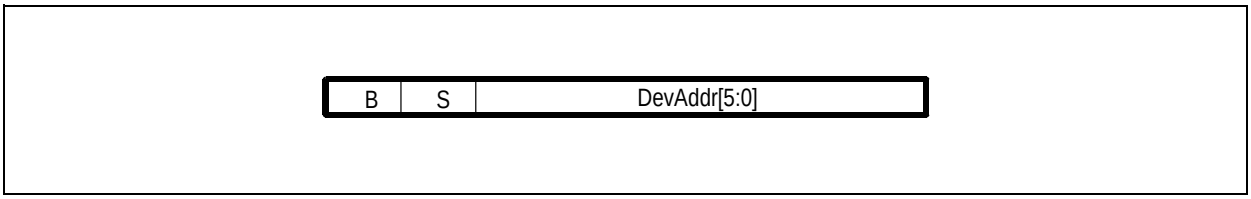
The first device has DevAddr = 0x01, the second device has DevAddr = 0x02 and so on. Device Addresses 0x00 and 0x3F are used for special broadcast writing commands described below.

SPI Protocol

Data Types

When xCS=0 all slaves will be activated. The addressing and data section is organized in byte packages. Each message can be built with the following Bytes:

Figure 88:
Device Address

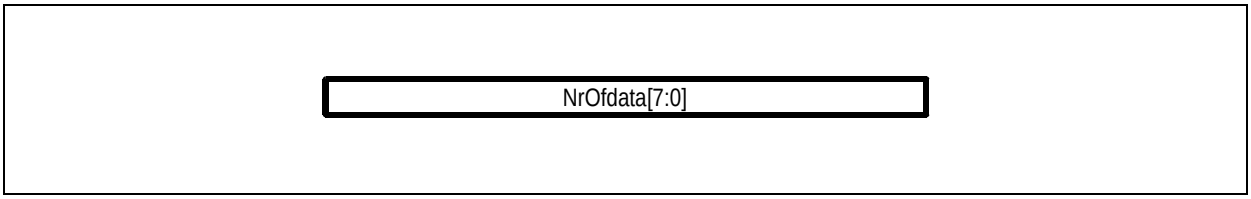


Addresses a specific driver and defines protocol information

Figure 89:
Device Address Description

Bit	Meaning	Value
B	Broadcast	B=1: Broadcast message to all devices B=0: Normal message to one single device
S	Singlebyte	S=0: Block data read or write S=1: Single data transmission (only one byte)
DevAddr[5:0]	Device Address	0x00 Write same data to same register of all devices (B=1) 0x01 to 0x3E. Device addresses for device 1 to 62 0x3F Write different data to same register of all devices (B=1)

Figure 90:
Nr_of_data



Defines the number of data bytes in the data frame if S=0

Figure 91:
Nr_of_data Description

Bit	Meaning	Value
NrOfdata[7:0]	Number of data bytes in frame	0x00 to 0xFF

Figure 92:
Register_address

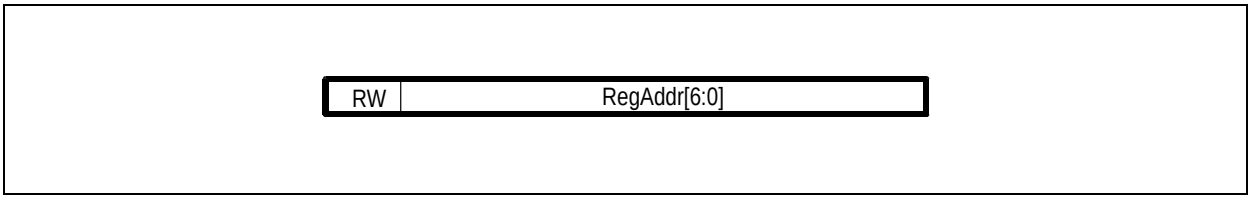


Figure 93:
Register Address to Be Read or Written

Bit	Meaning	Value
RW	Read/xWrite	RW = 0 write to reg address RW = 1 read from reg address
RegAddr[6:0]	Select register address	0x00 to 0x60

Figure 94:
Data

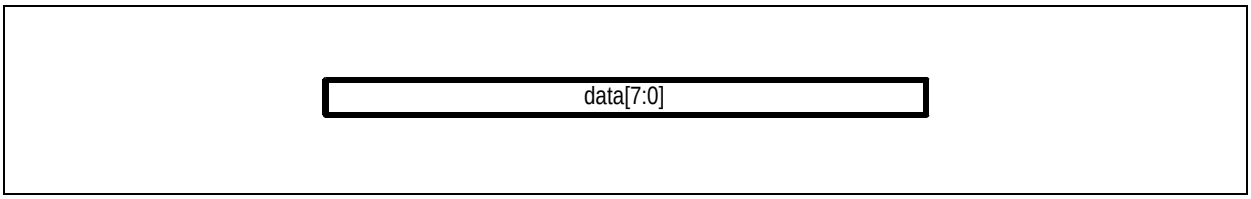


Figure 95:
Data Description

Bit	Meaning	Value
data[7:0]	Data	0x00 to 0xFF

Timings

DA...DevAddr

RA...RegAddr

D.....Data

Figure 96:
Write Single Data into Single Device

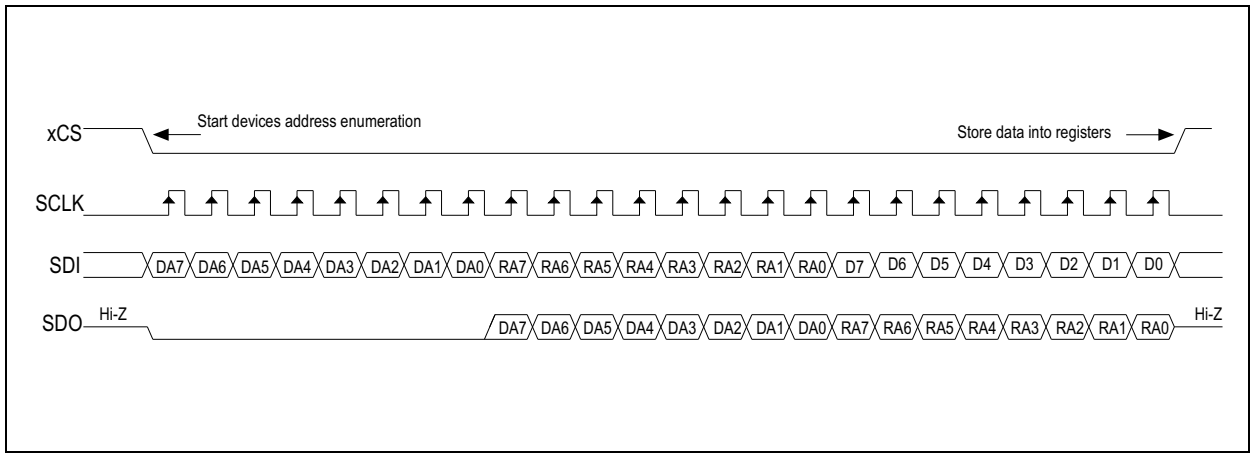
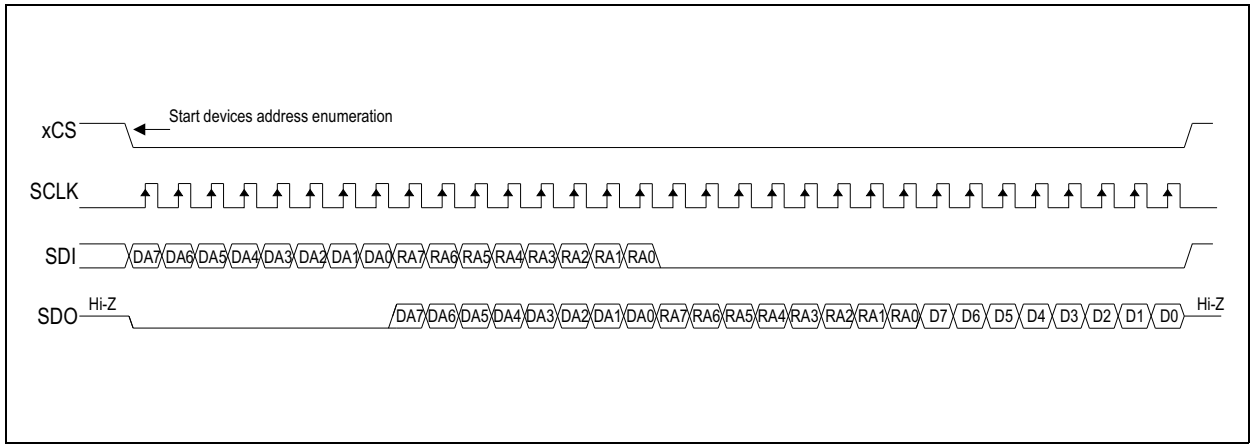


Figure 97:
Read Single Data from Single Device



SPI Protocol Examples

Write Single Data

Figure 98:
Write to Reg0x02 of Dev0x01

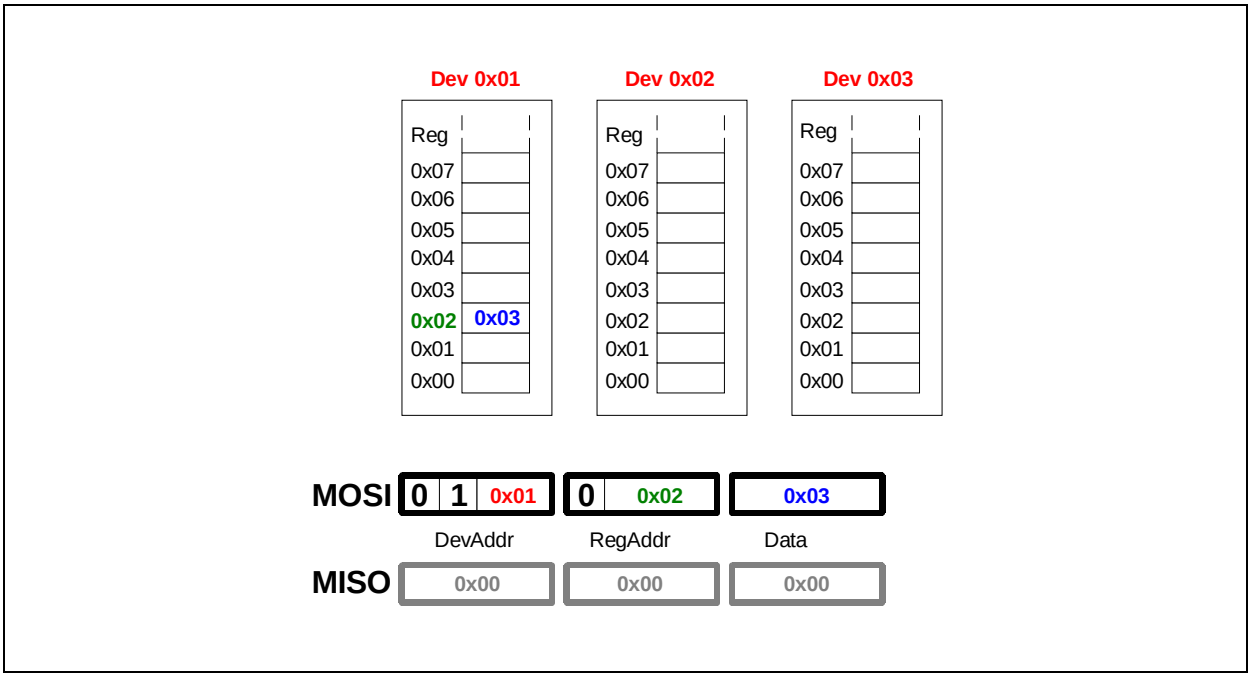
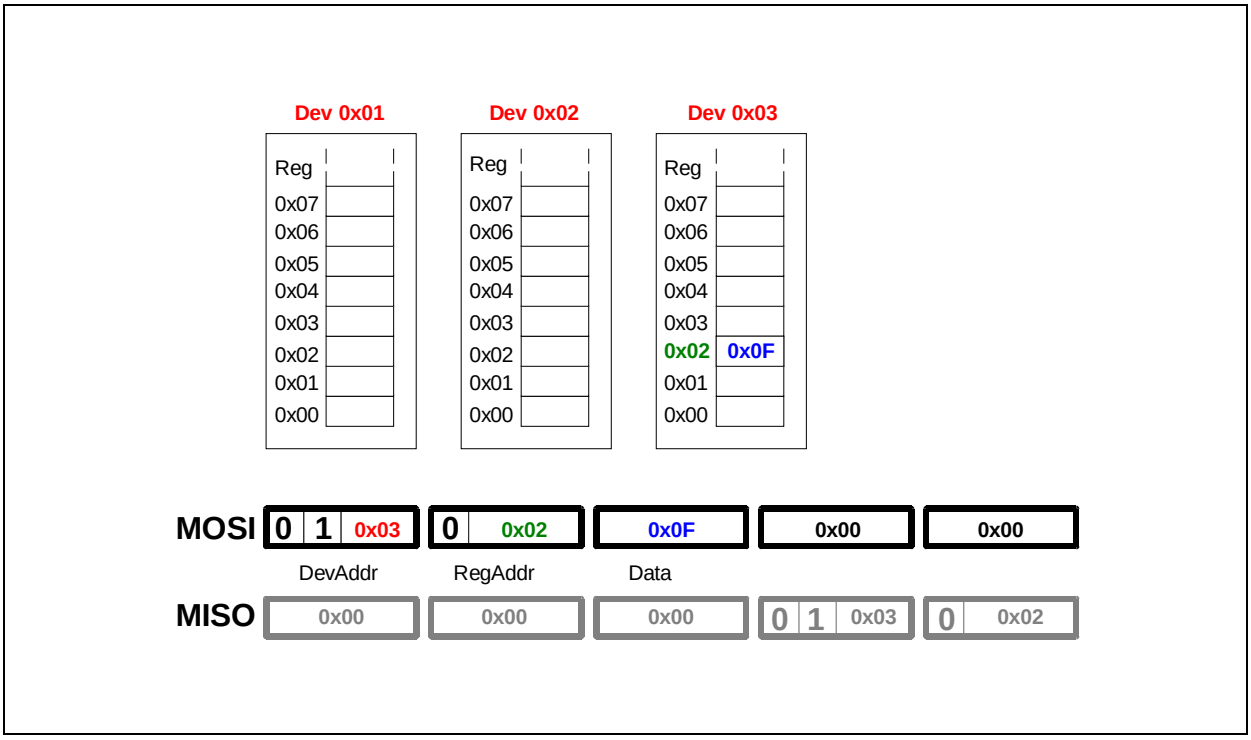
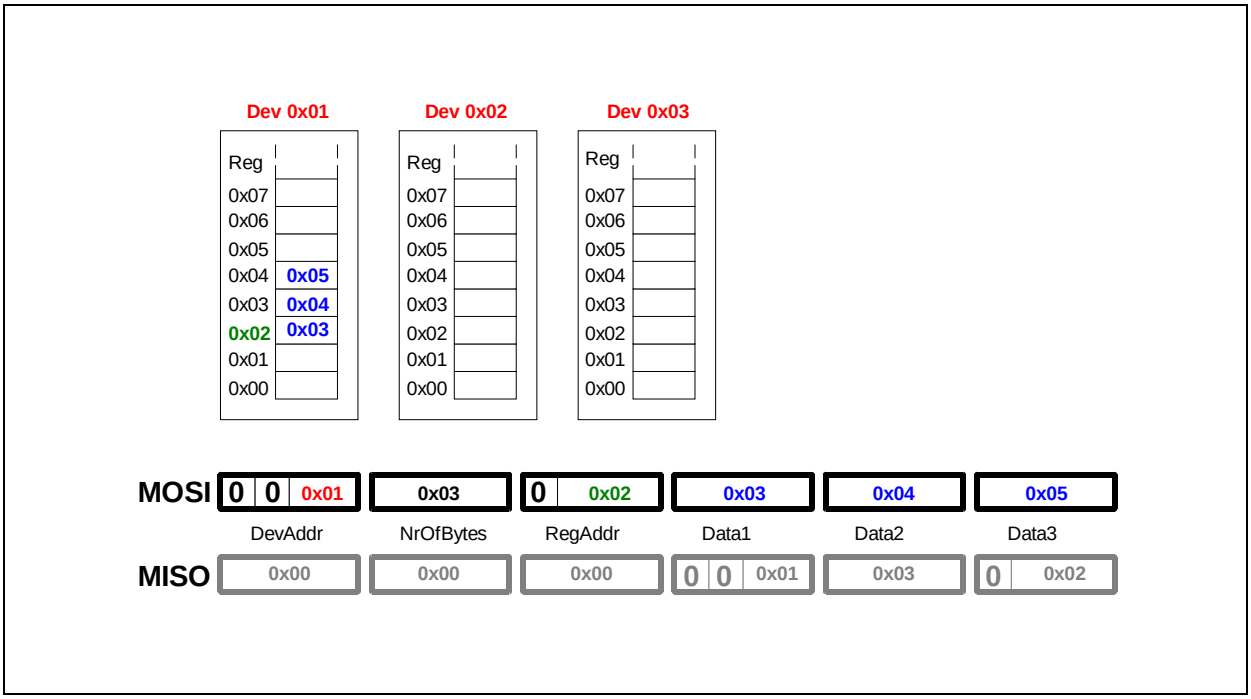


Figure 99:
Write to Reg0x02 of Dev0x03



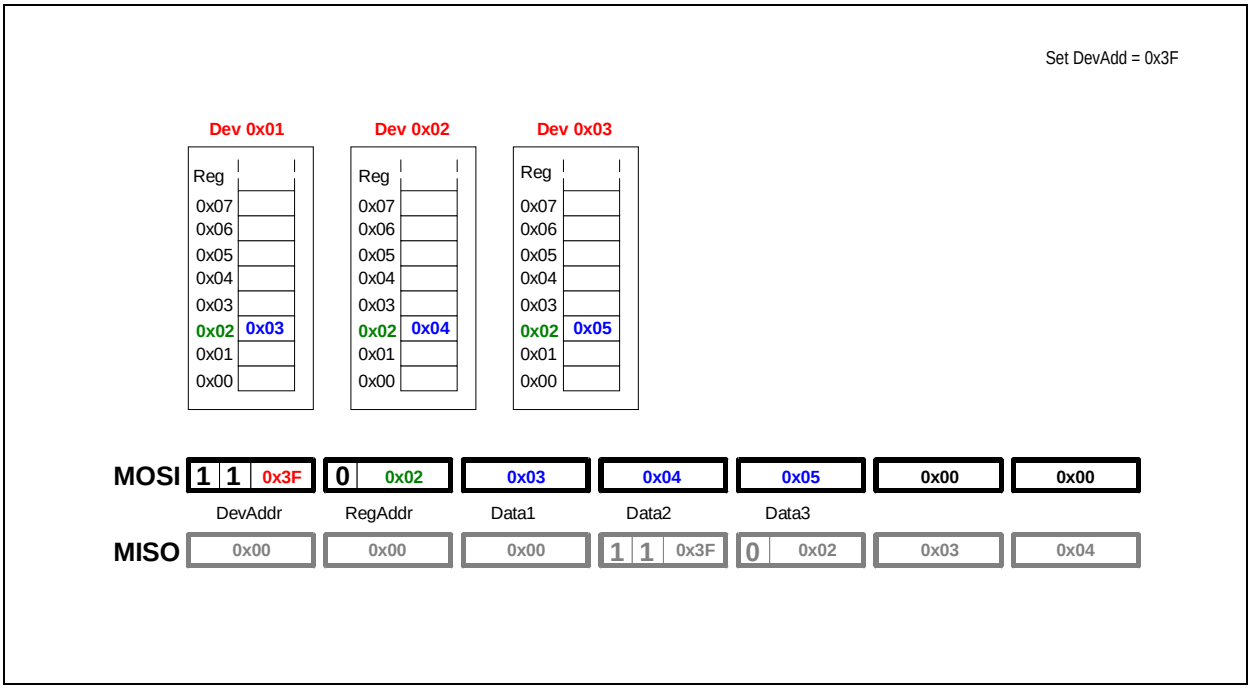
Write N Data

Figure 100:
Write to Reg0x02 - Reg0x04 of Dev0x01



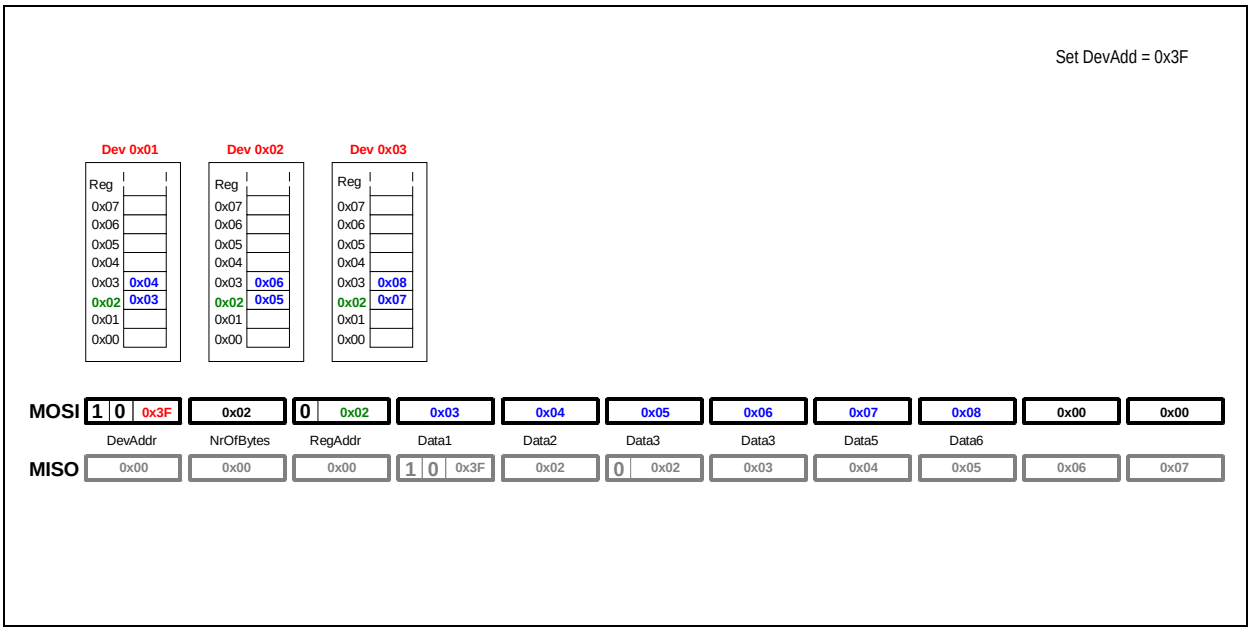
Write Different Data in Same Register of All Devices (single byte)

Figure 101:
Write to Reg0x02 of Dev0x01 – Dev0x03



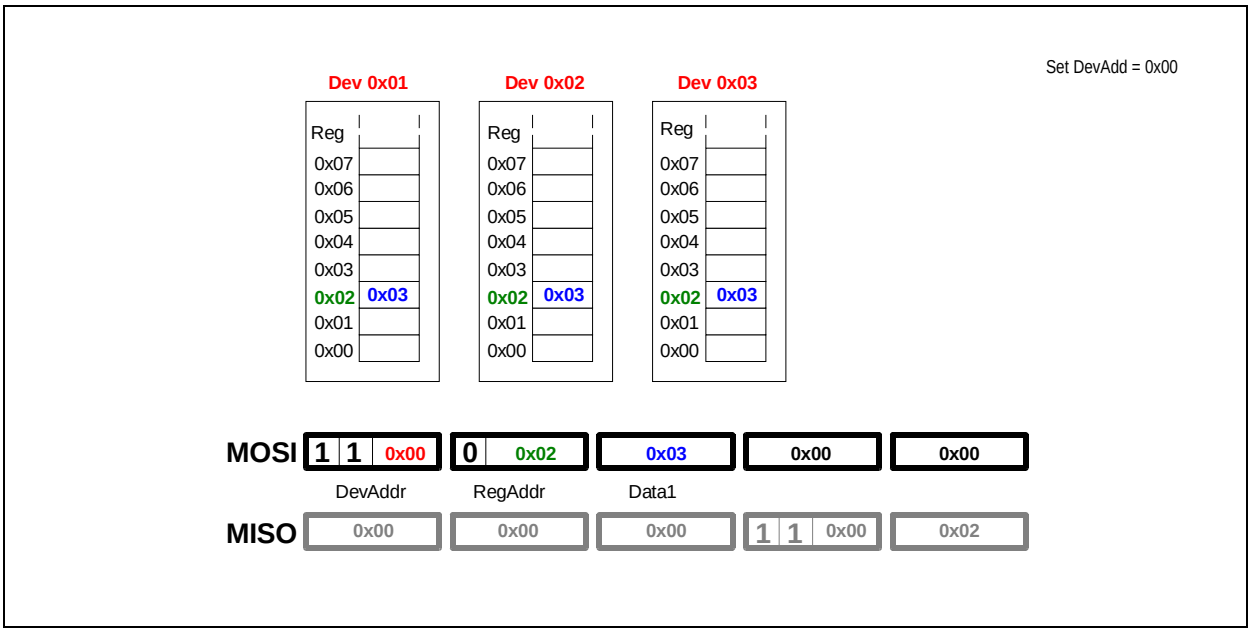
Write Different Data in Same Register of All Devices (multiple bytes)

Figure 102:
Write to Reg0x02- Reg0x03 of Dev0x01 – Dev0x03



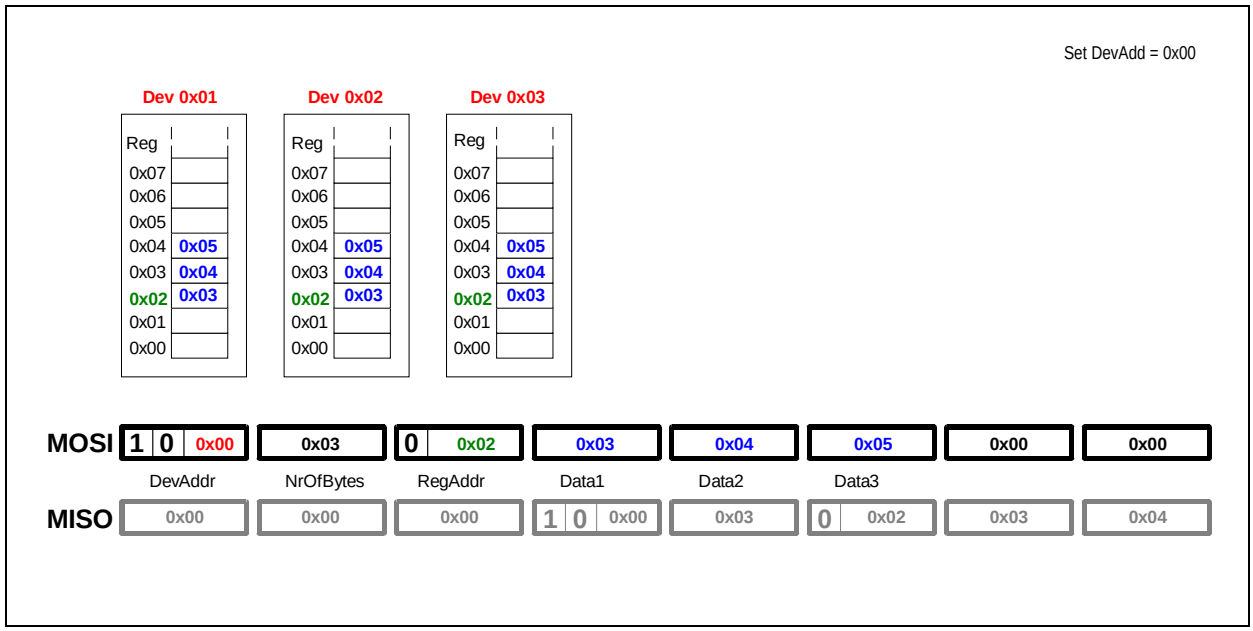
Write Same Data in Same Register of All Devices (single byte)

Figure 103:
Write to Reg0x02 of Dev0x01 – Dev0x03



Write Same Data in Same Register of All Devices (multiple bytes)

Figure 104:
Write to Reg0x02 - Reg0x04 of Dev0x01 – Dev0x03



Read Single Data

Figure 105:
Read from Reg0x02 of Dev0x01

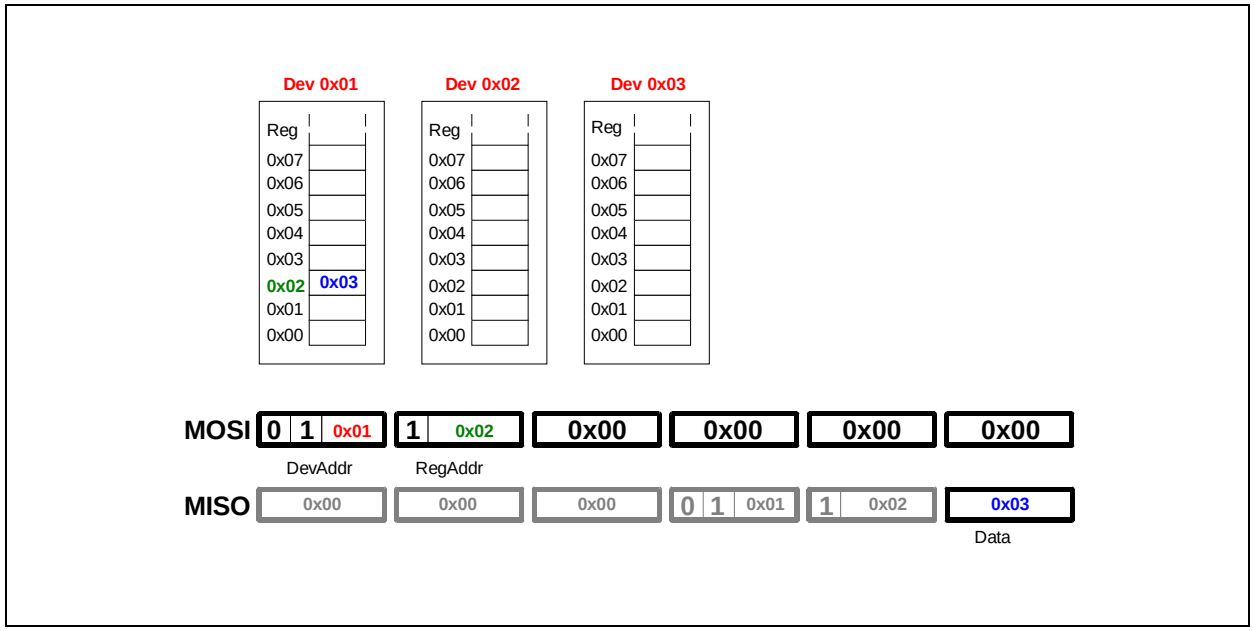
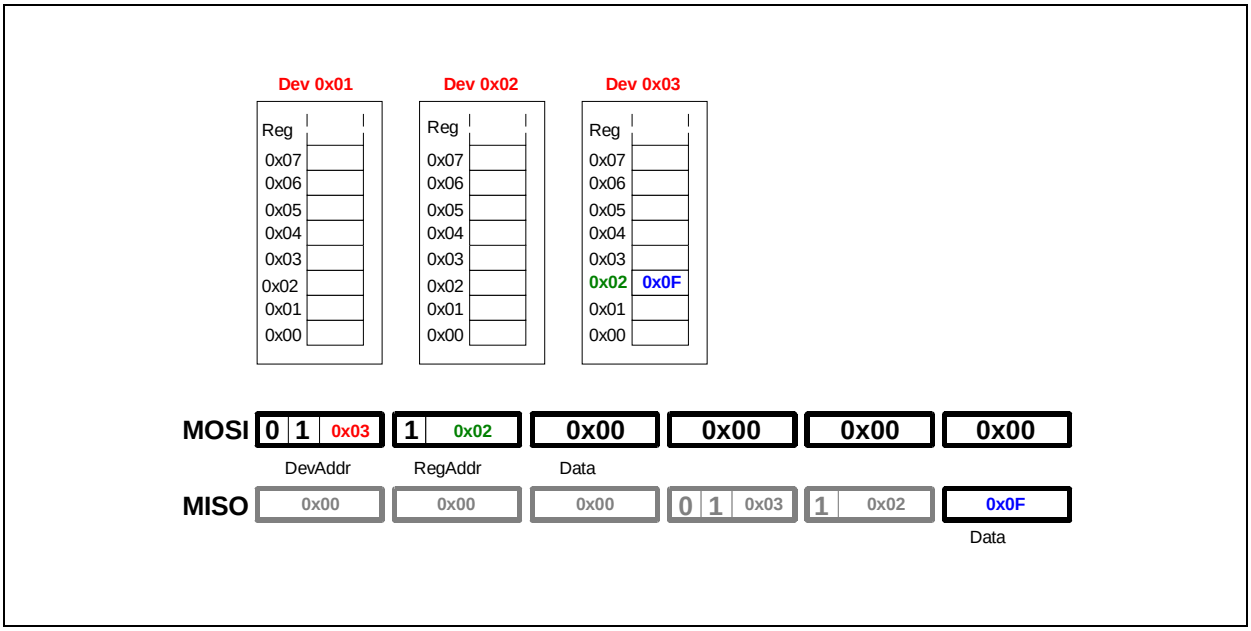
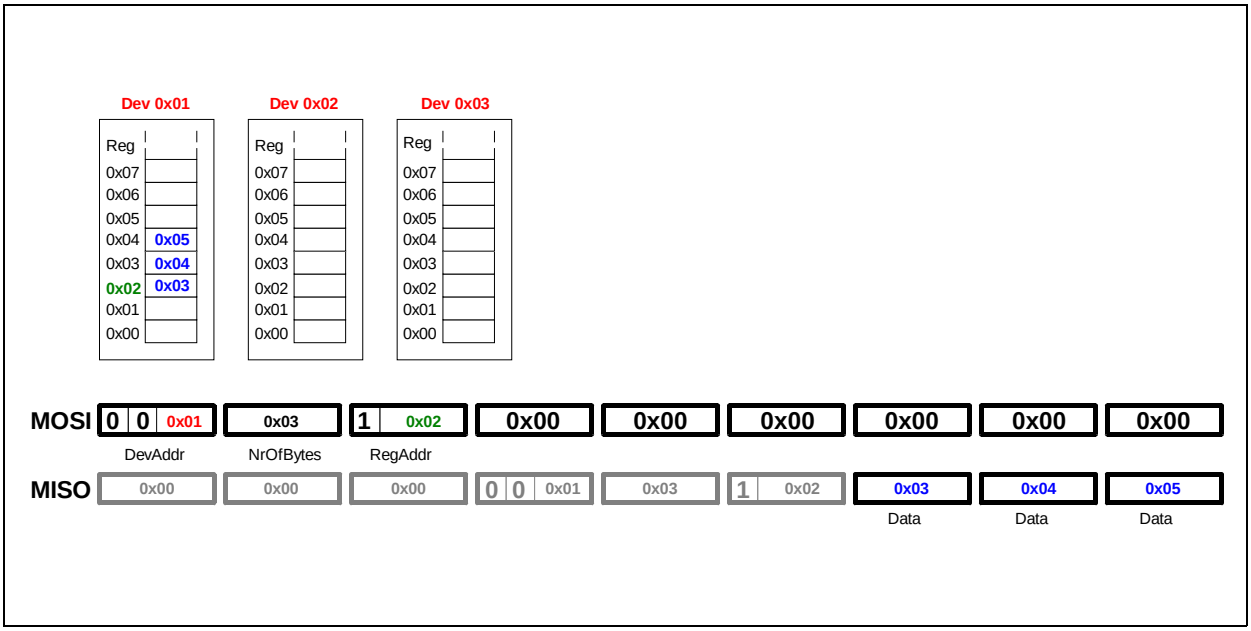


Figure 106:
Read from Reg0x02 of Dev0x03



Read N Data

Figure 107:
Read from Reg0x02-Reg0x04 of Dev0x03



Register Map

Figure 108:
Color Coding in Register Map

Registers can only be written if **Group1** is UNLOCKED. **Default = LOCKED**
Registers can only be written if **Group2** is UNLOCKED. **Default = LOCKED**

Figure 109:
Register Map

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00		Used for block writing								
0x01	CUR_ON_1	Curr_8	Curr_7	Curr_6	Curr_5	Curr_4	Curr_3	Curr_2	Curr_1	0x00
0x02	CUR_ON_2	Curr_16	Curr_15	Curr_14	Curr_13	Curr_12	Curr_11	Curr_10	Curr_9	0x00
0x03	FAULT_1	Autotoff_ uv			Retrial_ Short	Retrial_ Open	Autotoff_ot	Autotoff_ short	Autotoff_ open	0x84
0x04	FAULT_2			Short_volt				Short_en	Open_en	0x00
0x05	CASC_EXT	Casbias_en				casc				0x80
0x06	FB_SEL1	FBsel_8	FBsel_7	FBsel_6	FBsel_5	FBsel_4	FBsel_3	FBsel_2	FBsel_1	0x00
0x07	FB_SEL2	FBsel_16	FBsel_15	FBsel_14	FBsel_13	FBsel_12	FBsel_11	FBsel_10	FBsel_9	0x00
0x08	CURR_CTRL				Iledrange			Slew_rate		0x00
0x09	SHORTLED_1	Short_8	Short_7	Short_6	Short_5	Short_4	Short_3	Short_2	Short_1	0x00
0x0A	SHORTLED_2	Short_16	Short_15	Short_14	Short_13	Short_12	Shor_11	Shor_10	Short_9	0x00
0x0B	OPENLED_1	Open_8	Open_7	Open_6	Open_5	Open_4	Open_3	Open_2	Open_1	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0C	OPENLED_2	Open_16	Open_15	Open_14	Open_13	Open_12	Open_11	Open_10	Open_9	0x00
0x0D	IDAC_LED	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	0x00
0x0E	FB_ON_1	FB_ Curr_8	FB_ Curr_7	FB_ Curr_6	FB_ Curr_5	FB_ Curr_4	FB_ Curr_3	FB_ Curr_2	FB_ Curr_1	0x00
0x0F	FB_ON_2	FB_ Curr_16	FB_ Curr_15	FB_ Curr_14	FB_ Curr_13	FB_ Curr_12	FB_ Curr_11	FB_ Curr_10	FB_ Curr_9	0x00
0x10	IDAC_FB1_COUNTER	IDAC_FB1_COUNTER								0x00
0x11	IDAC_FB2_COUNTER	IDAC_FB2_COUNTER								0x00
0x12	FBLOOP_CTRL		FB_cnt_ man_fb2	FB_cnt_ man_fb1		FB_count_dn_time		FB_count_up_time		0x05
0x13	PWM_CTRL			PWM_rev	VSYNC det	VSYNC edge	Direct_ PWM	Update_ Mode	Clock_Src	0x00
0x14	PWMperiodLSB	PWM Per7	PWM Per6	PWM Per5	PWM Per4	PWM Per3	PWM Per2	PWM Per1	PWM Per0	0x00
0x15	PWMperiodMSB	0	0	0	PWM Per12	PWM Per11	PWM Per10	PWM Per9	PWM Per8	0x00
0x16	PWM1delLSB	PWM1 Del7	PWM1 Del6	PWM1 Del5	PWM1 Del4	PWM1 Del3	PWM1 Del2	PWM1 Del1	PWM1 Del0	0x00
0x17	PWM1delMSB	0	0	0	0	PWM1 Del11	PWM1 Del10	PWM1 Del9	PWM1 Del8	0x00
0x18	PWM2delLSB	PWM2 Del7	PWM2 Del6	PWM2 Del5	PWM2 Del4	PWM2 Del3	PWM2 Del2	PWM2 Del1	PWM2 Del0	0x00
0x19	PWM2delMSB	0	0	0	0	PWM2 Del11	PWM2 Del10	PWM2 Del9	PWM2 Del8	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x1A	PWM3delLSB	PWM3 Del7	PWM3 Del6	PWM3 Del5	PWM3 Del4	PWM3 Del3	PWM3 Del2	PWM3 Del1	PWM3 Del0	0x00
0x1B	PWM3delMSB	0	0	0	0	PWM3 Del11	PWM3 Del10	PWM3 Del9	PWM3 Del8	0x00
0x1C	PWM4delLSB	PWM4 Del7	PWM4 Del6	PWM4 Del5	PWM4 Del4	PWM4 Del3	PWM4 Del2	PWM4 Del1	PWM4 Del0	0x00
0x1D	PWM4delMSB	0	0	0	0	PWM4 Del11	PWM4 Del10	PWM4 Del9	PWM4 Del8	0x00
0x1E	PWM5delLSB	PWM5 Del7	PWM5 Del6	PWM5 Del5	PWM5 Del4	PWM5 Del3	PWM5 Del2	PWM5 Del1	PWM5 Del0	0x00
0x1F	PWM5delMSB	0	0	0	0	PWM5 Del11	PWM5 Del10	PWM5 Del9	PWM5 Del8	0x00
0x20	PWM6delLSB	PWM6 Del7	PWM6 Del6	PWM6 Del5	PWM6 Del4	PWM6 Del3	PWM6 Del2	PWM6 Del1	PWM6 Del0	0x00
0x21	PWM6delMSB	0	0	0	0	PWM6 Del11	PWM6 Del10	PWM6 Del9	PWM6 Del8	0x00
0x22	PWM7delLSB	PWM7 Del7	PWM7 Del6	PWM7 Del5	PWM7 Del4	PWM7 Del3	PWM7 Del2	PWM7 Del1	PWM7 Del0	0x00
0x23	PWM7delMSB	0	0	0	0	PWM7 Del11	PWM7 Del10	PWM7 Del9	PWM7 Del8	0x00
0x24	PWM8delLSB	PWM8 Del7	PWM8 Del6	PWM8 Del5	PWM8 Del4	PWM8 Del3	PWM8 Del2	PWM8 Del1	PWM8 Del0	0x00
0x25	PWM8delMSB	0	0	0	0	PWM8 Del11	PWM8 Del10	PWM8 Del9	PWM8 Del8	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x26	PWM9delLSB	PWM9 Del7	PWM9 Del6	PWM9 Del5	PWM9 Del4	PWM9 Del3	PWM9 Del2	PWM9 Del1	PWM9 Del0	0x00
0x27	PWM9delMSB	0	0	0	0	PWM9 Del11	PWM9 Del10	PWM9 Del9	PWM9 Del8	0x00
0x28	PWM10delLSB	PWM10 Del7	PWM10 Del6	PWM10 Del5	PWM10 Del4	PWM10 Del3	PWM10 Del2	PWM10 Del1	PWM10 Del0	0x00
0x29	PWM10delMSB	0	0	0	0	PWM10 Del11	PWM10 Del10	PWM10 Del9	PWM10 Del8	0x00
0x2A	PWM11delLSB	PWM11 Del7	PWM11 Del6	PWM11 Del5	PWM11 Del4	PWM11 Del3	PWM11 Del2	PWM11 Del1	PWM1 Del0	0x00
0x2B	PWM11delMSB	0	0	0	0	PWM11 Del11	PWM11 Del10	PWM11 Del9	PWM Del8	0x00
0x2C	PWM12delLSB	PWM12 Del7	PWM12 Del6	PWM12 Del5	PWM12 Del4	PWM12 Del3	PWM12 Del2	PWM12 Del1	PWM12 Del0	0x00
0x2D	PWM12delMSB	0	0	0	0	PWM12 Del11	PWM12 Del10	PWM12 Del9	PWM12 Del8	0x00
0x2E	PWM13delLSB	PWM13 Del7	PWM13 Del6	PWM13 Del5	PWM13 Del4	PWM13 Del3	PWM13 Del2	PWM13 Del1	PWM13 Del0	0x00
0x2F	PWM13delMSB	0	0	0	0	PWM13 Del11	PWM13 Del10	PWM13 Del9	PWM13 Del8	0x00
0x30	PWM14delLSB	PWM14 Del7	PWM14 Del6	PWM14 Del5	PWM14 Del4	PWM14 Del3	PWM14 Del2	PWM14 Del1	PWM14 Del0	0x00
0x31	PWM14delMSB	0	0	0	0	PWM14 Del11	PWM14 Del10	PWM14 Del9	PWM14 Del8	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x32	PWM15delLSB	PWM15 Del7	PWM15 Del6	PWM15 Del5	PWM15 Del4	PWM15 Del3	PWM15 Del2	PWM15 Del1	PWM15 Del0	0x00
0x33	PWM15delMSB	0	0	0	0	PWM15 Del11	PWM15 Del10	PWM15 Del9	PWM15 Del8	0x00
0x34	PWM16delLSB	PWM16 Del7	PWM16 Del6	PWM16 Del5	PWM16 Del4	PWM16 Del3	PWM16 Del2	PWM16 Del1	PWM16 Del0	0x00
0x35	PWM16delMSB	0	0	0	0	PWM16 Del11	PWM16 Del10	PWM16 Del9	PWM16 Del8	0x00
0x36	LOCKUNLOCK	MagicByte								0x00
0x37	PWM1htLSB	PWM1 HT7	PWM1 HT6	PWM1 HT5	PWM1 HT4	PWM1 HT3	PWM1 HT2	PWM1 HT1	PWM1 HT0	0x00
0x38	PWM1htMSB	0	0	0	0	PWM1 HT11	PWM1 HT10	PWM1 HT9	PWM1 HT8	0x00
0x39	PWM2htLSB	PWM2 HT7	PWM2 HT6	PWM2 HT5	PWM2 HT4	PWM2 HT3	PWM2 HT2	PWM2 HT1	PWM2 HT0	0x00
0x3A	PWM2htMSB	0	0	0	0	PWM2 HT11	PWM2 HT10	PWM2 HT9	PWM2 HT8	0x00
0x3B	PWM3htLSB	PWM3 HT7	PWM3 HT6	PWM3 HT5	PWM3 HT4	PWM3 HT3	PWM3 HT2	PWM3 HT1	PWM3 HT0	0x00
0x3C	PWM3htMSB	0	0	0	0	PWM3 HT11	PWM3 HT10	PWM3 HT9	PWM3 HT8	0x00
0x3D	PWM4htLSB	PWM4 HT7	PWM4 HT6	PWM4 HT5	PWM4 HT4	PWM4 HT3	PWM4 HT2	PWM4 HT1	PWM4 HT0	0x00
0x3E	PWM4htMSB	0	0	0	0	PWM4 HT11	PWM4 HT10	PWM4 HT9	PWM4 HT8	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3F	PWM5htLSB	PWM5 HT7	PWM5 HT6	PWM5 HT5	PWM5 HT4	PWM5 HT3	PWM5 HT2	PWM5 HT1	PWM5 HT0	0x00
0x40	PWM5htMSB	0	0	0	0	PWM5 HT11	PWM5 HT10	PWM5 HT9	PWM5 HT8	0x00
0x41	PWM6htLSB	PWM6 HT7	PWM6 HT6	PWM6 HT5	PWM6 HT4	PWM6 HT3	PWM6 HT2	PWM6 HT1	PWM6 HT0	0x00
0x42	PWM6htMSB	0	0	0	0	PWM6 HT11	PWM6 HT10	PWM6 HT9	PWM6 HT8	0x00
0x43	PWM7htLSB	PWM7 HT7	PWM7 HT6	PWM7 HT5	PWM7 HT4	PWM7 HT3	PWM7 HT2	PWM7 HT1	PWM7 HT0	0x00
0x44	PWM7htMSB	0	0	0	0	PWM7 HT11	PWM7 HT10	PWM7 HT9	PWM7 HT8	0x00
0x45	PWM8htLSB	PWM8 HT7	PWM8 HT6	PWM8 HT5	PWM8 HT4	PWM8 HT3	PWM8 HT2	PWM8 HT1	PWM8 HT0	0x00
0x46	PWM8htMSB	0	0	0	0	PWM8 HT11	PWM8 HT10	PWM8 HT9	PWM8 HT8	0x00
0x47	PWM9htLSB	PWM9 HT7	PWM9 HT6	PWM9 HT5	PWM9 HT4	PWM9 HT3	PWM9 HT2	PWM9 HT1	PWM9 HT0	0x00
0x48	PWM9htMSB	0	0	0	0	PWM9 HT11	PWM9 HT10	PWM9 HT9	PWM9 HT8	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x49	PWM10htLSB	PWM10 HT7	PWM10 HT6	PWM10 HT5	PWM10 HT4	PWM10 HT3	PWM10 HT2	PWM10 HT1	PWM10 HT0	0x00
0x4A	PWM10htMSB	0	0	0	0	PWM10 HT11	PWM10 HT10	PWM10 HT9	PWM10 HT8	0x00
0x4B	PWM11htLSB	PWM11 HT7	PWM11 HT6	PWM11 HT5	PWM11 HT4	PWM11 HT3	PWM11 HT2	PWM11 HT1	PWM11 HT0	0x00
0x4C	PWM11htMSB	0	0	0	0	PWM11 HT11	PWM11 HT10	PWM11 HT9	PWM11 HT8	0x00
0x4D	PWM12htLSB	PWM12 HT7	PWM12 HT6	PWM12 HT5	PWM12 HT4	PWM12 HT3	PWM12 HT2	PWM12 HT1	PWM12 HT0	0x00
0x4E	PWM12htMSB	0	0	0	0	PWM12 HT11	PWM12 HT10	PWM12 HT9	PWM12 HT8	0x00
0x4F	PWM13htLSB	PWM13 HT7	PWM13 HT6	PWM13 HT5	PWM13 HT4	PWM13 HT3	PWM13 HT2	PWM13 HT1	PWM13 HT0	0x00
0x50	PWM13htMSB	0	0	0	0	PWM13 HT11	PWM13 HT10	PWM13 HT9	PWM13 HT8	0x00
0x51	PWM14htLSB	PWM14 HT7	PWM14 HT6	PWM14 HT5	PWM14 HT4	PWM14 HT3	PWM14 HT2	PWM14 HT1	PWM14 HT0	0x00
0x52	PWM14htMSB	0	0	0	0	PWM14 HT11	PWM14 HT10	PWM14 HT9	PWM14 HT8	0x00

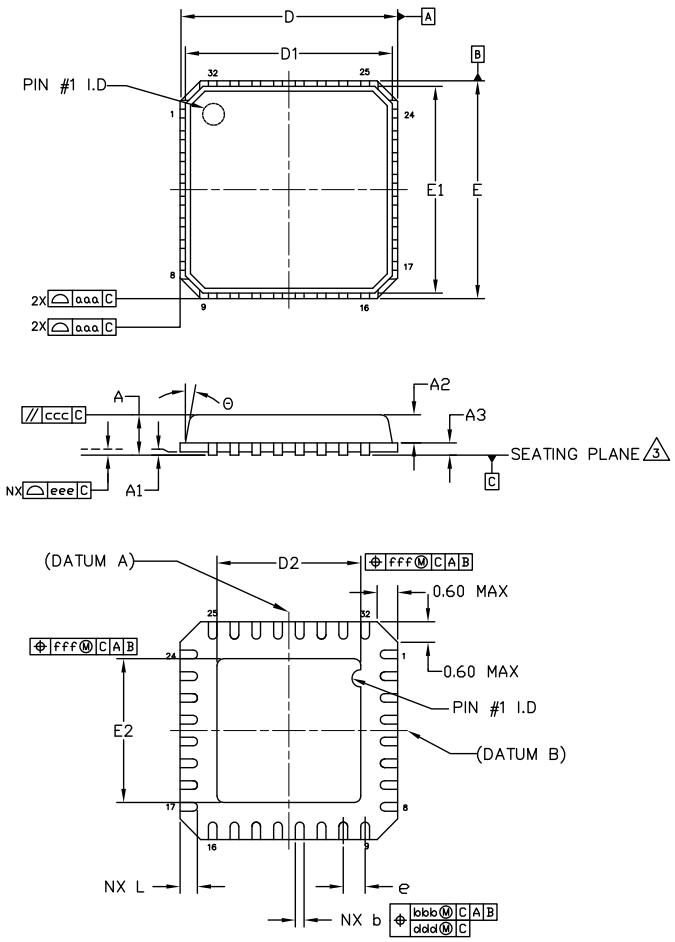
Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x53	PWM15htLSB	PWM15 HT7	PWM15 HT6	PWM15 HT5	PWM15 HT4	PWM15 HT3	PWM15 HT2	PWM15 HT1	PWM15 HT0	0x00
0x54	PWM15htMSB	0	0	0	0	PWM15 HT11	PWM15 HT10	PWM15 HT9	PWM15 HT8	0x00
0x55	PWM16htLSB	PWM16 HT7	PWM16 HT6	PWM16 HT5	PWM16 HT4	PWM16 HT3	PWM16 HT2	PWM16 HT1	PWM16 HT0	0x00
0x56	PWM16htMSB	0	0	0	0	PWM16 HT11	PWM16 HT10	PWM16 HT9	PWM16 HT8	0x00
0x57	ASICIDLSB	Asic_ID0				Rev Nr.				0xD2
0x58	ASICIDMSB	ASIC_ID2				ASIC_ID1				0x10
0x59	Not used									0x00
0x60	STATUS	STAT Nosync	STAT OT	STAT Open	STAT Short	0	STAT UVLO	STAT power		

Note(s):

1. Addresses above 0x60 are for factory test only. DO NOT WRITE!

Package Drawings & Markings

Figure 110:
32-pin QFN Package



Ref	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3	-	0.20 REF	-
L	0.35	0.40	0.45
Θ	0°	-	14°
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
D1	-	4.75 BSC	-
E1	-	4.75 BSC	-
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

Note(s):

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Thermal Characteristics

The thermal characteristics of the devices were measured at 25°C ambient temperature. The device was mounted on a double sided FR4 PCB with the bottom layer used as cooling area.

Figure 113:
PCB FR4, 1cm Distance from Ground

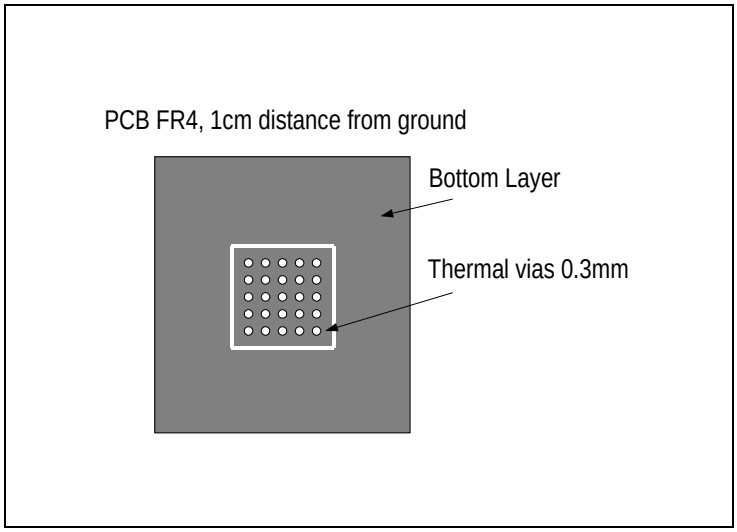


Figure 114:
Tcase vs Power QFN-32 with Different Copper Area, T_A = 25°C

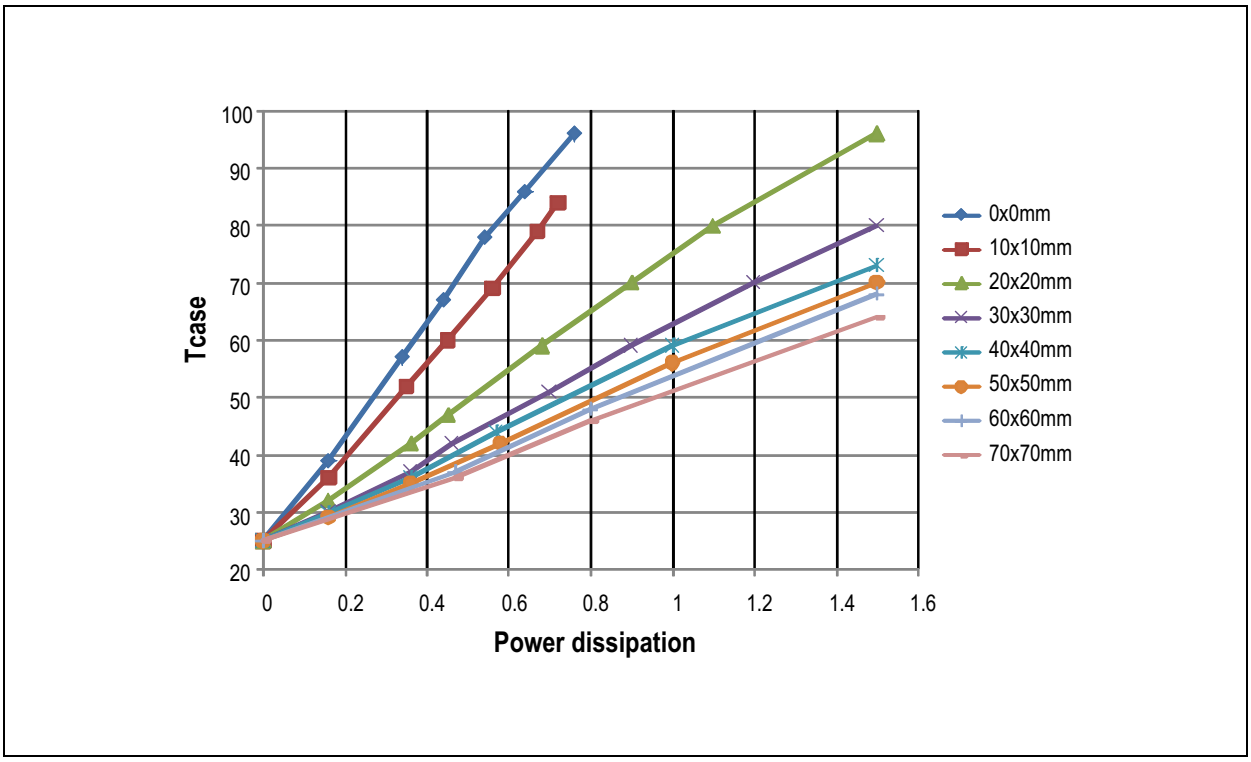
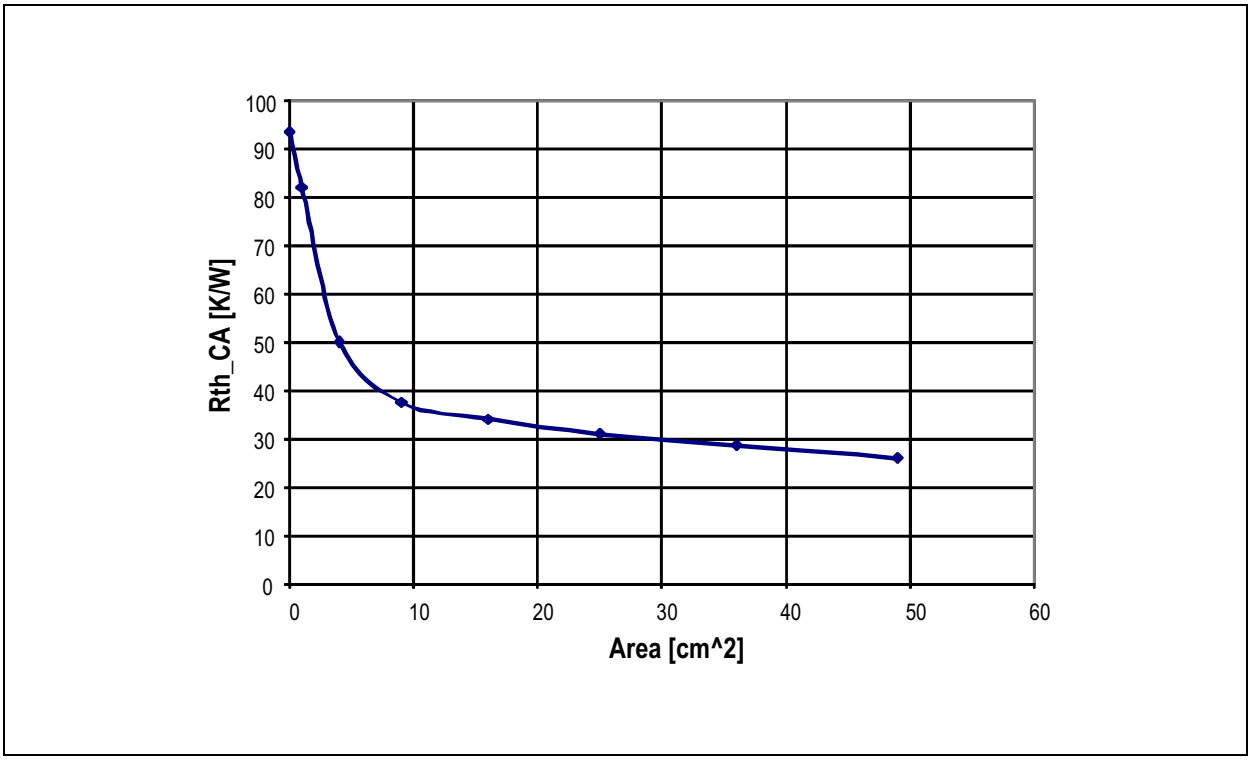


Figure 115:
Rth_CA [K/W] vs Copper Area



Ordering Information

The devices are available as the standard products shown in Figure 116.

Figure 116:
Ordering Information

Ordering Code	Package	Marking	Description	Delivery Form	Delivery Quantity
AS3810-ZQFT	32-pin QFN	AS3810	16 Channel White LED Driver for LCD Backlight	Tape & Reel	4000

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