

# AS3833

## 6 channel high-precision LED controller for 3D-LCD backlight with integrated step-up controller

### 1 General Description

The AS3833 is a 6 channel high precision LED controller with PWM input for driving external bipolar transistors in LCD-backlight panels, optimized for 2D and 3D operation.

The integrated step-up controller provides the necessary output voltage for the LED string supply.

The SMPS feedback control optimizes the power efficiency by adjusting the LED string supply voltage.

Build in safety features include under-voltage and thermal shutdown as well as open and short LED detection.

- Output current up to 250mA per channel
- Absolute current accuracy +/- 0.8%
- Channel to channel accuracy +/- 0.6%
- 1 PWM input with internal phase shift
- Open LED detection and disconnect
- Short LED protection and auto-turnoff
- Undervoltage shutdown
- Temperature shutdown
- Temperature supervision of external BJT
- BJT Beta compensation
- SMPS feedback control
- DCDC Softstart Function
- Over Voltage Protection (OVP)
- Package SOIC-28
- Package TQFP-32

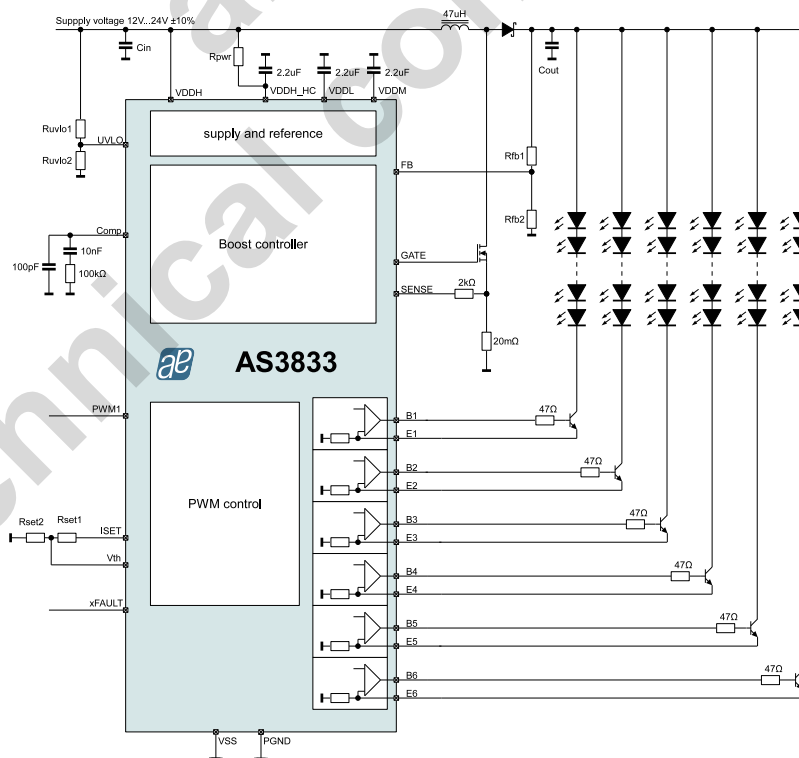
### 2 Key Features

- 6 channel LED controller
- Step-up controller optimized for 2D/3D mode
- Supply voltage range: 12V to 50V

### 3 Applications

LED backlighting for 3D-LCD backlight TV sets and monitors

Figure 1. AS3833

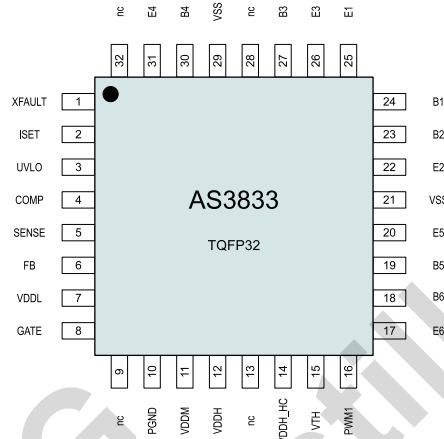
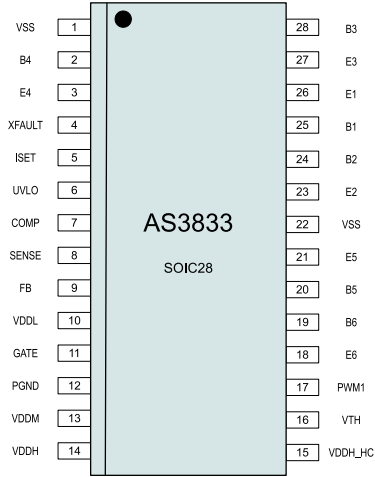


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## 4 Pin Assignments (Top View)

Figure 2. Pin Assignments (Top View)



## 4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number AS3833 TQFP-32	Pin Number AS3833 SOIC-28	Pin Name	Pin Type	Description
29	1	VSS	P	<b>Analog Ground</b>
30	2	B4	A_I/O	<b>Base 4.</b> Connect to base of external transistor.
31	3	E4	A_I/O	<b>Emitter 4.</b> Connect to emitter of external transistor.
1	4	xFAULT	DO_OD	<b>Fault output.</b> Active low.
2	5	ISET	A_I/O	<b>Current setting.</b> Connect current setting resistor.
3	6	UVLO	A_I/O	<b>Undervoltage lockout input.</b>
4	7	COMP	A_I/O	<b>Compensation network.</b> Connect compensation network.
5	8	SENSE	A_I/O	<b>Current sense input.</b> Provide a short, direct PCB path between this pin and the positive side of the current sense resistor.
6	9	FB	A_I/O	<b>Output voltage feedback input.</b> Input for voltage divider. Connect voltage divider output as short as possible to this pin
7	10	VDDL	A_I/O	<b>Voltage regulator output 3.3V.</b> Connect 2.2 $\mu$ F decoupling capacitor to GND
8	11	GATE	A_I/O	<b>Gate driver output.</b>
10	12	PGND	P	<b>Power Ground</b>
11	13	VDDM	P	<b>Voltage regulator output.</b> Connect 2.2 $\mu$ F decoupling capacitor to GND
12	14	VDDH	P	<b>Supply voltage.</b> Connect 1 $\mu$ F decoupling capacitor to GND
14	15	VDDH_HC	P	<b>Voltage regulator Input.</b> Connect 2.2 $\mu$ F decoupling capacitor to GND
15	16	VTH	A_I/O	<b>Reference input for overtemperature detection.</b>
16	17	PWM1	DI_PD	<b>PWM input 1.</b> PWM input for channel 1
17	18	E6	A_I/O	<b>Emitter 6.</b> Connect to emitter of external transistor.
18	19	B6	A_I/O	<b>Base 6.</b> Connect to base of external transistor.
19	20	B5	A_I/O	<b>Base 5.</b> Connect to base of external transistor.
20	21	E5	A_I/O	<b>Emitter 5.</b> Connect to emitter of external transistor.
21	22	VSS	P	<b>Analog Ground</b>
22	23	E2	A_I/O	<b>Emitter 2.</b> Connect to emitter of external transistor.
23	24	B2	A_I/O	<b>Base 2.</b> Connect to base of external transistor.
24	25	B1	A_I/O	<b>Base 1.</b> Connect to base of external transistor.
25	26	E1	A_I/O	<b>Emitter 1.</b> Connect to emitter of external transistor.
26	27	E3	A_I/O	<b>Emitter 3.</b> Connect to emitter of external transistor.
27	28	B3	A_I/O	<b>Base 3.</b> Connect to base of external transistor.

A\_I/O...Analog pin, P...Power pin, DO...digital output, DO\_OD...digital output open drain, DI...digital input, DI\_PU...digital input with pullup resistor, DI\_PD...digital input with pull down resistor

## 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
<b>Electrical Parameters</b>				
VDDH to VSS, VDDH_HC to VSS	-0.3	55	V	
VDDM to VSS, GATE to VSS	-0.3	25	V	
xFAULT to VSS	-0.3	7	V	
VDDL to VSS	-0.3	5	V	
Analog Pin Voltage to VSS <sup>1</sup>	-0.3	5	V	
Digital Pin Voltage to VSS <sup>2</sup>	-0.3	5	V	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
<b>Electrostatic Discharge</b>				
Electrostatic Discharge HBM		+/- 1500	V	Norm: MIL 883 E method 3015
Electrostatic Discharge MM		+/- 200	V	Norm: JESD22-A115C
<b>Continuous Power Dissipation (TA = +70°C)</b>				
Continuous Power Dissipation		1.5	W	PT <sup>3</sup> for SOIC-28 Package
Continuous Power Dissipation Derating Factor		13	mW / °C	PDERATE <sup>4</sup>
<b>Temperature Ranges and Storage Conditions</b>				
Junction to ambient thermal resistance		76	°C/W	SOIC-28 Package. For more information about thermal metrics, see application note AN01 Thermal Characteristics.
Junction Temperature (T <sub>Jmax</sub> )		+150	°C	
Storage Temperature Range	-55	+150	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level		1		Represents a max. floor life time of unlimited

1. Pins Vth, UVLO, Comp, Sense, FB, Iset, Ex, Bx

2. Pins PWMx

3. Depending on actual PCB layout and PCB used.

4. PDERATE derating factor changes the total continuous power dissipation (PT) if the ambient temperature is not 25°C. Therefore for e.g. TA=85°C calculate PT at 85°C = PT - PDERATE x (85°C - 25°C)

## 6 Electrical Characteristics

VDDH = 24V, all voltages referenced to VSS, Typical values are at TA = +25°C (unless otherwise specified). All limits are guaranteed. The parameters with min. and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>General</b>						
TA	Operating Temperature Range	apply proper cooling to stay below maximum allowed TJ.	-20		+85	°C
TJ	Operating Junction Temperature		-20		+115	°C
<b>Power supply</b>						
VDDH	Supply Voltage		+12		+50	V
VDDM	Driver supply voltage regulator output			+9		V
VDDL	3V voltage regulator output			+3.3		V
IDD	Operating Current Consumption	UVLO=2V, PWM1=0, Rset=6kΩ, Vth=0.47V	4.6	5.0	5.6	mA
IDDQ	Quiescent Current Consumption	UVLO=0V, PWM1=0, Rset=6kΩ, Vth=0.47V	2.25	2.50	2.75	mA
<b>Current sink parameters</b>						
I <sub>LED_100</sub>	Trimmed current accuracy	I <sub>LED</sub> =100mA, T <sub>j</sub> = 25°C excluding error of Rset	-0.8		+0.8	%
I <sub>LED_ALL</sub>	current accuracy	I <sub>LED</sub> =50 <sup>1</sup> to 250mA, BJT β>50 T <sub>j</sub> = -20 to +115°C	-1.5		+1.5	%
I <sub>CH_100</sub>	Channel to channel accuracy	I <sub>LED</sub> =100mA, T <sub>j</sub> = 25°C	-0.6		+0.6	%
V <sub>IsetX</sub>	Reference Voltage at pins Iset		+1.18	+1.20	+1.22	V
Ratio	Ratio = I <sub>LED</sub> /Iset			500		
I <sub>BX</sub>	Base output current limit		5.5		7.5	mA
<b>Short detection comparator</b>						
ACC <sub>short</sub>	Over-Temperature protection accuracy	Accuracy of V <sub>be</sub> comparison with V <sub>TH</sub> level	-10		+10	mV
<b>Power supply regulation</b>						
B <sub>th</sub>	BJT beta threshold		45	48	52	
<b>Boost controller oscillator</b>						
f <sub>osc</sub>	Oscillator frequency		220	250	280	kHz
<b>Boost controller PWM</b>						
D <sub>MAX</sub>	Maximum duty cycle		85	87	89	%
<b>Boost controller error amplifier</b>						
V <sub>FB</sub>	Reference Voltage at pin FB		+1.23	+1.25	+1.27	V
A <sub>V</sub>	Voltage gain			80		dB
BW	Bandwidth	A <sub>V</sub> = 0dB		2		MHz
I <sub>FB_in</sub>	Voltage sense input current	pins FB		0.1	0.2	μA
I <sub>comp_out</sub>	Compensation output current	pins COMP, V <sub>comp</sub> = 1V		10		μA
<b>Boost controller over current protection</b>						
V <sub>SENSE</sub>	Current sense threshold	pin SENSE	+600	+800	+1000	mV

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Boost controller driver</b>						
$R_{driver}$	Driver resistance sink and source	pin GATE	4	6	8	$\Omega$
$V_{driver}$	GATE maximum output voltage	IGATE = 0mA		VDDM		V
$t_{RISE\_driver}$	GATE voltage rise time	VGATE = 0 to 3V, CLOAD = 3nF	15	25	50	ns
$t_{FALL\_driver}$	GATE voltage fall time	VGATE = 3 to 0V, CLOAD = 3nF	15	25	50	ns
<b>Boost controller under voltage lockout</b>						
$V_{UVLO}$	Under voltage lockout threshold		+1.28	+1.35	+1.42	V
$I_{UVLO\_Hyst}$	Under voltage lockout hysteresis current			20		$\mu A$
<b>Digital pins</b>						
$V_{IH}$	Logic high input threshold		+1.8			V
$V_{IL}$	Logic low input threshold				+0.8	V
$V_{OL}$	Logic low output level	PIN xFAULT open drain. I = -2mA			+0.3	V
$R_{PU}$	Input resistance Pull-up inputs			300		k $\Omega$
$R_{PD}$	Input resistance Pull-down inputs			300		k $\Omega$
<b>Thermal protection</b>						
$T_{OFF}$	Thermal shutdown threshold			140		$^{\circ}C$
$T_{hyst}$	Thermal shutdown hysteresis			30		$^{\circ}C$

1. Is is not recommended to set ILED < 50mA in order to minimize influences of offset voltages.

## 7 Typical Operating Characteristics

$V_{OUT\ Boost} = 60V$ ;  $I_{OUT} = 1A$ ,  $T_{AMB} = +25^{\circ}C$  (unless otherwise specified).

Figure 3. Boost - Efficiency vs. Output Current;  $V_{IN} = 13V$

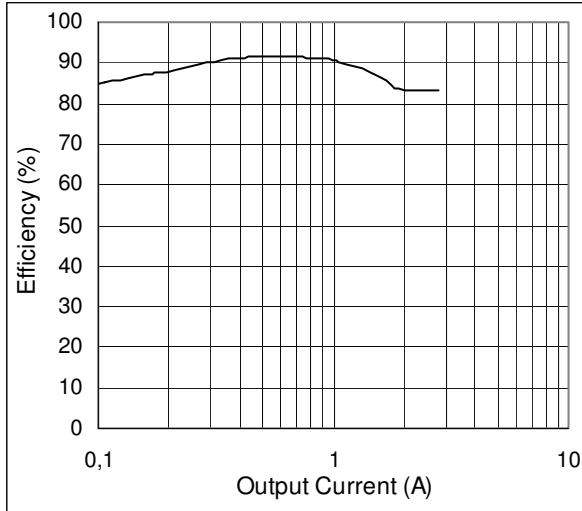


Figure 4. Boost - Efficiency vs. Output Current;  $V_{IN} = 24V$

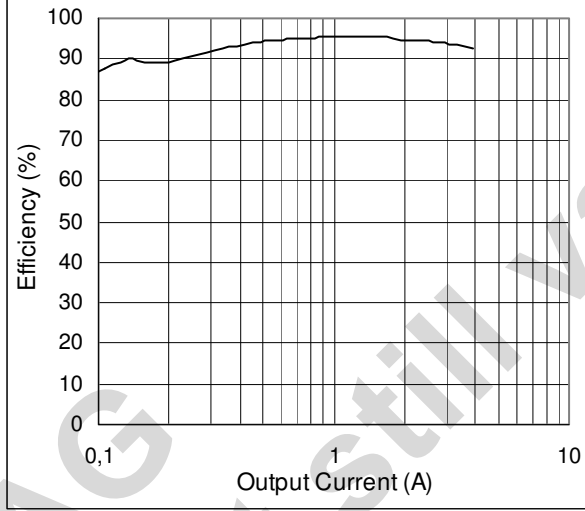


Figure 5.  $V_{OUT}$  vs.  $I_{OUT}$ ,  $V_{IN} = 13V$

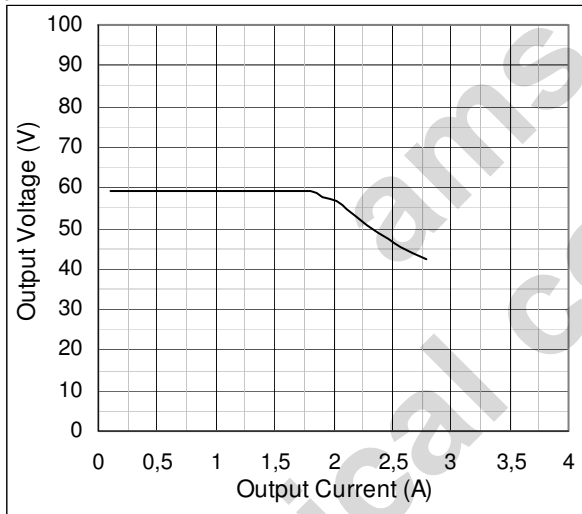




Figure 6.  $V_{OUT}$  vs.  $I_{OUT}$ ,  $V_{IN} = 24V$

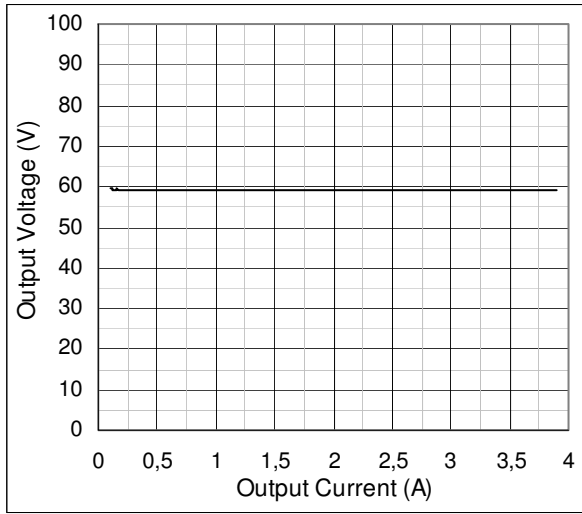


Figure 7. Boost - Efficiency vs. Input Voltage,  $I_{OUT} = 1A$

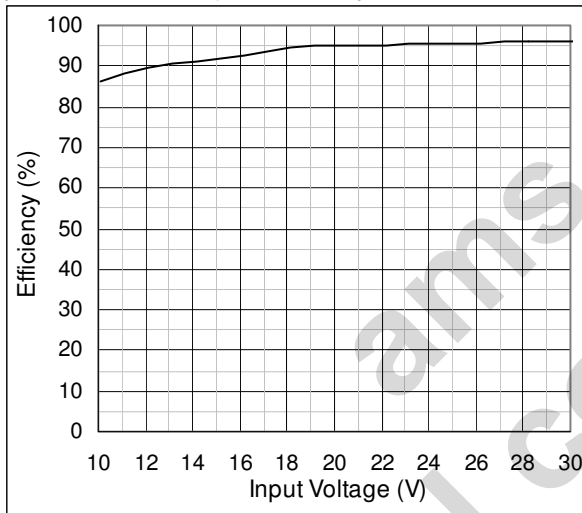
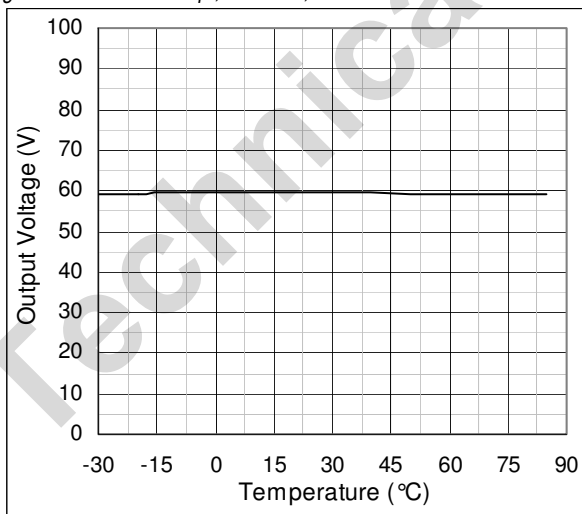


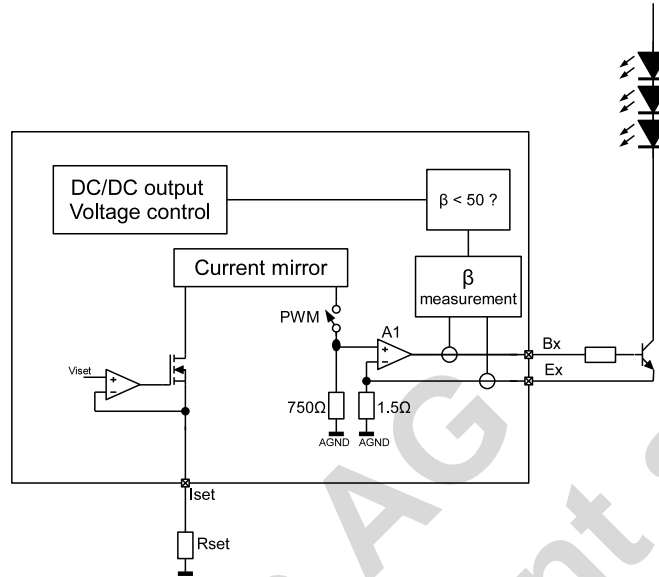
Figure 8.  $V_{OUT}$  vs. Temp,  $V_{IN} = 24V$ ,  $I_{OUT} = 0.2A$



## 8 Detailed Description

### 8.1 Precision current output

Figure 9. Current output stage



The LED-current is derived from either Rset using the following equation

$$I_{LED} = \text{RATIO} \times I_{set} = \text{RATIO} \times \frac{V_{set}}{R_{set}} = 500 \times \frac{1.2V}{R_{SET}} \tag{EQ 1}$$

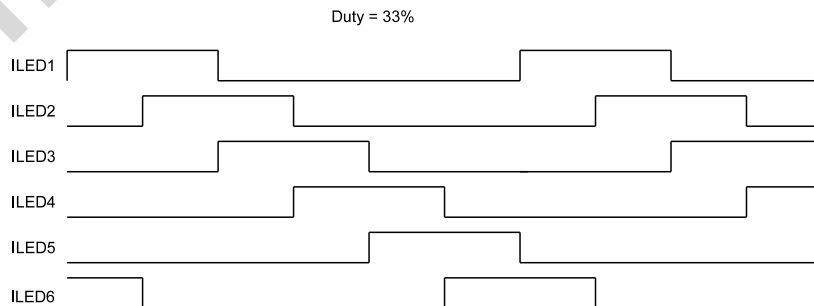
Iset is protected against a short to ground. In the case of a ground short the current Iset is limited to 660uA and the LED-current to 330mA.

Iset has a lower limit of 6uA with a 1uA hysteresis. This sets the lower limit of the LED-current to 3mA with Rset=200kΩ. If Rset is large than 200kΩ, the LED-current is set to 0mA.

#### 8.1.1 Phase shift

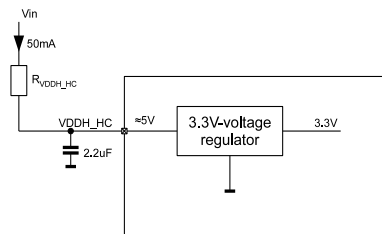
The outputs are controlled by the PWM-input and a built in phase shift generator. All outputs are phase shifted by 1/6 of the PWM-period. In order to calculate the phase shift timing, two PWM-periods are needed. This means that after changing the PWM-frequency, the phase shift is updated after the second period. The PWM-frequency must be in the range from 60Hz to 1kHz.

Figure 10. Phase shift



## 8.2 VDDH\_HC resistor

Figure 11. VDDH\_HC resistor



Pin VDDH\_HC is connected to an internal 3.3V voltage regulator. In order to keep the power dissipation of this regulator low, it is recommended to connect pin VDDH\_HC to the power supply  $V_{in}$  with a resistor. The resistor should guarantee sufficient voltage drop so that the remaining voltage at pin VDDH\_HC is approximately 5V. The power dissipation of the  $R_{VDDH\_HC}$  has to be considered.

$$R_{VDDH\_HC} = \frac{V_{in} - 5V}{75mA} \quad (EQ 2)$$

$$P_{R_{VDDH\_HC}} = (75mA)^2 \times R_{VDDH\_HC} \quad (EQ 3)$$

Typical values for  $R_{VDDH\_HC}$  are:

$V_{IN} = 13V$ :  $R_{VDDH\_HC} = 100\Omega / 1W$

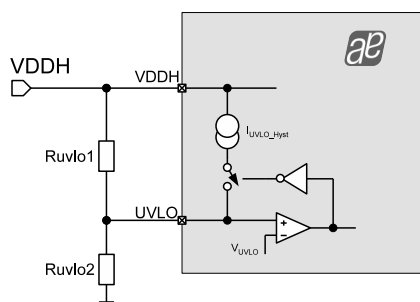
$V_{IN} = 24V$ :  $R_{VDDH\_HC} = 250\Omega / 2W$

## 8.3 Safety features

### 8.3.1 Undervoltage lockout

In order to avoid startup of the Boost controller at low supply voltage an undervoltage lockout function is implemented. The boost controller only turns on when the voltage at pin UVLO exceeds  $V_{UVLO}$ . Once the boost controller is turned on a current source  $I_{UVLO\_Hyst}$  is activated which increases the UVLO voltage and so shifts the turn off voltage level.

Figure 12. Undervoltage lockout



Following equations can be derived for adjusting the threshold voltages:

$$\text{Undervoltage lockout HIGH level: } V_{DDH\_UVH} = V_{UVLO} \times \left(1 + \frac{R_{UVLO1}}{R_{UVLO2}}\right) \quad (\text{EQ 4})$$

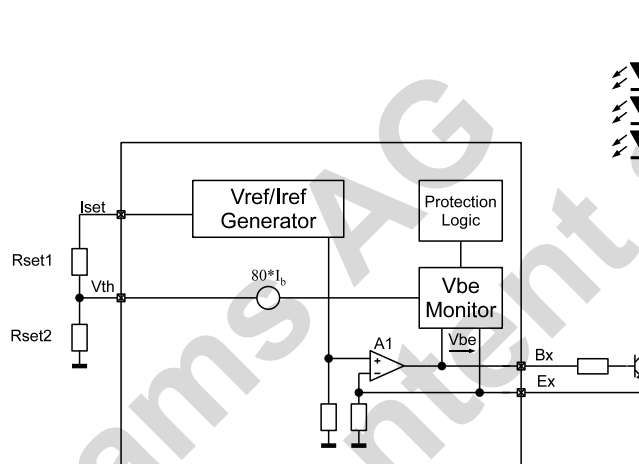
$$\text{Undervoltage lockout LOW level: } V_{DDH\_UVL} = V_{UVLO} \times \left(1 + \frac{R_{UVLO1}}{R_{UVLO2}}\right) - I_{UVLO} \times R_{UVLO1} \quad (\text{EQ 5})$$

### 8.3.2 Overtemperature Shutdown

If the device temperature reaches  $T_{OFF}$  the boost controller and all current outputs are turned off. After the temperature has decreased by  $T_{hyst}$  all blocks are turned on again.

### 8.3.3 Short LED protection

Figure 13. Short Led protection



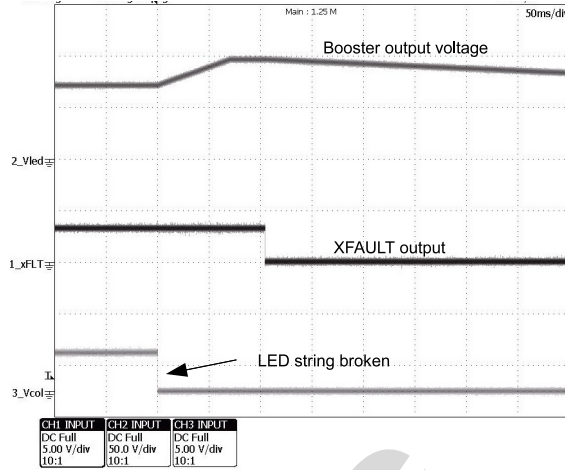
A built in short protection comparator is monitoring the junction temperature  $T_J$  of the external bipolar transistors by measuring the base-emitter voltage  $V_{BE}$ .

$$V_{BE} = 1,2V - 0,002 \times T_J \quad T_J \dots \text{junction temperature in K} \quad (\text{EQ 6})$$

When the measured  $V_{BE}$  gets lower than the voltage applied at pin  $V_{th}$  an overtemperature and hence an short LED condition is detected. Subsequently the fault output is activated ( $xFAULT = 0$ ) and the corresponding output is deactivated.

### 8.3.4 Open LED detection

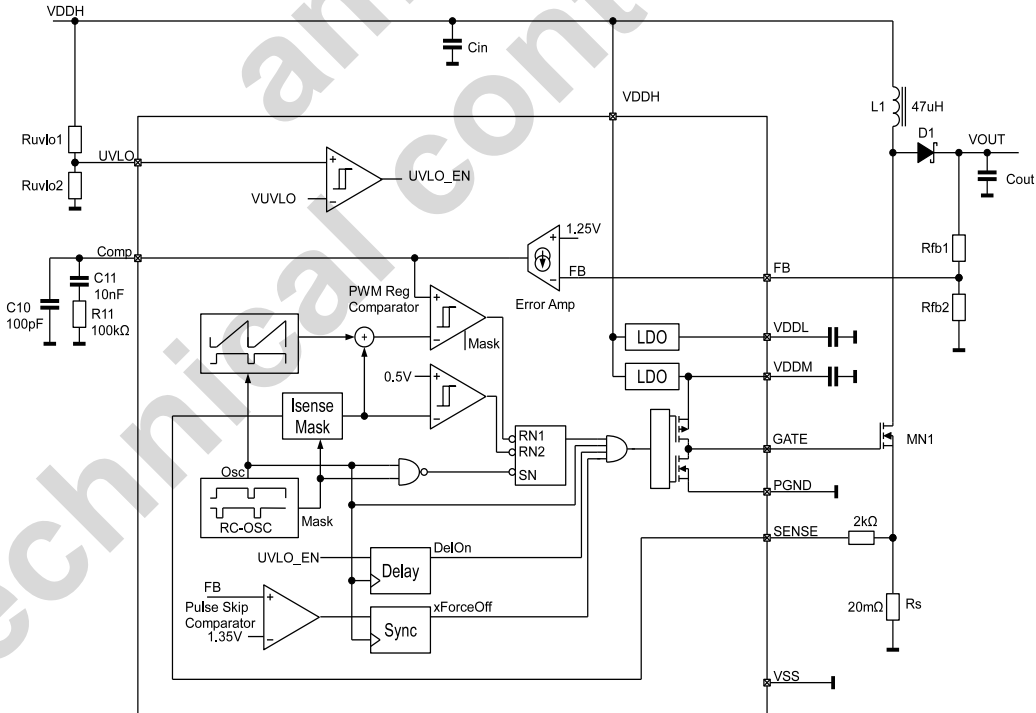
Figure 14. Open Led detection



A broken LED-string is detected during PWM=1. If a LED-string is broken the power supply feedback will increment the IDAC to increase the power supply output voltage. After the IDAC has reached its maximum value, a debounce counter is started. In order to run the debounce counter, the corresponding PWM-signal has to be high for more than 150us. After the debounce counter has counted up for 32ms, the fault output is activated (xFAULT = 0) and the corresponding output is disconnected from the power supply feedback loop.

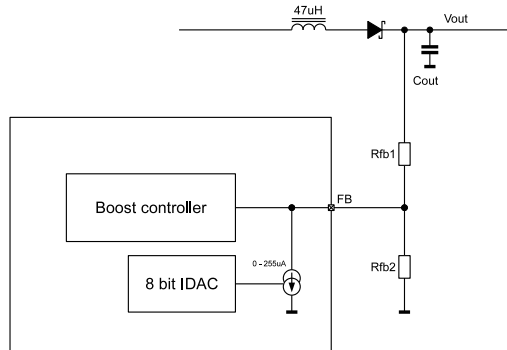
### 8.4 Boost controller

Figure 15. Boost controller



### 8.4.1 Setting the output voltage

Figure 16. Vout setting



According to the requirements of the LED strings, the output voltage  $V_{out}$  is adjusted by the internal power supply feedback

$$\text{between: } V_{OUTmin} = V_{fb} \left( 1 + \frac{R_{fb1}}{R_{fb2}} \right) \quad \text{and} \quad V_{OUTmax} = V_{fb} \left( 1 + \frac{R_{fb1}}{R_{fb2}} \right) + 255\mu A \cdot R_{fb1}$$

Once  $V_{out\_min}$  and  $V_{out\_max}$  is known the external resistors can be calculated:

$$R_{fb1} = \frac{(V_{OUTmax} - V_{OUTmin})}{255\mu A} \quad (\text{EQ 7})$$

$$R_{fb2} = \frac{V_{fb} R_{fb1}}{(V_{OUTmin} - V_{fb})} \quad (\text{EQ 8})$$

**Note:** The overall resistance should be in the range of 100k $\Omega$  to 200k $\Omega$  to avoid any noise issues. Keep FB-line as short as possible.

### 8.4.2 Continuous Conduction Mode (CCM)

For normal operation the converter should stay in continuous conduction mode, to ensure that the inductor value must be bigger than LCRIT.

$$L_{CRIT} = \frac{\left(1 - \frac{V_{IN}}{V_{OUT} + V_D}\right) \times V_{IN}^2 \times R}{2 \times f_{SW} \times (V_{OUT} + V_D)^2} \quad (EQ 9)$$

#### Where:

V<sub>IN</sub> ... Input voltage at VDDH

V<sub>OUT</sub> ... Output voltage

V<sub>D</sub> ... Diode forward voltage at D1

f<sub>SW</sub> ... Switching frequency

R ... Load resistor, should be calculated with minimum current load R = V<sub>OUT</sub> / I<sub>OUT\_min</sub>

I<sub>OUT\_min</sub> ... Minimum output current (e.g. for LED driver only one LED string is on)

### 8.4.3 Duty Cycle

Within CCM, the well known relation between input and output voltage is deripied in the following equation:

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{1}{1 - D} \quad (EQ 10)$$

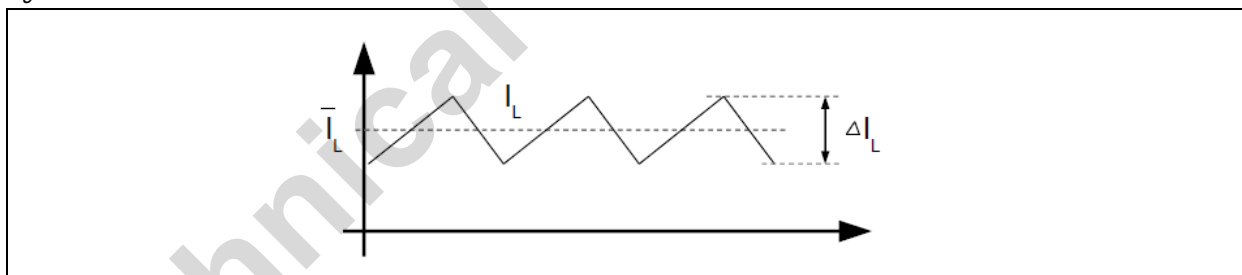
this means for the duty cycle:

$$D = 1 - \frac{V_{IN}}{V_{OUT} + V_D} \quad (EQ 11)$$

### 8.4.4 Inductor Current

The inductor current varies during a switching cycle. This variation can be expressed by the mean value of the inductor current and the delta rise/fall current within each cycle (see Figure 17).

Figure 17. Inductor Current



Mean inductor current:

$$\bar{I}_L = \frac{I_{OUT}}{1 - D} \quad (EQ 12)$$

Delta inductor current:

$$\Delta I_L = \frac{D \times V_{IN}}{f_S \times L} \quad (EQ 13)$$

Peak current:

$$I_{pk} = \bar{I}_L + \frac{\Delta I_L}{2} = \frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \quad (\text{EQ 14})$$

RMS inductor current:

$$I_{RMS} = \sqrt{\bar{I}_L^2 + \left(\frac{1}{12} \times \Delta I_L\right)^2} \quad (\text{EQ 15})$$

This peak current is flowing through MN1 during phase 1 and through D1 during phase 2 of each cycle. Therefore this peak current is important for a proper diode, MOSFET and inductor selection.

**Note:** The saturation current of the inductor should be about 20 to 30% larger than the peak current

#### 8.4.5 Input Capacitor

The input capacitor has to supply the delta inductor current and it should be selected according to:

$$C_{IN} > \frac{\Delta I_L}{4 \times \Delta V_{IN} \times f_{SW}} \quad (\text{EQ 16})$$

$$ESR < \frac{\Delta V_{IN}}{2 \times \Delta I_L} \quad (\text{EQ 17})$$

#### 8.4.6 Output Capacitor

The output capacitor must be chosen according to the max allowable output ripple at high load.

$$C_{OUT} > \frac{I_{OUT-max} \times D}{\Delta V_{OUT} \times f_{SW}} \quad (\text{EQ 18})$$

$$ESR < \frac{\Delta V_{OUT}}{\left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times L \times f_{SW}}\right)} \quad (\text{EQ 19})$$

#### 8.4.7 Current Sense Resistor

$$R_{S-max} = \frac{V_{SENSE}}{\bar{I}_L + 0,5 \times \Delta I_L} \quad (\text{EQ 20})$$

$$P_{RS} = I_{L-rms}^2 \times R_S \times D \quad (\text{EQ 21})$$

**Note:** Low inductance, specific designed current sensing resistors should be used, e.g. Stackpole Electronics CSR/CSRN series of sensing resistors with less than 0.2nH (typ.).

#### 8.4.8 Compensation Network

A typical choice for values of the compensation network is C10 = 100pF, C11 = 10nF, R11 = 100KΩ. Use these values as initial choice and evaluate the transient response of the system to verify the behavior at output load change.



## 9 Package Drawings and Markings

Figure 18. TQFP-32 Marking



Table 4. Packaging Code

YY	WW	G	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

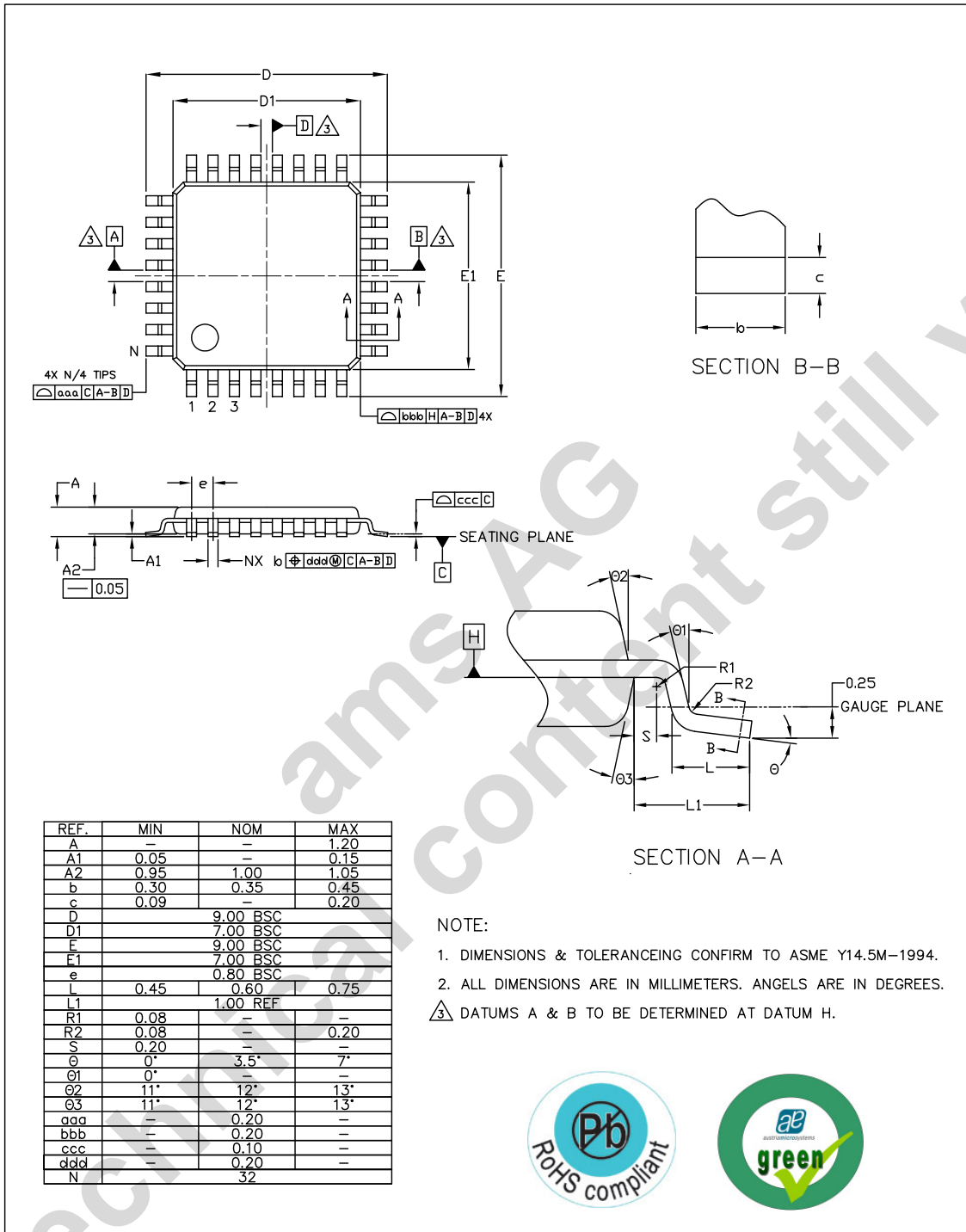
Figure 19. SOIC-28 Marking



Table 5. Packaging Code

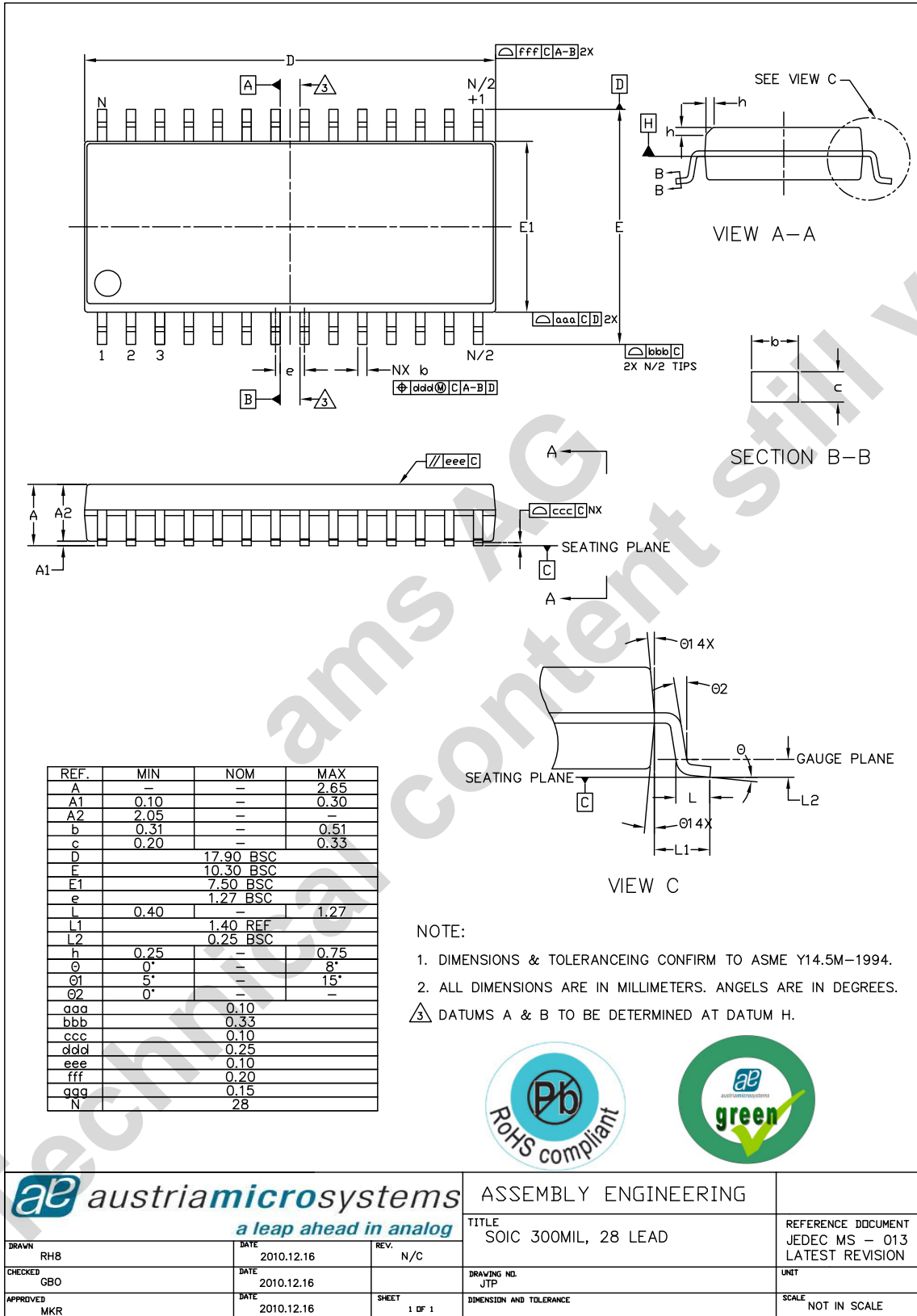
YY	WW	R	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

Figure 20. TQFP-32 Package



austriamicrosystems <i>a leap ahead in analog</i>		ASSEMBLY ENGINEERING		
DRAWN RHB	DATE 2010.12.17	REV. N/C	TITLE TQFP 7x7x1.0mm, 32 LEAD,	REFERENCE DOCUMENT JEDEC MS - 026 LATEST REVISION
CHECKED GBO	DATE 2010.12.17		DRAWING NO. BPX	UNIT
APPROVED MKR	DATE 2010.12.17	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

Figure 21. SOIC-28 Package



## 10 Ordering Information

The devices are available as the standard products shown in [Table 6](#).

Table 6. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS3833-ZTQT	AS3833		Tape & Reel	TQFP-32
AS3833-ZSOT	AS3833		Tape & Reel	SOIC-28

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