DRAM

1 MEG x 1 DRAM

FAST PAGE MODE

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883

FEATURES

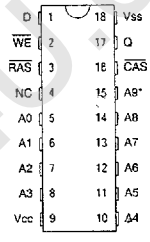
- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- Optional PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Specifications guaranteed over full military temperature range (-55°C to +125°C)

OPTIONS

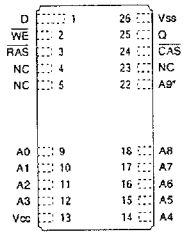
	MARKING	
• Timing		
80ns access	- 8	
100ns access	-10	
120ns access	-12	
• Packages		
Ceramic DIP (300 mil)	C	No. 101
Ceramic LCC	EC	No. 202

PIN ASSIGNMENT (Top View)

18-Pin DIP (D-6)



20-Pin LCC



*Address not used for $\overline{RAS}$-ONLY REFRESH

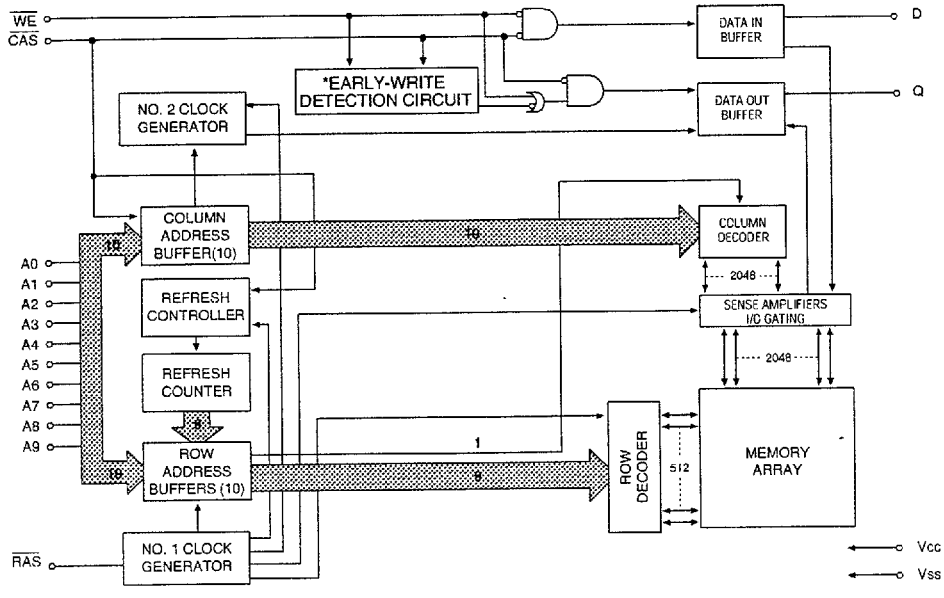
GENERAL DESCRIPTION

The AS4C1024 883C is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1-bit configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output (Q) remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches Q, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1.5V to +7.0V
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation 1W
Lead Temperature (soldering 5 seconds) ..... 270°C
Junction Temperature (Tj) ..... +175°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (-55°C ≤ T_C ≤ +125°; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	Vcc+.5	V	
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-.5	0.8	V	
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-5	5	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-5	5	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	3	3	3	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V; all other inputs = Vcc -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	90	80	70	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		7	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ +125°; Vcc = 5V ±10%)

AC CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-WRITE cycle time	^tRWC	175		210		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	70		85		100		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	25	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		12		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		12		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

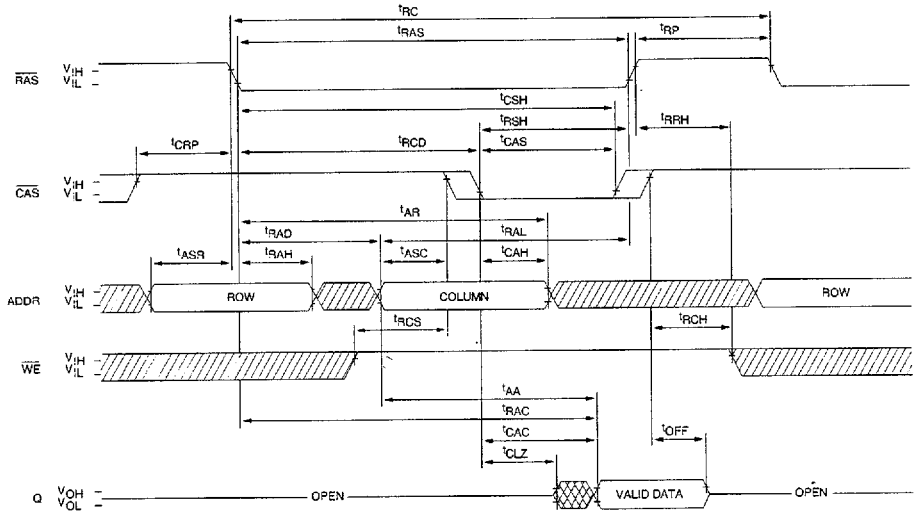
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T C ≤ 125°C, VCC = 5.0V ±10%)

AC CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WRITE command hold time	^{t}WCH	15		20		25		ns	
WRITE command hold time (referenced to RAS\ )	^{t}WCR	60		70		80		ns	
WRITE command pulse width	^{t}WP	15		20		25		ns	
WRITE command to RAS\ lead time	^{t}RWL	20		25		30		ns	
WRITE command to CAS\ lead time	^{t}CWL	20		25		30		ns	
Data-in set-up time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	15		20		25		ns	22
Data-in hold time referenced to RAS\	^{t}DHR	60		70		80		ns	
RAS\ to WRITE delay	^{t}RWD	80		100		120		ns	21
Column address to WE\ delay time	^{t}AWD	40		50		60		ns	21
CAS\ to WRITE delay	^{t}CWD	20		25		30		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	
Refresh period (512 cycles)	^{t}REF		8		8		8	ms	
RAS\ to CAS\ precharge time	^{t}RPC	0		0		0		ns	
CAS\ set-up time (CAS-BEFORE-RAS REFRESH)	^{t}CSR	10		10		10		ns	5
CAS\ hold time (CAS-BEFORE-RAS REFRESH)	^{t}CHR	15		20		25		ns	5
WE\ set-up time before RAS\ low	^{t}WRP	10		10		10		ns	9,10,11
WE\ hold time after RAS\ low CAS\ before RAS\ refresh	^{t}WPH	10		10		10		ns	9,10,11

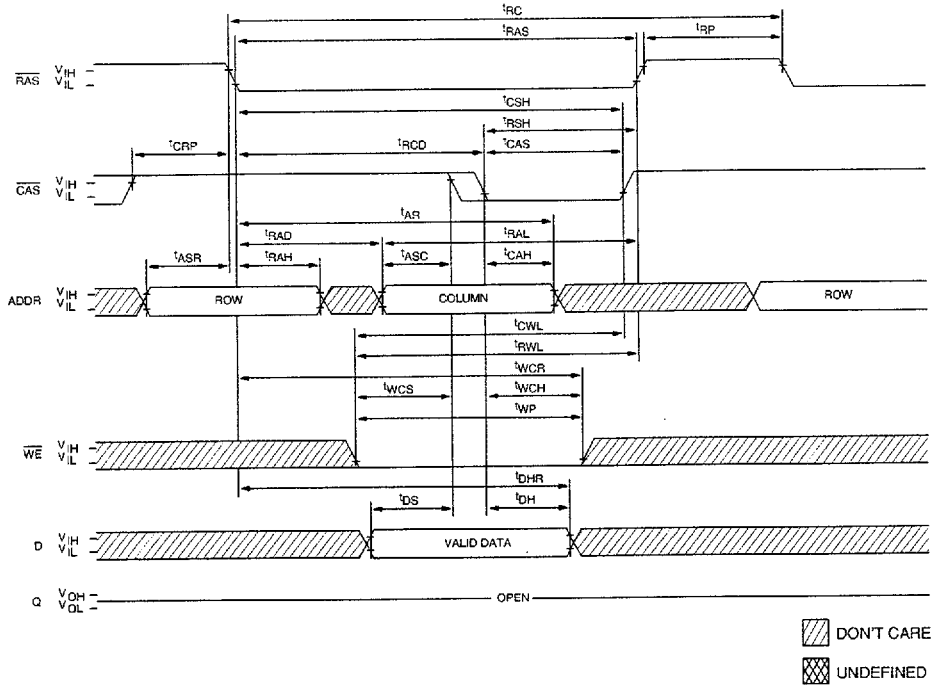
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled, not 100% tested. Capacitance is measured with Vcc = 5V, f = 1 MHz at less than 50mVrms; T_A = 25°C ±3°C; Vbias = 2.4V applied to each input and output individually with remaining inputs and outputs open.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ +125°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh only cycles or CBR refresh cycle (WE\ held high) before proper device operation is assured.
8. AC characteristics assume transition time (^tT) = 5ns. This parameter is not measured.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output (Q) is High-Z.
12. If $\overline{CAS}$ = VIL, Q may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX).
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves open circuit condition. ^tOFF (MAX) is not referenced to VOH or VOL.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the Q (at access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.

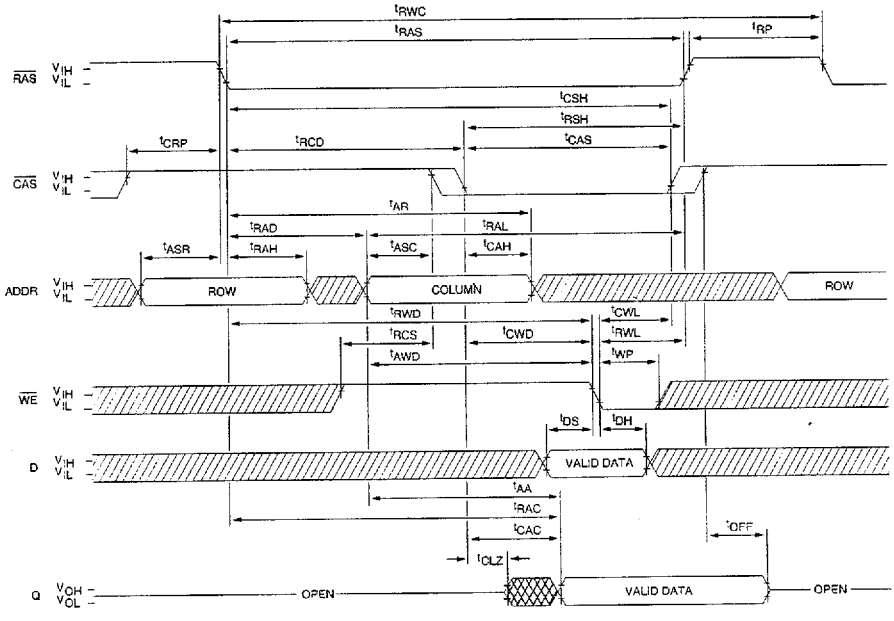
READ CYCLE



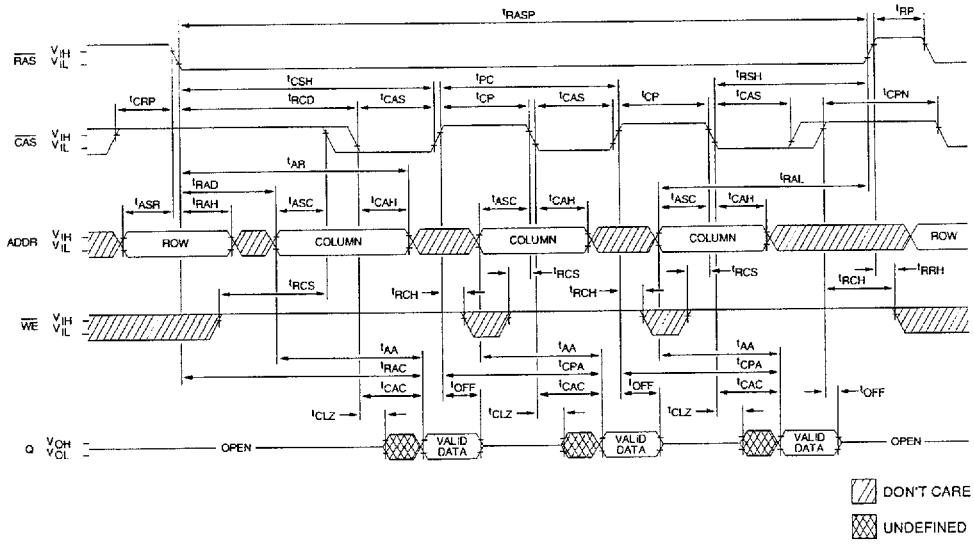
EARLY-WRITE CYCLE



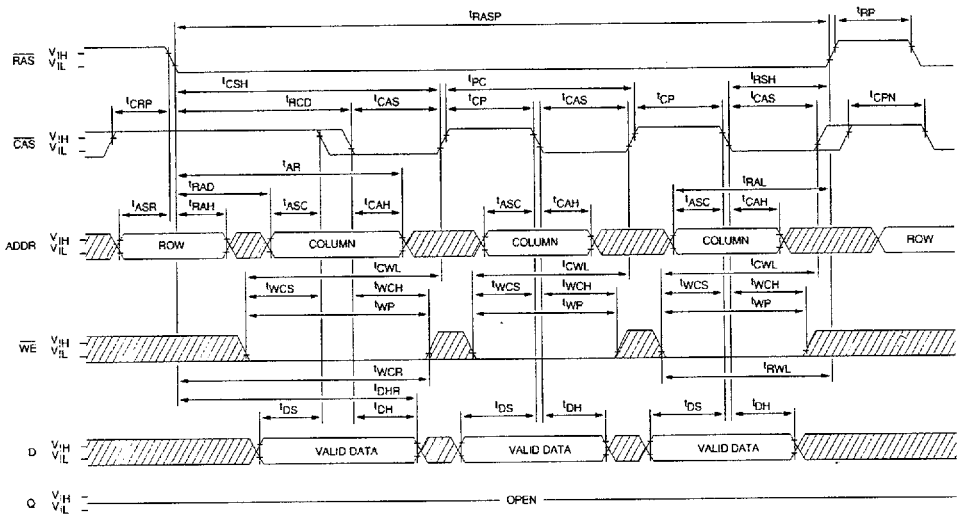
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



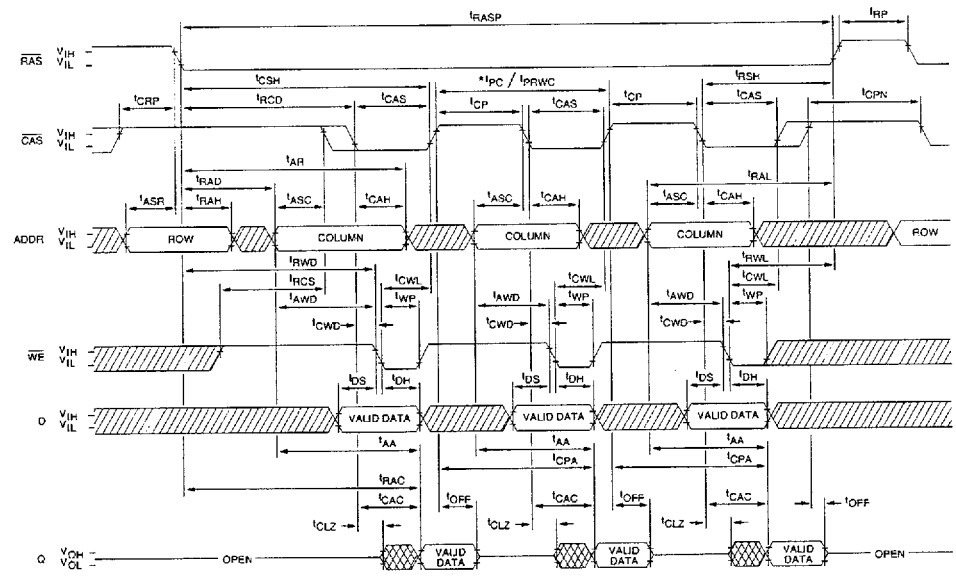
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



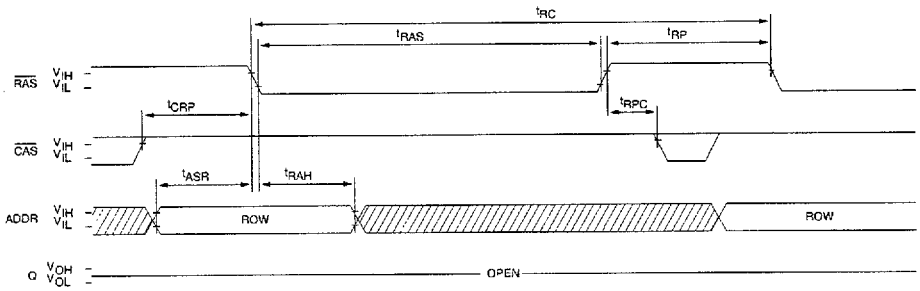
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



*tPC = LATE-WRITE cycle
tPRWC = FAST RMW cycle

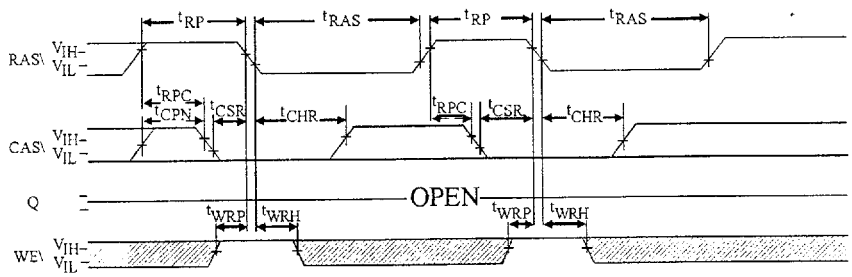
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A0-A8; A9 and $\overline{WE}$ = DON'T CARE)



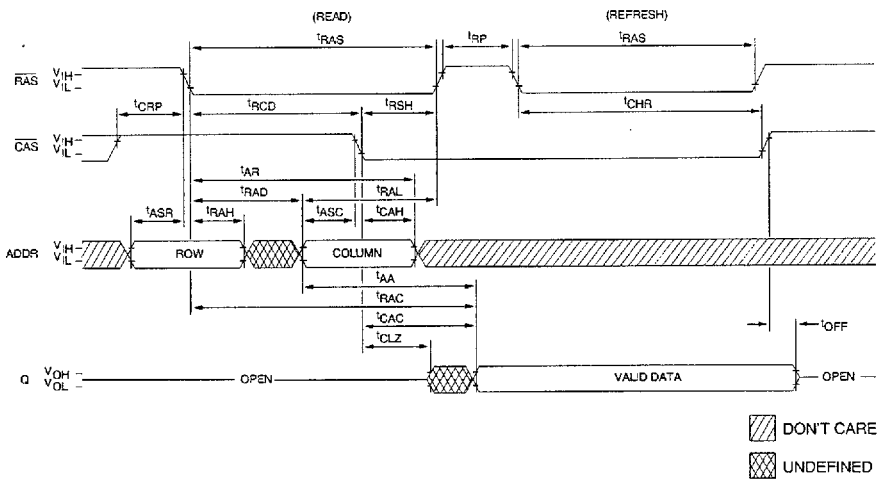
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A0-A9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [23]

($\overline{WE}$ = HIGH)



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.