



32Mx64 DDR2 SDRAM INTEGRATED Plastic Encapsulated Microcircuit

FEATURES

- DDR2 Data rate = 667, 533, 400
- Available in Industrial, Enhanced and Military Temp
- Package:
 - 255 Plastic Ball Grid Array (PBGA), 25 x 32mm
 - 1.27mm pitch
- Differential data strobe (DQS, DQS#) per byte
- Internal, pipelined, double data rate architecture
- 4-bit prefetch architecture
- DLL for alignment of DQ and DQS transitions with clock signal
- Four internal banks for concurrent operation (Per DDR2 SDRAM Die)
- Programmable Burst lengths: 4 or 8
- Auto Refresh and Self Refresh Modes
- On Die Termination (ODT)
- Adjustable data – output drive strength
- 1.8V ±0.1V power supply and I/O (VCC/VCCQ)
- Programmable CAS latency: 3, 4, 5, or 6
- Posted CAS additive latency: 0, 1, 2, 3 or 4
- Write latency = Read latency - 1* tCK
- Organized as 32M x 64
- Weight: AS4DDR232M64PBG ~ 3.5 grams typical

BENEFITS

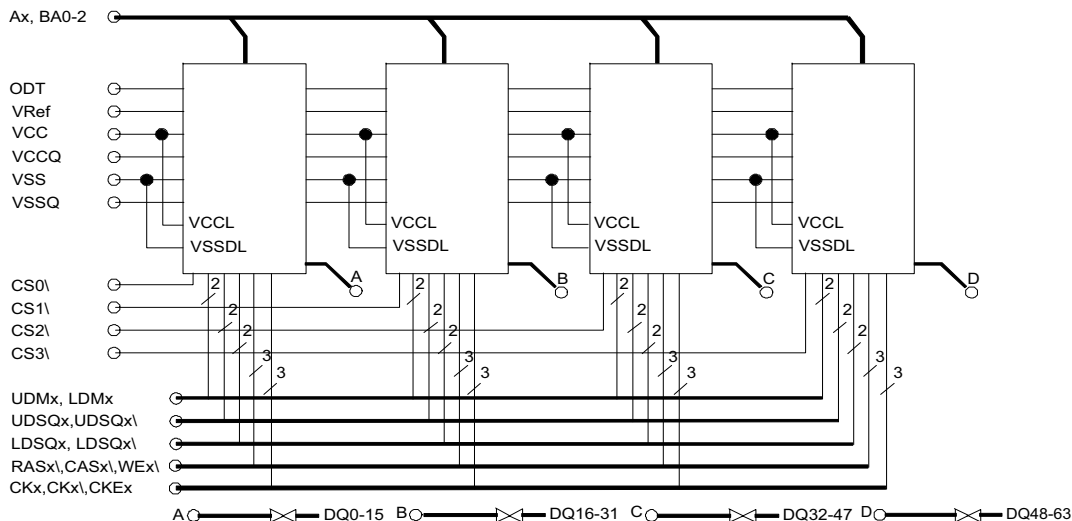
- SPACE conscious PBGA defined for easy SMT manufacturability (50 mil ball pitch)
- Reduced part count
- 47% I/O reduction vs Individual CSP approach
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Upgradable to 64M x 64 density (consult factory for info on AS4DDR264M64PBG)

Configuration Addressing

| Parameter | 32 Meg x 72 |
|----------------|----------------------|
| Configuration | 8 Meg x 16 x 4 Banks |
| Refresh Count | 8K |
| Row Address | 8K (A0-A12) |
| Bank Address | 4 (BA0-BA1) |
| Column Address | 1K (A0-A9) |

NOTE: Self Refresh Mode available on Industrial and Enhanced temp. only

FUNCTIONAL BLOCK DIAGRAM





IPEM
2.1 Gb SDRAM-DDR2
Austin Semiconductor, Inc. AS4DDR232M64PBG

SDRAM-DDRII PINOUT TOP VIEW

| | | | | | | | | | | | | | | | | | |
|---|-------|-------|------|-------|-------|--------|--------|--------|------|--------|--------|-------|------|------|-------|-------|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| A | | DQ0 | DQ14 | DQ15 | VSS | VSS | A9 | A10 | A11 | A8 | VCCQ | VCCQ | DQ16 | DQ17 | DQ31 | VSS | A |
| B | DQ1 | DQ2 | DQ12 | DQ13 | VSS | VSS | A0 | A7 | A6 | A1 | VCC | VCC | DQ18 | DQ19 | DQ29 | DQ30 | B |
| C | DQ3 | DQ4 | DQ10 | DQ11 | VCC | VCC | A2 | A5 | A4 | A3 | VSS | VSS | DQ20 | DQ21 | DQ27 | DQ28 | C |
| D | DQ6 | DQ5 | DQ8 | DQ9 | VCCQ | VCCQ | A12/NC | DNU | DNU | DNU | VSS | VSS | DQ22 | DQ23 | DQ26 | DQ25 | D |
| E | DQ7 | LDM0 | VCC | UDM0 | UDQS3 | LDQS0 | UDQS0 | BA0 | BA1 | LDQS1 | UDQS1 | VREF | LDM1 | VSS | NC | DQ24 | E |
| F | CAS0\ | WE0\ | VCC | CLK0 | LDQS3 | UDQS3\ | LDQS0\ | UDQS0\ | NC | UDQS1\ | LDQS1\ | RAS1\ | WE1\ | VSS | UDM1 | CLK1 | F |
| G | CS0\ | RAS0\ | VCC | CKE0 | CLK0\ | LDQS3\ | VSSQ | VSSQ | VSSQ | VSSQ | NC | CAS1\ | CS1\ | VSS | CLK1\ | CKE1 | G |
| H | VSS | VSS | VCC | VCCQ | VSS | NC | VSSQ | VSSQ | VSSQ | VSSQ | NC | VCC | VSS | VSS | VCCQ | VCC | H |
| J | VSS | VSS | VCC | VCCQ | VSS | NC | VSSQ | VSSQ | VSSQ | VSSQ | NC | VCC | VSS | VSS | VCCQ | VCC | J |
| K | CLK3\ | CKE3 | VCC | CS3\ | NC | NC | VSSQ | VSSQ | VSSQ | VSSQ | NC | CLK2\ | CKE2 | VSS | RAS2\ | CS2\ | K |
| L | NC | CLK3 | VCC | CAS3\ | RAS3\ | ODT | NC | NC | NC | LDQS2\ | UDQS2\ | LDQS2 | CLK2 | VSS | WE2\ | CAS2\ | L |
| M | DQ56 | UDM3 | VCC | WE3\ | LDM3 | NC | NC | NC | NC | NC | NC | NC | UDM2 | VSS | LDM2 | DQ39 | M |
| N | DQ57 | DQ58 | DQ55 | DQ54 | NC | NC | NC | NC | NC | NC | NC | UDQS2 | DQ41 | DQ40 | DQ37 | DQ38 | N |
| P | DQ60 | DQ59 | DQ53 | DQ52 | VSS | VSS | NC | NC | NC | NC | VCC | VCC | DQ43 | DQ42 | DQ36 | DQ35 | P |
| R | DQ62 | DQ61 | DQ51 | DQ50 | VCC | VCC | NC | NC | NC | NC | VSS | VSS | DQ45 | DQ44 | DQ34 | DQ33 | R |
| T | VSS | DQ63 | DQ49 | DQ48 | VCCQ | VCCQ | NC | NC | NC | NC | VSS | VSS | DQ47 | DQ46 | DQ32 | VCC | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

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| | | | | | | | | | |
|--|------------|--|-------------|--|-------------|--|-------------|--|---------|
| | Ground | | Array Power | | D/Q Power | | Address | | Data IO |
| | Level REF. | | CNTRL | | ADDRESS-DNU | | UNPOPULATED | | NC |

Note 1: Ball location D9 is reserved for future use on 64M x 64 in which it will be BANKSELECT2 'BA2'. Ball D10 is reserved for future use on 128M x 64 in which it will be A13.

Important Note: It is recommended that no bias be applied to either the DNU or NC pins. They are not connected to any die pad but DNU & NC pins may be shorted together in package.



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2.1 Gb SDRAM-DDR2

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| BGA Locations | Symbol | Type | Description |
|--|-------------|--------------|---|
| L6 | ODT | CNTL Input | On-Die-Termination: Registered High enables on data bus termination |
| F4, F16, G5, G15, K12 L13, L2, K1 | CKx, CKx\ | CNTL Input | Differential input clocks, one set for each x16bits |
| G4, G16, K13, K2 | CKEx | CNTL Input | Clock enable which activates all on silicon clocking circuitry |
| G1, G13, K16, K4 | CSx\ | CNTL Input | Chip Selects, one for each 16 bits of the data bus width |
| F12, G2, K15, L5 | RASx\ | CNTL Input | Command input which along with CAS\, WE\ and CS\ define operations |
| F1, G12, L16, L4 | CASx\ | CNTL Input | Command input which along with RAS\, WE\ and CS\ define operations |
| F2, F13, L15, M4 | Wex\ | CNTL Input | Command input which along with RAS\, CAS\ and CS\ define operations |
| E4, F15, M13, M2 | UDMx | CNTL Input | One Data Mask cntl. for each upper 8 bits of a x16 word |
| E2, E13, M15, M5 | LDMx | CNTL Input | One Data Mask cntl. For each lower 8 bits of a x16 word |
| E5, E7, E11, N12 | UDQSx | CNTL Input | Data Strobe input for upper byte of each x16 word |
| F6, F8, F10, L11 | UDQSx\ | CNTL Input | Differential input of UDQSx, only used when Differential DQS mode is enabled |
| E6, E10, F5, L12 | LDQSx | CNTL Input | Data Strobe input for lower byte of each x16 word |
| F7, F11, G6, L10 | LDQSx\ | CNTL Input | Differential input of LDQSx, only used when Differential DQS mode is enabled |
| A7, A8, A9, A10, B7, B8, B9, B10, C7, C8, C9, C10, D7 | Ax | Input | Array Address inputs providing ROW addresses for Active commands, and the column address and auto precharge bit (A10) for READ/WRITE commands |
| D8, D9, D10 | DNU | Future Input | |
| E8, E9 | BA0, BA1 | Input | Bank Address inputs |
| A2, A3, A4, A13, A14, A15, B1, B2, B3, B4, B13, B14, B15, B16, C1, C2, C3, C4, C13, C14, C15, C16, D1, D2, D3, D4, D13, D14, D15, D16, E1, E16, M1, M16, N1, N2, N3, N4, N13, N14 N15, N16, PP1, P2, P3, P4, P13, P14, P15, P16, R1, R2, R3, R4, R13, R14 R15, R16, T2, T3, T4, T13 T14, T15 | DQx | Input/Output | Data bidirectional input/Output pins |
| E12 | Vref | Supply | SSTL_18 Voltage Reference |
| B11, B12, C5, C6, E3, F3, G3, H3, H12, H16, J3, J12, J16, K3, L3, M3, P11, P12, R5, R6, T16 | VCC | Supply | Core Power Supply |
| A11, A12, D5, D6, H4, H15, J4, J15, T5, T6 | VCCQ | Supply | I/O Power |
| A5, A6, A16, B5, B6, C11, C12, D11, D12, E14, F14, G14, H1, H2, H14, J1, J2, J5, J13, J14, K14, L14, M14, P5, P6, R11, R12, T1, T11, T12 | VSS | Supply | Core Ground return |
| G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10 | VSSQ | Supply | I/O Ground return |
| E15, F9, G11, H6, H11, J6, J11, K11, L1, L8, L9, N7, N8, N9, N10, P7, P8, P9, P10, R7, R8, R9, R10, T7, T8, T9, T10, K5, K6, L7, M6, M7, M8, M9, M10, M11, M12, N5, N6, N11 | NC | | No connection |
| A1 | UNPOPULATED | | Unpopulated ball matrix location (location registration aid) |



DESCRIPTION

The 2.1Gb DDR2 SDRAM, a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. Each of the five chips in the MCP are internally configured as 4-bank DRAM. The block diagram of the device is shown in Figure 2. Ball assignments and are shown in Figure 3.

The 2.1Gb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the x64 DDR2 SDRAM effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. There are strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The MCP DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

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Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write.

An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

GENERAL NOTES

- The functionality and the timing specifications discussed in this data sheet are for the DLLenabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as $i^{\circ}DQ_{j\pm}$. The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, each chip is divided into 2 bytes, the lower byte and upper byte. For the lower byte (DQ0[°]CDQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8[°]CDQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

INITIALIZATION

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for power up and initialization and is shown in Figure 4 on page 8.

1. Applying power; if CKE is maintained below $0.2 \times V_{CCQ}$, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined, I/Os and outputs must be less than V_{CCQ} during voltage ramp time to avoid DDR2 SDRAM device latch-up). At least one of the



following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as V_{CC} , V_{CCQ} , V_{REF} , and V_{TT} are between their minimum and maximum values as stated in Table 20);

A. (single power source) The V_{CC} voltage ramp from 300mV to V_{CC} (MIN) must take no longer than 200ms; during the V_{CC} voltage ramp, $V_{CC} - V_{CCQ} \pm 0.3V$. Once supply voltage ramping is complete (when V_{CCQ} crosses V_{CC} (MIN)), Table 20 specifications apply.

- V_{CC} , V_{CCQ} are driven from a single power converter output
- V_{TT} is limited to 0.95V MAX
- V_{REF} tracks $V_{CCQ/2}$; V_{REF} must be within $\pm 0.3V$ with respect to $V_{CCQ/2}$ during supply ramp time
- $V_{CCQ} \geq V_{REF}$ at all times

B. (multiple power sources) $V_{CC} > V_{CCQ}$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (V_{CCQ} crosses V_{CC} [MIN]). Once supply voltage ramping is complete, Table 20 specifications apply.

- Apply V_{CC} before or at the same time as V_{CCQ} ; V_{CC} voltage ramp time must be $\leq 200ms$ from when V_{CC} ramps from 300mV to V_{CC} (MIN)
- Apply V_{CCQ} before or at the same time as V_{TT} ; the V_{CCQ} voltage ramp time from when V_{CC} (MIN) is achieved to when V_{CCQ} (MIN) is achieved must be $\leq 500ms$; while V_{CC} is ramping, current can be supplied from V_{CC} through the device to V_{CCQ}
- V_{REF} must track $V_{CCQ/2}$, V_{REF} must be within $\pm 0.3V$ with respect to $V_{CCQ/2}$ during supply ramp time; $V_{CCQ} > V_{REF}$ must be met at all times
- Apply V_{TT} ; The V_{TT} voltage ramp time from when V_{CCQ} (MIN) is achieved to when V_{TT} (MIN) is achieved must be no greater than 500ms

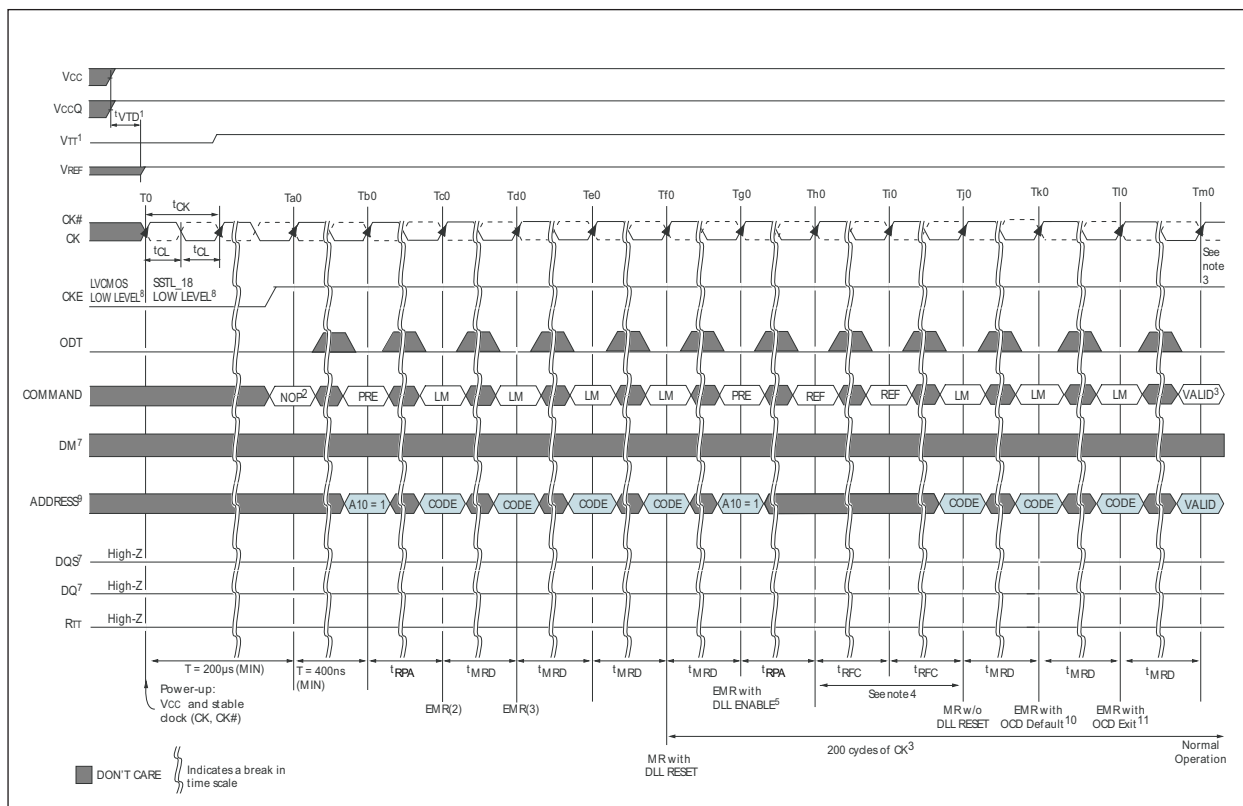
2. For a minimum of 200 μs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
4. Issue an LOAD MODE command to the EMR(2). (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)
5. Issue a LOAD MODE command to the EMR(3). (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
6. Issue an LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 can be set to "0" or "1"; Micron recommends setting them to "0".
7. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1, and BA0.) CKE must be HIGH the entire time.
8. Issue PRECHARGE ALL command.
9. Issue two or more REFRESH commands, followed by a dummy WRITE.



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FIGURE 4 - POWER-UP AND INITIALIZATION

Notes appear on page 7





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NOTES:

1. Applying power; if CKE is maintained below $0.2 \times V_{CCQ}$, outputs remain disabled. To guarantee RTT (ODT resistance) is off, VREF must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined, I/Os and outputs must be less than VCCQ during voltage ramp time to avoid DDR2 SDRAM device latch-up). At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as VCC, VCCQ, VREF, and VTT are between their minimum and maximum values as stated in DC Operating Conditions table):
 - A. (single power source) The VCC voltage ramp from 300mV to VCC(MIN) must take no longer than 200ms; during the VCC voltage ramp, $|V_{CC} - V_{CCQ}| < 0.3V$. Once supply voltage ramping is complete (when VCCQ crosses VCC (MIN)), DC Operating Conditions table specifications apply.
 - VCC, VCCQ are driven from a single power converter output
 - VTT is limited to 0.95V MAX
 - VREF tracks VCCQ/2; VREF must be within $\pm 3V$ with respect to VCCQ/2 during supply ramp time.
 - $V_{CCQ} > V_{REF}$ at all times
 - B. (multiple power sources) VCC e" VCCQ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (VCCQ crosses VCC [MIN]). Once supply voltage ramping is complete, DC Operating Conditions table specifications apply.
 - Apply VCC before or at the same time as VCCQ; VCC voltage ramp time must be $< 200ms$ from when VCC ramps from 300mV to VCC (MIN)
 - Apply VCCQ before or at the same time as VTT; the VCCQ voltage ramp time from when VCC (MIN) is achieved to when VCCQ (MIN) is achieved must be $< 500ms$; while VCC is ramping, current can be supplied from VCC through the device to VCCQ
 - VREF must track VCCQ/2, VREF must be within $\pm 0.3V$ with respect to VCCQ/2 during supply ramp time; $V_{CCQ} > V_{REF}$ must be met at all times
 - Apply VTT; The VTT voltage ramp time from when VCCQ (MIN) is achieved to when VTT (MIN) is achieved must be no greater than 500ms
2. For a minimum of 200 μs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
 3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command/
 4. Issue an LOAD MODE command to the EMR(2). (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)
 5. Issue a LOAD MODE command to the EMR(3). (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
 6. Issue an LOAD MODE command to the EMR to enable DLL. To issue a DLLENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 can be set to "0" or "1"; Micron recommends setting them to "0."
 7. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1, and BA0.) CKE must be HIGH the entire time.
 8. Issue PRECHARGE ALL command.
 9. Issue two or more REFRESH commands, followed by a dummy WRITE.
 10. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
 11. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters.
 12. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters.
 13. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
 14. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters.
 15. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. The DDR2 SDRAM is now initialized and ready for normal operation 200 clocks after DLL RESET (in step 7).



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MODE REGISTER (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CL, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 5. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the command is issued.

The mode register is programmed via the LM command (bits BA1–BA0 = 0, 0) and other bits (M12–M0) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is selfclearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

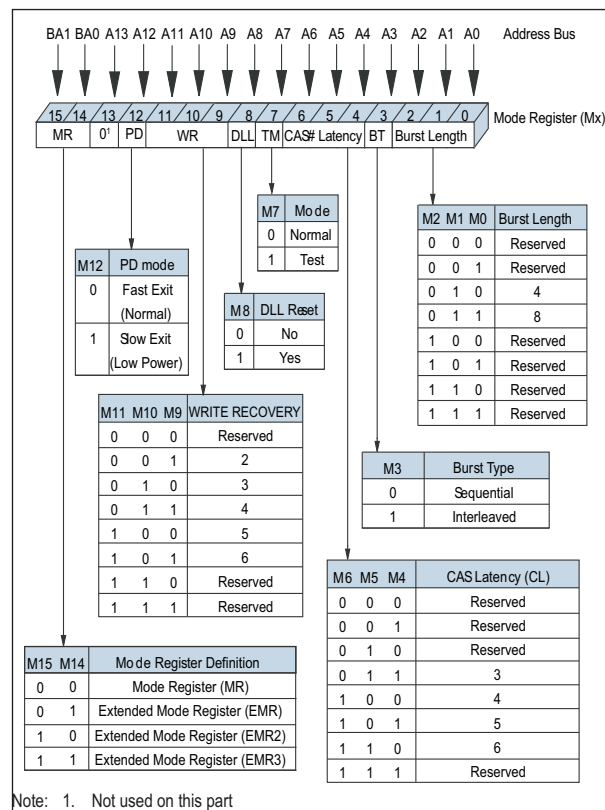
The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time tMRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

BURST LENGTH

Burst length is defined by bits M0–M3, as shown in Figure 5. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–Ai when BL = 4 and by A3–Ai when BL = 8 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

FIGURE 5 – MODE REGISTER (MR) DEFINITION



BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 5. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 2. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.



TABLE 2 - BURST DEFINITION

| Burst Length | Starting Column Address | | Order of Accesses Within a Burst | | |
|--------------|-------------------------|-----------|----------------------------------|--------------------|-----------------|
| | | | Type = Sequential | Type = Interleaved | |
| 4 | A1 | A0 | | | |
| | 0 | 0 | 0-1-2-3 | 0-1-2-3 | |
| | 0 | 1 | 1-2-3-0 | 1-0-3-2 | |
| | 1 | 0 | 2-3-0-1 | 2-3-0-1 | |
| | 1 | 1 | 3-0-1-2 | 3-2-1-0 | |
| 8 | A2 | A1 | A0 | | |
| | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 | 0 | 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | 0 | 1 | 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| | 0 | 1 | 1 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 | 0 | 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | 1 | 1 | 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | 1 | 1 | 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |

NOTES:

- For a burst length of two, A1-Ai select two-data-element block; A0 selects the starting column within the block.
- For a burst length of four, A2-Ai select four-data-element block; A0-1 select the starting column within the block.
- For a burst length of eight, A3-Ai select eight-data-element block; A0-2 select the starting column within the block.
- Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

OPERATING MODE

The normal operating mode is selected by issuing a command with bit M7 set to i^0, i_{\pm} and all other bits set to the desired values, as shown in Figure 5. When bit M7 is "1," no other bits of the mode register are programmed. Programming bit M7 to i^1, i_{\pm} places the DDR2 SDRAM into a test mode that is only used by the manufacturer and should not be used. No operation or functionality is guaranteed if M7 bit is "1."

DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 5. Programming bit M8 to "1" will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of i^0, i_{\pm} after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the 'AC or 'DQSCK parameters.

WRITE RECOVERY

Write recovery (WR) time is defined by bits M9-M11, as shown in Figure 5. The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9-M11) from the last data burst.

WR values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9-M11. The user is required to program the value of WR, which is calculated by dividing iWR (in ns) by iCK (in ns) and rounding up a non integer value to the next integer; $WR [\text{cycles}] = iWR [\text{ns}] / iCK [\text{ns}]$. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

POWER-DOWN MODE

Active power-down (PD) mode is defined by bit M12, as shown in Figure 5. PD mode allows the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode.

When bit M12 = 0, standard active PD mode or "fast-exit" active PD mode is enabled. The 'XARD parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode or "slowexit" active PD mode is enabled. The 'XARD parameter is used for slow-exit active PD exit timing. The DLL can be enabled, but "frozen" during active PD mode since the exit-to-READ command timing is relaxed. The power difference expected between PD normal and PD low-power mode is defined in the Icc table.



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CAS LATENCY (CL)

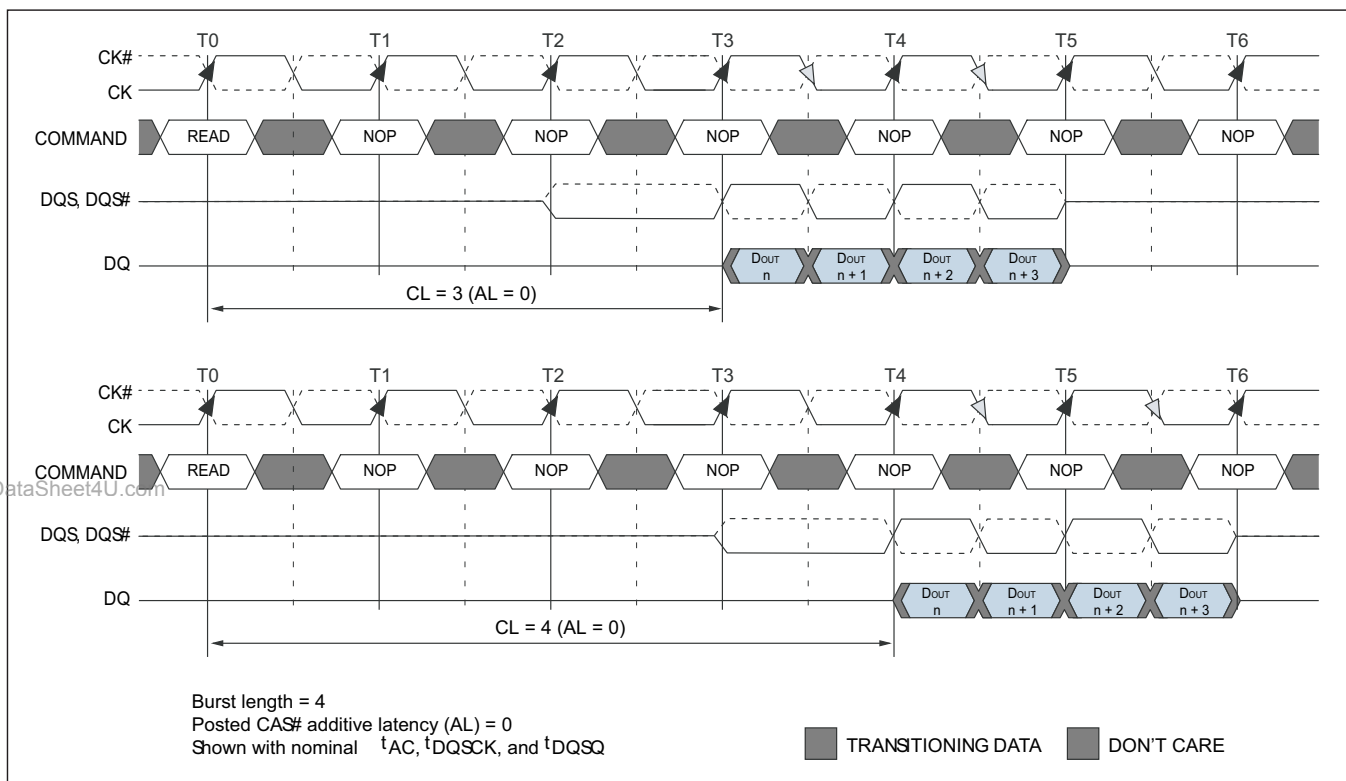
The CAS latency (CL) is defined by bits M4-M6, as shown in Figure 5. CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, or 6 clocks, depending on the speed grade option being used.

DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to tRCD (MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks.

Examples of CL = 3 and CL = 4 are shown in Figure 6; both assume AL = 0. If a READ command is registered at clock edge n , and the CL is m clocks, the data will be available nominally coincident with clock edge $n+m$ (this assumes $AL = 0$).

FIGURE 6 - CAS LATENCY (CL)





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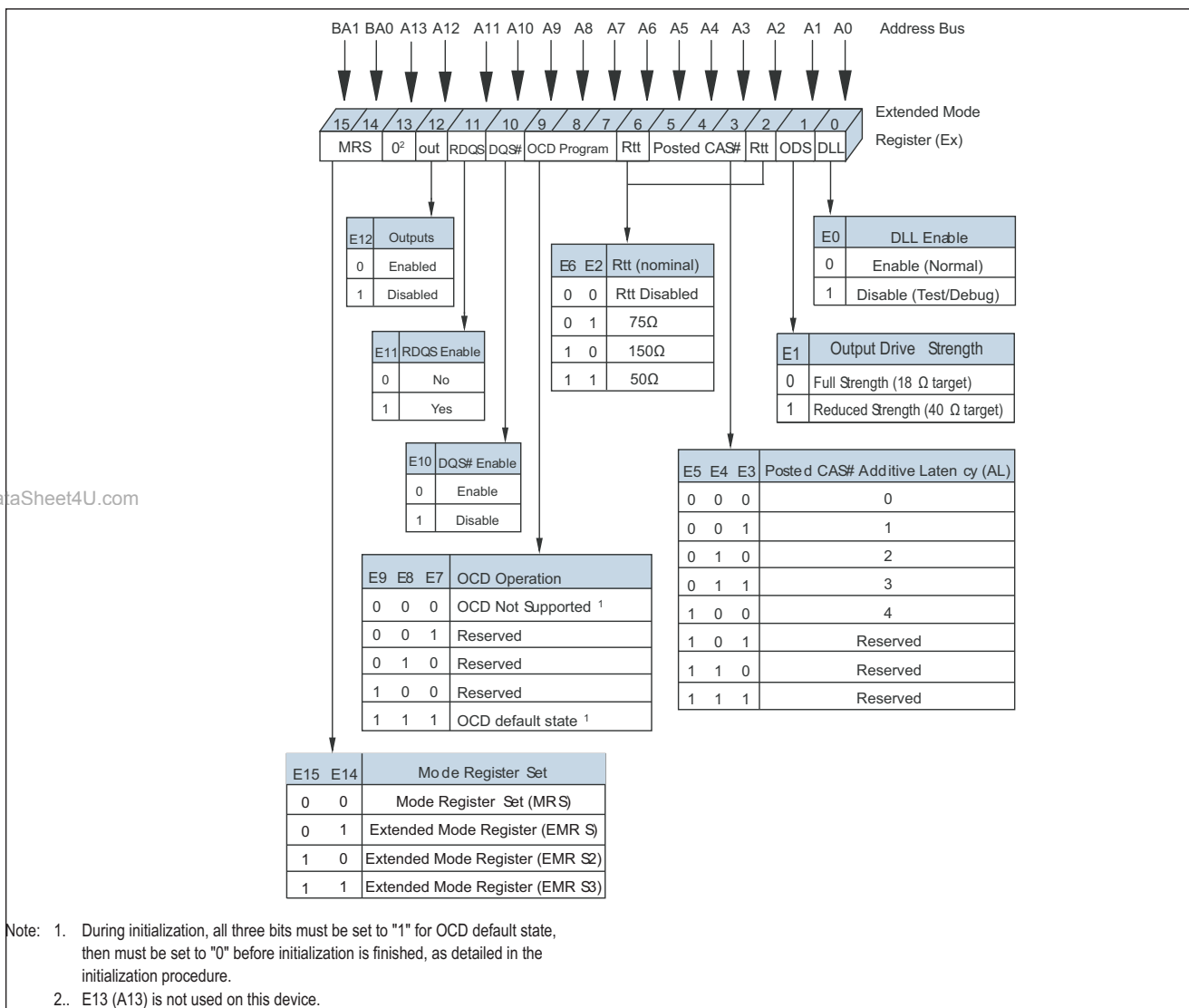
EXTENDED MODE REGISTER (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on die termination (ODT) (RTT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 7. The EMR is programmed via the LOAD MODE (LM) command and will retain the stored information

until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

FIGURE 7 – EXTENDED MODE REGISTER DEFINITION





DLL ENABLE/DISABLE

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 7. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using an LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued, to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the 'AC or 'DQSCK parameters.

OUTPUT DRIVE STRENGTH

The output drive strength is defined by bit E1, as shown in Figure 7. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

DQS# ENABLE/DISABLE

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (E10 = 1), DQS is used in a single ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 7. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during Icc characterization of read current.

ON-DIE TERMINATION (ODT)

ODT effective resistance, $R_{TT}(EFF)$, is defined by bits E2 and E6 of the EMR, as shown in Figure 7. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. R_{TT} effective resistance values of 50Ω, 75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off “sw1,” “sw2,” or “sw3.” The ODT effective resistance value is elected by enabling switch “sw1,” which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω ($R_{TT2}(EFF) = R2/2$). Similarly, if “sw2” is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω ($R_{TT2}(EFF) = R2/2$). Switch “sw3” enables R1 values of 100Ω enabling effective resistance of 50Ω. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control ball is used to determine when $R_{TT}(EFF)$ is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge powerdown modes of operation. ODT must be turned off prior to entering self refresh. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until issuing the EMR command to enable the ODT feature, at which point the ODT ball will determine the $R_{TT}(EFF)$ value. Any time the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled. See “ODT Timing” section for ODT timing diagrams.



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POSTED CAS ADDITIVE LATENCY (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 7. Bits E3–E5 allow the user to program the DDR2 SDRAM with an inverse AL of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to tRCD (MIN) with the requirement that AL ≥ tRCD (MIN). A typical application using this feature would set AL = tRCD (MIN) - 1x tCK. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of AL and CL; RL = AL + CL. Write latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 x tCK.

FIGURE 8 - EXTENDED MODE REGISTER 2 (EMR2) DEFINITION

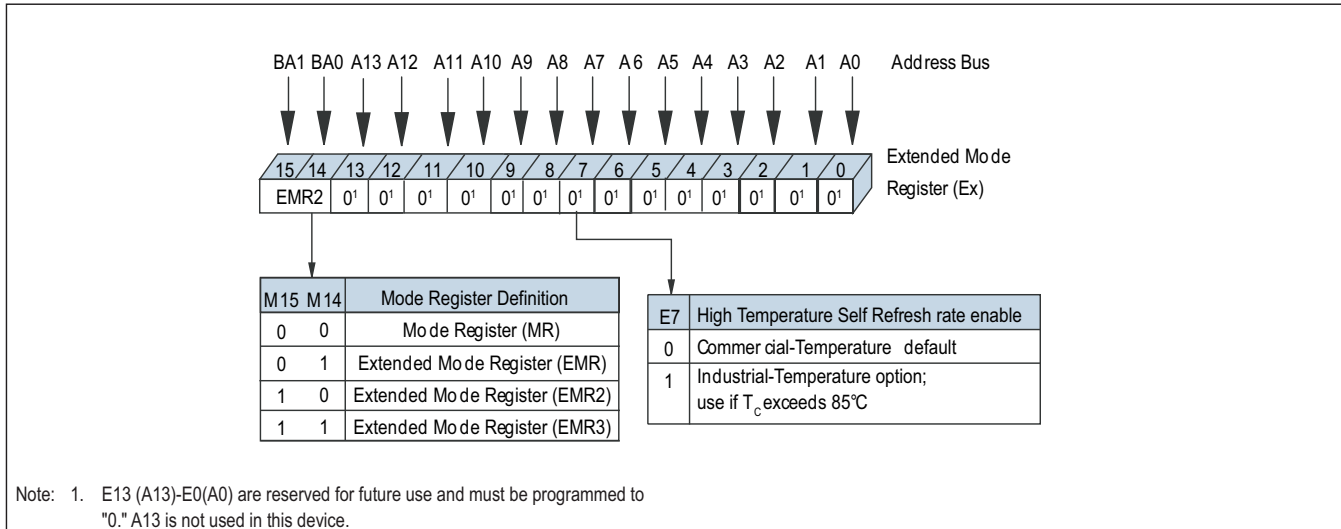
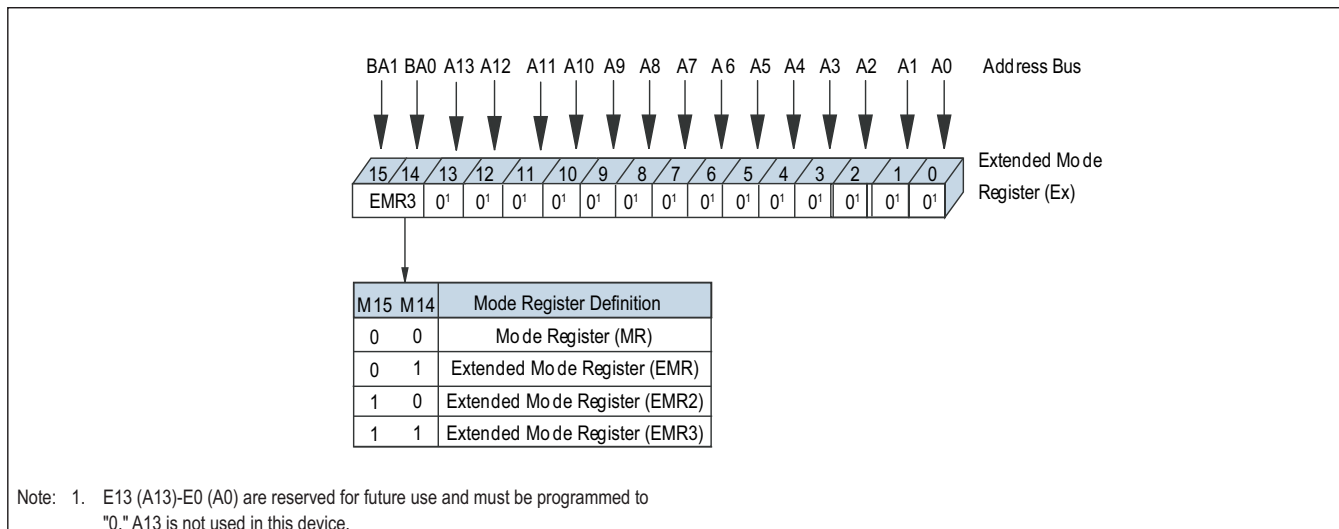




FIGURE 9 - EXTENDED MODE REGISTER 3 (EMR3) DEFINITION



EXTENDED MODE REGISTER 2

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, as shown in Figure 8. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

EXTENDED MODE REGISTER 3

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently, all bits in EMR3 are reserved, as shown in Figure 9. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

COMMAND TRUTH TABLES

The following tables provide a quick reference of DDR2 SDRAM available commands, including CKE power-down modes, and bank-to-bank commands.



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TABLE 3 - TRUTH TABLE - DDR2 COMMANDS

| Function | CKE | | CS# | RAS# | CAS# | WE# | BA1 BA0 | A12 A11 | A10 | A9-A0 | Notes |
|---------------------------|----------------|---------------|-----|------|------|-----|------------|----------------|-----|----------------|-------|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| LOAD MODE | H | H | L | L | L | L | BA | OP CODE | | | 2 |
| REFRESH | H | H | L | L | L | H | X | X | X | X | |
| SELF-REFRESH Entry | H | L | L | L | L | H | X | X | X | X | |
| SELF-REFRESH exit | L | H | H | X | X | X | X | X | X | X | 7 |
| | | | L | H | H | H | | | | | |
| Single Bank Precharge | H | H | L | L | H | L | X | X | L | X | 2 |
| All banks PRECHARGE | H | H | L | L | H | L | X | X | H | X | |
| Bank Activate | H | H | L | L | H | L | BA | ROW ADDRESS | | | |
| WRITE | H | H | L | L | H | L | BA | Column Address | L | Column Address | 2,3 |
| WRITE with auto precharge | H | H | L | H | L | L | BA | Column Address | H | Column Address | 2,3 |
| READ | H | H | L | H | L | H | BA | Column Address | L | Column Address | 2,3 |
| READ with auto precharge | H | H | L | H | L | H | BA | Column Address | L | Column Address | 2,3 |
| NO OPERATION | H | X | L | H | H | H | X | X | X | X | |
| Device DESELECT | H | X | H | X | X | X | X | X | X | X | |
| POWER-DOWN entry | H | L | H | X | X | X | X | X | X | X | 4 |
| | | | L | H | H | H | | | | | |
| POWER-DOWN exit | L | H | H | X | X | X | X | X | X | X | 4 |
| | | | L | H | H | H | | | | | |

- Note:
- All DDR2-SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
 - Bank addresses (BA) BA0-BA12 determine which bank is to be operated upon. BA during a LM command selects which mode register is programmed.
 - Burst reads or writes at BL=4 cannot be terminated or interrupted.
 - The power down mode does not perform any REFRESH operations. The duration of power down is therefore limited by the refresh requirements outlined in the AC parametric section.
 - The state of ODT does not effect the states described in this table. The ODT function is not available during self refresh. See "On Die Termination (ODT)" for details.
 - "X" means "H or L" (but a defined logic level)
 - Self refresh exit is asynchronous.



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DESELECT

The Deselect function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via inputs BA1–BA0, and A12–A0. BA1–BA0 determine which mode register will be programmed. See “Mode Register (MR)”. The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

BANK/ROW ACTIVATION ACTIVE COMMAND

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A12–A0 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

ACTIVE OPERATION

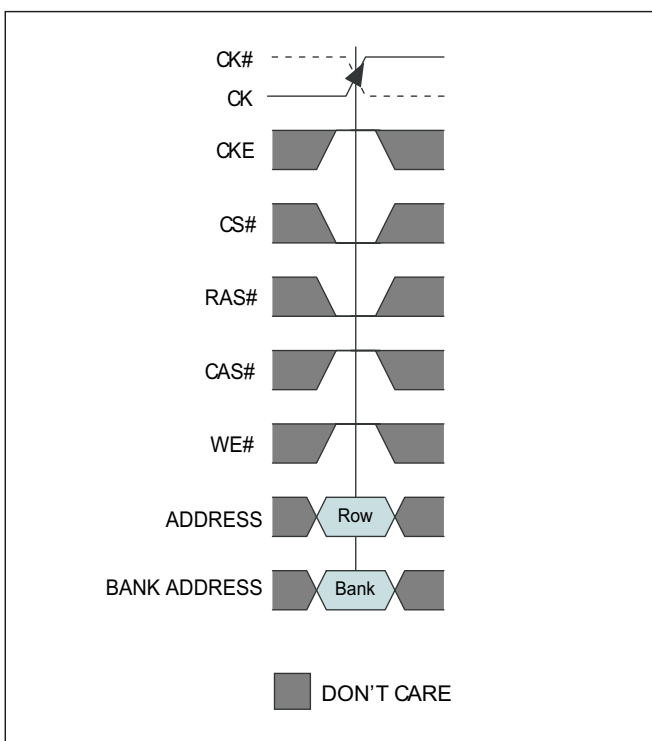
Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a tRCD (MIN) specification of 20ns with a 266 MHz clock (tCK = 3.75ns) results in 5.3 clocks, rounded up to 6.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

FIGURE 10 - ACTIVE COMMAND





READ COMMAND

The READ command is used to initiate a burst read access to an active row. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A0–i (where i = A9) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

READ OPERATION

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

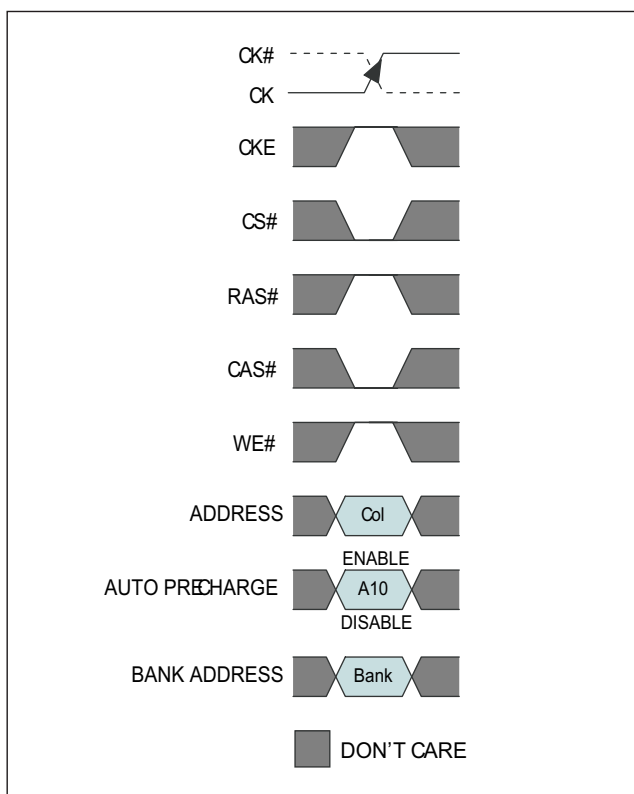
During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL; $RL = AL + CL$. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#).

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and HIGH state on DQS# is known as the read preamble (tRPRE). The LOW state on DQS and HIGH state on DQS# coincident with the last data-out element is known as the read postamble (tRPST).

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued x cycles after the first READ command, where x equals $BL / 2$ cycles.

FIGURE 11 - READ COMMAND



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WRITE COMMAND

The WRITE command is used to initiate a burst write access to an active row. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A0–9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

WRITE OPERATION

WRITE bursts are initiated with a WRITE command, as shown in Figure 12. DDR2 SDRAM uses WL equal to RL minus one clock cycle [$WL = RL - 1CK = AL + (CL - 1CK)$]. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is $WL \pm tDQSS$. Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as $\pm tDQSS$. $tDQSS$ is specified with a relatively wide range (25 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases ($tDQSS$ [MIN] and $tDQSS$ [MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued x cycles after the first WRITE command, where x equals $BL/2$.

DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 4.

DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using $BL = 4$ operation. Once the $BL = 4$ WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE (with auto precharge disabled) using $BL = 8$ operation might be interrupted and truncated ONLY by another WRITE burst as long as the interruption occurs on a 4-bit boundary, due to the $4n$ prefetch architecture of DDR2 SDRAM. WRITE burst $BL = 8$ operations may not to be interrupted or truncated with any command except another WRITE command.

Data for any WRITE burst may be followed by a subsequent READ command. The number of clock cycles required to meet $tWTR$ is either 2 or $tWTR/CK$, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. tWT starts at the end of the data burst, regardless of the data mask condition.



FIGURE 12 - WRITE COMMAND

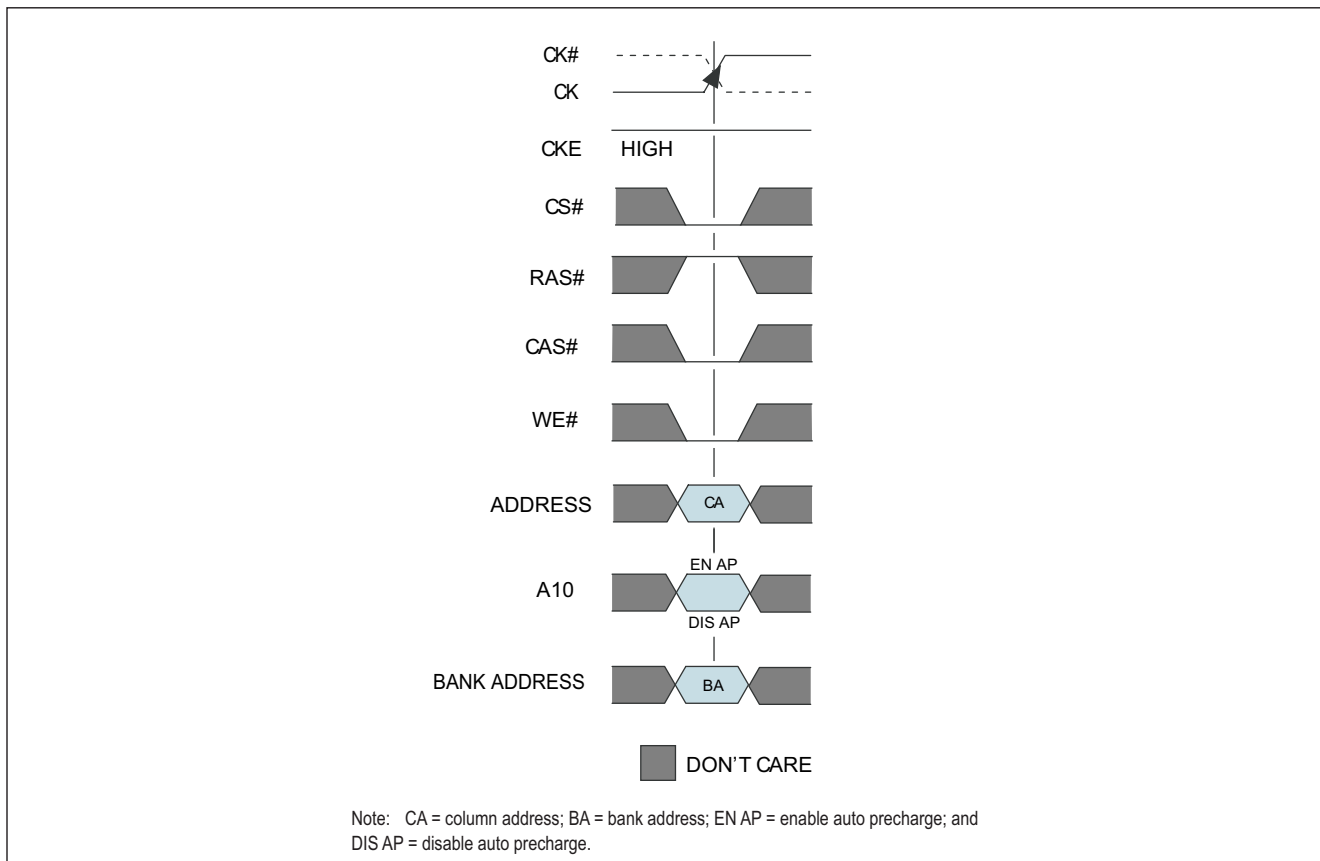


TABLE 4 - WRITE USING CONCURRENT AUTO PRECHARGE

| From Command (Bank <i>n</i>) | To Command (Bank <i>m</i>) | Minimum Delay (With Concurrent Auto Precharge) | Units |
|-------------------------------|-----------------------------|--|----------|
| WRITE with Auto Precharge | READ OR READ w/ AP | $(CL-1) + (BL/2) + t_{WTR}$ | t_{CK} |
| | WRITE OR WRITE w/ AP | $(BL/2)$ | t_{CK} |
| | PRECHARGE or ACTIVE | 1 | t_{CK} |

PRECHARGE COMMAND

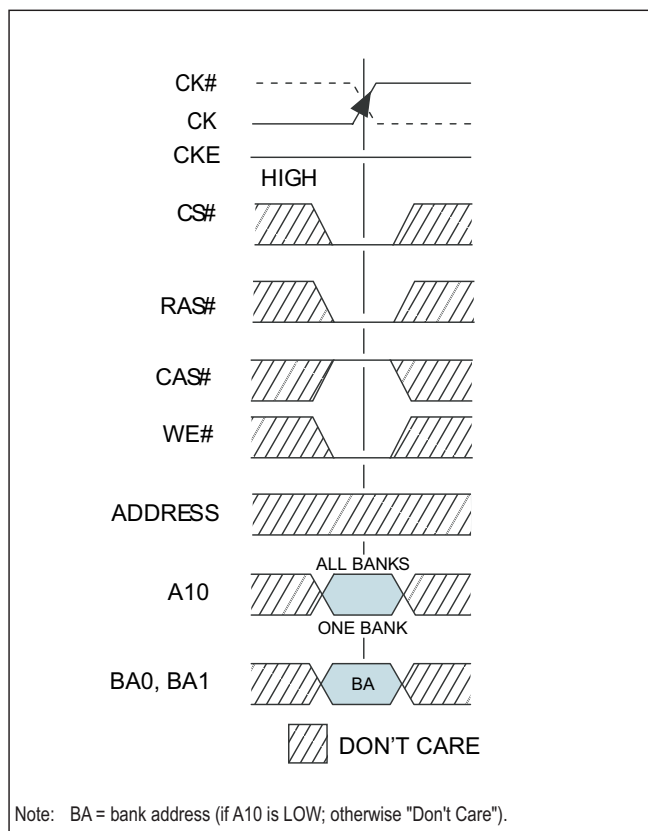
The PRECHARGE command, illustrated in Figure 13, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (t_{RP}) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

PRECHARGE OPERATION

Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA1–BA0 select the bank. Otherwise BA1–BA0 are treated as “Don’t Care.” When all banks are to be precharged, inputs BA1–BA0 are treated as “Don’t Care.”

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. t_{RPA} timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, t_{RP} timing applies.

FIGURE 13 – PRECHARGE COMMAND



issued). The differential clock should remain stable and meet t_{CKE} specifications at least $1 \times t_{CK}$ after entering self refresh mode. All command and address input signals except CKE are “Don’t Care” during self refresh.

The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet t_{CK} specifications at least $1 \times t_{CK}$ prior to CKE going back HIGH. Once CKE is HIGH ($t_{CLE}(\text{MIN})$ has been satisfied with four clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

Note: Self refresh not available at military temperature.

SELF REFRESH COMMAND

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including V_{REF}) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh (200 clock cycles must then occur before a READ command can be



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DC OPERATING CONDITIONS

All Voltages referenced to V_{SS}

| Parameter | Symbol | MIN | TYP | MAX | Units | Notes |
|-------------------------|------------------|-------------------------|-------------------------|-------------------------|-------|-------|
| Supply Voltage | V _{CC} | 1.7 | 1.8 | 1.9 | V | 1 |
| I/O Supply Voltage | V _{CCQ} | 1.7 | 1.8 | 1.9 | V | 4 |
| I/O Reference Voltage | V _{REF} | 0.49 x V _{CCQ} | 0.50 x V _{CCQ} | 0.51 x V _{CCQ} | V | 2 |
| I/O Termination Voltage | V _{TT} | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 | V | 3 |

Notes:

- V_{CC} V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
- V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCQ} tracks with V_{CC} track with V_{CC}.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|---|--|-------|------|----|
| V _{CC} | Voltage on V _{CC} pin relative to V _{SS} | -1.0 | 2.3 | V | |
| V _{CCQ} | Voltage on V _{CCQ} pin relative to V _{SS} | -0.5 | 2.3 | V | |
| V _{IN} , V _{OUT} | Voltage on any pin relative to V _{SS} | -0.5 | 2.3 | V | |
| T _{STG} | Storage Temperature | -55.0 | 125.0 | C | |
| T _{CASE} | Device Operating Temperature | -55.0 | 125.0 | C | |
| I _I | Input Leakage current; Any input 0V < V _{IN} < V _{CC} ; V _{REF} input 0V < V _{IN} < 0.95V; Other pins not under test = 0V | CMD/ADR, RAS ₁ , CAS ₁ , WE ₁ , CS ₁ , CKE | -10.0 | 10.0 | µA |
| | | CK, CK ₁ | -10.0 | 10.0 | µA |
| | | DM | -5 | 5 | µA |
| I _{OZ} | | -10 | 10 | µA | |
| I _{VREF} | | -10 | 10 | µA | |

INPUT / OUTPUT CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{CC} = V_{CCQ} = 1.8V

| Parameter | Symbol | Max | Unit |
|--|-------------------|-----|------|
| Input capacitance (A0-A12, BA0-BA1) | C _{ADDR} | 28 | pF |
| Input capacitance (CS#, RAS#, CAS#, WE#, CKE, ODT) | C _{IN1} | 10 | pF |
| Input capacitance CK, CK# | C _{IN2} | 8 | pF |
| Input capacitance DM, DQS, DQS# | C _{IN3} | 10 | pF |
| Input capacitance DQ0-63 | C _{OUT} | 12 | pF |



IPEM
2.1 Gb SDRAM-DDR2
 Austin Semiconductor, Inc. **AS4DDR232M64PBG**

INPUT DC LOGIC LEVEL

All voltages referenced to Vss

| Parameter | Symbol | Min | Max | Unit |
|------------------------------|---------------|-------------------|-------------------|------|
| Input High (Logic 1) Voltage | $V_{IH} (DC)$ | $V_{REF} + 0.125$ | $V_{CCQ} + 0.300$ | V |
| Input Low (Logic 0) Voltage | $V_{IL} (DC)$ | -0.300 | $V_{REF} - 0.125$ | V |

INPUT AC LOGIC LEVEL

All voltages referenced to Vss

| Parameter | Symbol | Min | Max | Unit |
|---|---------------|-------------------|-------------------|------|
| AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533 | $V_{IH} (AC)$ | $V_{REF} + 0.250$ | --- | V |
| AC Input High (Logic 1) Voltage DDR2-667 | $V_{IH} (AC)$ | $V_{REF} + 0.200$ | --- | V |
| AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533 | $V_{IL} (AC)$ | --- | $V_{REF} - 0.250$ | V |
| AC Input Low (Logic 1) Voltage DDR2-667 | $V_{IL} (AC)$ | --- | $V_{REF} - 0.200$ | V |



IPEM

2.1 Gb SDRAM-DDR2

Austin Semiconductor, Inc. AS4DDR232M64PBG

DDRII ICC SPECIFICATIONS AND CONDITIONS

| Parameter | Symbol | -3 | -38 | -5 | Units |
|---|---------------------------------|-----------|-----------|-----------|-------|
| Operating Current: One bank active-precharge tCL=tCK(ICC), tRC=tRC(ICC), tRAS=tRAS MIN(ICC); CKE is HIGH, CS\ is HIGH between valid commands; Address bus switching, Data bus switching | ICC0 | 480 | 440 | 400 | mA |
| Operating Current: One bank active-READ-precharge current IOUT=0mA; BL=4, CL=CL(ICC), AL=0; tCK = tCK(ICC), tRC=tRC(ICC), tRAS=tRAS MIN(ICC), tRCD=tRCD(ICC); CKE is HIGH, CS\ is HIGH between valid commands; Address bus is switching; | ICC1 | 650 | 520 | 480 | mA |
| Precharge POWER-DOWN current All banks idle; tCK=tCK(ICC); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | ICC2P | 25 | 25 | 25 | mA |
| Precharge quiet STANDBY current All banks idle; tCK=tCK(ICC); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | ICC2Q | 225 | 180 | 145 | mA |
| Precharge STANDBY current All banks idle; tCK=tCK(ICC); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | ICC2N | 250 | 200 | 170 | mA |
| Active POWER-DOWN current All banks open; tCK=tCK(ICC); CKE is LOW; Other control and address inputs are stable; Data bus inputs are floating | MRS[12]=0 ICC3P MRS[12]=1 | 145 32 | 125 32 | 105 32 | mA |
| Active STANDBY current All banks open; tCK=tCK(ICC), tRAS MAX(ICC), tRP=tRP(ICC); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | ICC3N | 275 | 225 | 200 | mA |
| Operating Burst WRITE current All banks open, continuous burst writes; BL=4, CL=CL(ICC), tRP=tRP(ICC); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs | ICC4W | 700 | 575 | 500 | mA |
| Operating Burst READ current All banks open, continuous burst READS, Iout=0mA; BL=4, CL=CL(ICC), AL=0; tCL=tCK(ICC), tRAS=tRAS MAX(ICC), tRP=tRP(ICC); CKE is HIGH, CS\ is HIGH between valid commands; Address and Data bus inputs switching | ICC4R | 750 | 625 | 550 | mA |
| Burst REFRESH current tCK=tCK(ICC); refresh command at every tRFC9(ICC) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control, Address and Data bus inputs are switching | ICC5 | 600 | 550 | 500 | mA |
| Self REFRESH current CK and CKI at 0V; CKE <= 0.2V; Other Control, address and data inputs are floating. | ICC6 | 25 | 25 | 25 | mA |
| Operating bank Interleave READ current: All bank interleaving READS, IOUT = 0mA; BL=4, CL=CL(ICC), AL=tRCD(ICC)-1xtCK(ICC); tCK=tCK(ICC), tRC=tRC(ICC), tRRD=tRRD(ICC); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are stable during deselects; Data | ICC7 | 1025 | 1025 | 1025 | mA |



IPEM

2.1 Gb SDRAM-DDR2

Austin Semiconductor, Inc. AS4DDR232M64PBG

AC OPERATING SPECIFICATIONS

| Parameter | | | -3 | | -38 | | -5 | | Units | |
|--|---------------------------------------|----------------------|-----------------------|----------|----------------|----------|----------------|----------|----------|-----|
| | | | 333MHz/667Mbps | | 266MHz/567Mbps | | 200MHz/400Mbps | | | |
| | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| Clock | Clock Cycle Time | CL=5 | tCK _{AVG} | 3 | 8 | | | | ns | |
| | | CL=4 | tCK _{AVG} | 3.75 | 8 | 3.75 | 8 | 5 | 8 | ns |
| | | CL=3 | tCK _{AVG} | 5 | 8 | 5 | 8 | 5 | 8 | ns |
| | Clock High Time | | tCH _{AVG} | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK |
| | | | tCL _{AVG} | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK |
| | Half Clock Period | Min of | tHP | tCH,tCL | | | tCH,tCL | | ps | |
| Clock Jitter | Clock Jitter - Period | | tJIT _{PER} | -125 | 125 | -125 | 125 | -125 | 125 | ps |
| | Clock Jitter - Half Period | | tJIT _{DUTY} | -125 | 125 | -125 | 125 | -150 | 150 | ps |
| | Clock Jitter - Cycle to Cycle | | tJIT _{CC} | 250 | | 250 | | 250 | | ps |
| | Cumulative Jitter error, 2 Cycles | | tERR _{2PER} | -175 | 175 | -175 | 175 | -175 | 175 | ps |
| | Cumulative Jitter error, 4 Cycles | | tERR _{4PER} | -250 | 250 | -250 | 250 | -250 | 250 | ps |
| | Cumulative Jitter error, 6-10 Cycles | | tERR _{10PER} | -350 | 350 | -350 | 350 | -350 | 350 | ps |
| | Cumulative Jitter error, 11-50 Cycles | | tERR _{50PER} | -450 | 450 | -450 | 450 | -450 | 450 | ps |
| | DQ hold skew factor | | tQHS | - | 340 | - | 400 | - | 450 | ps |
| | DQ output access time from CK/CK\ | | tAC | -450 | 450 | -500 | 500 | -600 | 600 | ps |
| | Data-out High-Z window from CK/CK\ | | tHZ | | tAC(MAX) | | tAC(MAX) | | tAC(MAX) | ps |
| DQS Low-Z window from CL/CK\ | | tLZ ₁ | tAC(MIN) | tAC(MAX) | tAC(MIN) | tAC(MAX) | tAC(MIN) | tAC(MAX) | ps | |
| DQ Low-Z window from CK/CK\ | | tLZ ₂ | 2*tAC(MIN) | tAC(MAX) | 2*tAC(MIN) | tAC(MAX) | 2*tAC(MIN) | tAC(MAX) | ps | |
| DQ and DM input setup time relative to DQS | | tDS _{JEDEC} | 100 | | 100 | | 150 | | ps | |
| DQ and DM input hold time relative to DQS | | tDS _{JEDEC} | 175 | | 225 | | 275 | | ps | |
| DQ and DM input pulse width (for each input) | | tDIPW | 0.35 | | 0.35 | | 0.35 | | tCK | |
| Data Hold skew factor | | tQHS | | 340 | | 400 | | 450 | ps | |
| DQ-DQS Hold, DQS to first DQ to go non valid, per access | | tQH | tHP-tQHS | | tHP-tQHS | | tHP-tQHS | | ps | |
| Data valid output window (DVW) | | tDVW | tQH-tDQSQ | | tQH-tDQSQ | | tQH-tDQSQ | | ps | |
| DQS input-high pulse width | | tDQSH | 0.35 | | 0.35 | | 0.35 | | tCK | |
| DQS input-low pulse width | | tDQSL | 0.35 | | 0.35 | | 0.35 | | tCK | |
| DQS output access time from CK/CK\ | | tDQSK | -400 | 400 | -400 | 400 | -450 | 450 | ps | |
| DQS falling edge to CK rising - setup time | | tDSS | 0.2 | | 0.2 | | 0.2 | | tCK | |
| DQS falling edge from CK rising-hold time | | tDSH | 0.2 | | 0.2 | | 0.2 | | tCK | |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | | tDQSQ | | 240 | | 300 | | 350 | ps | |
| DQS READ preamble | | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| DQS READ postamble | | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| WRITE preamble setup time | | tWPRES | 0 | | 0 | | 0 | | ps | |
| DQS WRITE preamble | | tWPRES | 0.35 | | 0.25 | | 0.25 | | tCK | |
| DQS WRITE postamble | | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Positive DQS latching edge to associated Clock edge | | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | tCK | |
| WRITE command to first DQS latching transition | | | WL-tDQSS | WL+tDQSS | WL-tDQSS | WL+tDQSS | WL-tDQSS | WL+tDQSS | tCK | |



IPEM

2.1 Gb SDRAM-DDR2

Austin Semiconductor, Inc. AS4DDR232M64PBG

AC OPERATING SPECIFICATIONS (CONTINUED)

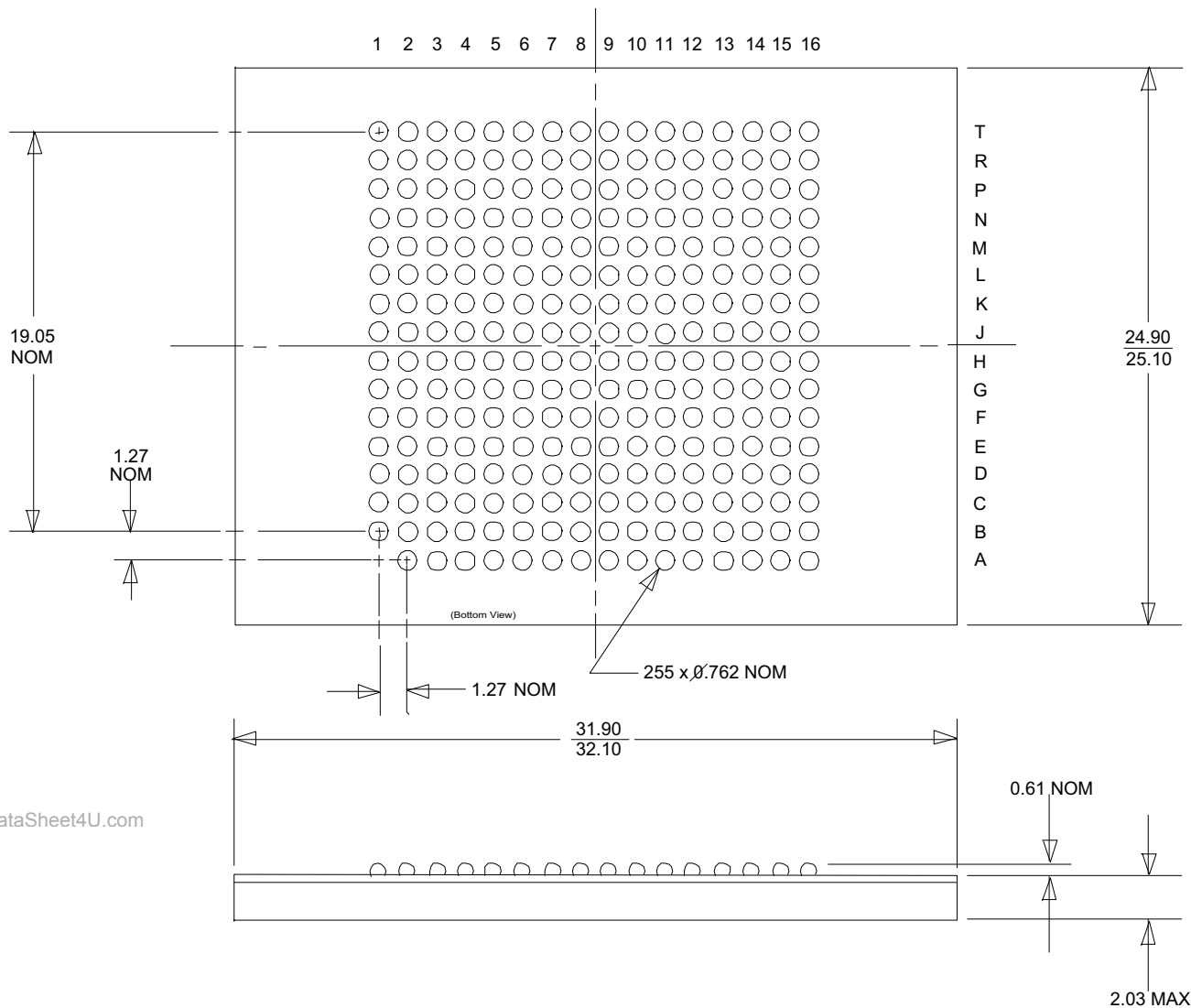
| Parameter | Symbol | -3 333MHz/667Mbps | | -38 266MHz/567Mbps | | -5 200MHz/400Mbps | | Units | |
|-------------------------------|--|-----------------------|-----------------|---------------------------|-----------------|---------------------------|-----------------|---------------------------|-----|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| COMMAND and ADDRESS | Address and Control input pulse width for each input | tIPW | 0.6 | | 0.6 | | 0.6 | tCK | |
| | Address and Control input setup time | tS _{JEDDEC} | 200 | | 250 | | 350 | ps | |
| | Address and Control input hold time | tIH _{JEDDEC} | 275 | | 375 | | 475 | ps | |
| | CAS\ to CAS\ command delay | tCCD | 2 | | 2 | | 2 | ps | |
| | ACTIVE to ACTIVE command (same bank) | tRC | 55 | | 55 | | 55 | ps | |
| | ACTIVE bank a to ACTIVE bank b Command | tRRD | 10 | | 10 | | 10 | ns | |
| | ACTIVE to READ or WRITE delay | tRCD | 15 | | 15 | | 15 | ns | |
| | 4-Bank activate period | tFAW | 50 | | 50 | | 50 | ns | |
| | ACTIVE to PRECHARGE | tRAS | 40 | 70000 | 10 | 70000 | 40 | 70000 | ns |
| | Internal READ to PRECHARGE command delay | tRTP | 7.5 | | 7.5 | | 7.5 | ns | |
| | WRITE recovery time | tWR | 15 | | 15 | | 15 | ns | |
| | Auto PRECHARGE WRITE recovery+PRECHARGE time | tDAL | tWR + tRP | | tWR + tRP | | tWR + tRP | ns | |
| | Internal WRITE to READ command delay | tWTR | 7.5 | | 7.5 | | 10 | ns | |
| | PRECHARGE command period | tRP | 15 | | 15 | | 15 | ns | |
| PRECHARGE ALL command period | tRPA | tRP+tCL | | tRP+tCL | | tRP+tCL | ns | | |
| LOAD MODE, command Cycle time | tMRD | 2 | | 2 | | 2 | tCK | | |
| REFRESH | CKE LOW to CK, CKI uncertainty | tDELAY | tIS + tCL + tIH | | tIS + tCL + tIH | | tIS + tCL + tIH | ns | |
| | REFRESH to ACTIVE or REFRESH to REFRESH command Interval | tRFC | 105 | 70000 | 105 | 70000 | 105 | 70000 | ns |
| | Average periodic REFRESH interval [Industrial temp] | tREFI _{IT} | | 7.8 | | 7.8 | | 7.8 | us |
| | Average periodic REFRESH interval [Enhanced temp] | tREFI _{ET} | | TBD | | 3.9 | | 3.9 | us |
| | Average periodic REFRESH interval [Military temp] | tREFI _{XT} | | TBD | | TBD | | 3.9 | us |
| S. REFRESH | Exit SELF REFRESH to non READ command | tXSNR | tRFC(min)+10 | | tRFC(min)+10 | | tRFC(min)+10 | ns | |
| | Exit SELF REFRESH to READ command | tXSRD | 200 | | 200 | | 200 | tCK | |
| | Exit SELF REFRESH timing reference | tISXR | tIS | | tIS | | tIS | ps | |
| ODT | ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | 2 | 2 | tCK |
| | ODT turn-on delay | tAOND | tAC(min) | tAC(max)+700 | tAC(min) | tAC(max)+1000 | tAC(min) | tAC(max)+1000 | ps |
| | ODT turn-off delay | tAOPD | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | tCK |
| | ODT turn-off delay | tAOF | tAC(min) | tAC(max)+600 | tAC(min) | tAC(max)+600 | tAC(min) | tAC(max)+600 | ps |
| | ODT turn-on (power-down mode) | tAONPD | tAC(min)+2000 | 2 x tCK + tAC(max)+1000 | tAC(min)+2000 | 2 x tCK + tAC(max)+1000 | tAC(min)+2000 | 2 x tCK + tAC(max)+1000 | ps |
| | ODT turn-off (power-down mode) | tAQFPD | tAC(min)+2000 | 2.5 x tCK + tAC(max)+1000 | tAC(min)+2000 | 2.5 x tCK + tAC(max)+1000 | tAC(min)+2000 | 2.5 x tCK + tAC(max)+1000 | ps |
| | ODT to power-down entry latency | tANPD | 3 | | 3 | | 3 | | tCK |
| | ODT power-down exit latency | tAXPD | 8 | | 8 | | 8 | | tCK |
| | ODT enable from MRS command | tMOD | 12 | | 12 | | 12 | | ns |
| PWRDN | Exit active POWER-DOWN to READ command, MR[12]=0 | tXARD | 2 | | 2 | | 2 | | tCK |
| | Exit active POWER-DOWN to READ command, MR[12]=1 | tSARDS | 7 - AL | | 6 - AL | | 6 - AL | | tCK |
| | Exit PRECHARGE POWER-DOWN to any non READ | tXP | 2 | | 2 | | 2 | | tCK |
| | CKE Min. HIGH/LOW time | tCLE | 3 | | 3 | | 3 | | tCK |



AUSTIN SEMICONDUCTOR
Austin Semiconductor, Inc. AS4DDR232M64PBG

IPEM
2.1 Gb SDRAM-DDR2

MECHANICAL DIAGRAM



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2.1 Gb SDRAM-DDR2
 Austin Semiconductor, Inc. **AS4DDR232M64PBG**

ORDERING INFORMATION

| <u>Part Number</u> | <u>Core Frequency</u> | <u>Data Rate</u> | <u>Device Grade</u> | <u>Availability</u> |
|------------------------|-----------------------|------------------|---------------------|---------------------|
| AS4DDR232M64PBG-3/IT | 333MHz | 667Mbps | Industrial | Full Production |
| AS4DDR232M64PBG-38/IT | 266MHz | 533Mbps | Industrial | Full Production |
| AS4DDR232M64PBG-5/IT | 200MHZ | 400Mbps | Industrial | Full Production |
| AS4DDR232M64PBG-3/ET | 333MHz | 667Mbps | Enhanced | Full Production |
| AS4DDR232M64PBG-38/ET | 266MHz | 533Mbps | Enhanced | Full Production |
| AS4DDR232M64PBG-5/ET | 200MHZ | 400Mbps | Enhanced | Full Production |
| AS4DDR232M64PBG-3/XT | 333MHz | 667Mbps | Military | Full Production |
| AS4DDR232M64PBG-38/XT | 266MHz | 533Mbps | Military | Full Production |
| AS4DDR232M64PBG-5/XT | 200MHZ | 400Mbps | Military | Full Production |
| AS4DDR232M64PBGR-3/IT | 333MHz | 667Mbps | Industrial - RoHS | Full Production |
| AS4DDR232M64PBGR-38/IT | 266MHz | 533Mbps | Industrial - RoHS | Full Production |
| AS4DDR232M64PBGR-5/IT | 200MHZ | 400Mbps | Industrial - RoHS | Full Production |
| AS4DDR232M64PBGR-3/ET | 333MHz | 667Mbps | Enhanced - RoHS | Full Production |
| AS4DDR232M64PBGR-38/ET | 266MHz | 533Mbps | Enhanced - RoHS | Full Production |
| AS4DDR232M64PBGR-5/ET | 200MHZ | 400Mbps | Enhanced - RoHS | Full Production |
| AS4DDR232M64PBGR-3/XT | 333MHz | 667Mbps | Military- RoHS | Full Production |
| AS4DDR232M64PBGR-38/XT | 266MHz | 533Mbps | Military- RoHS | Full Production |
| AS4DDR232M64PBGR-5/XT | 200MHZ | 400Mbps | Military- RoHS | Full Production |

IT = Industrial = Full production, Industrial class integrated component, fully operable across -40C to +85C

ET = Enhanced = Full production, Enhanced class integrated component, fully operable across -40C to +105C

XT = Military = Full production, Mil-Temperature class integrated component, fully operable across -55C to +125C

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 * **Contact ASI Sales Rep for Thermal Models**



IPEM
2.1 Gb SDRAM-DDR2
 Austin Semiconductor, Inc. **AS4DDR232M64PBG**

DOCUMENT TITLE

2.1Gb, 32M x 64, DDR2 SDRAM, 25mm x 32mm - 255 PBGA Multi-Chip Package [iPEM]

REVISION HISTORY

| Rev # | History | Release Date | Status |
|--------------|--|---------------------|---------------|
| 1.0 | New Release | October 2007 | Preliminary |
| 1.1 | Added Configuration Addressing table to page 1 | September 2008 | Preliminary |
| 1.2 | Changed tRRD from tCK to ns, pg 25 | March 2009 | Preliminary |
| 1.3 | Changed temp reference from "Extended" to "Military" | June 2009 | Release |