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AS5115

Programmable 360º Magnetic Angle Encoder with Buffered SINE & COSINE Output Signals

1 General Description

The AS5115 is a contactless rotary encoder sensor for accurate angular measurement over a full turn of 360º and over an extended ambient temperature range of -40ºC to +150ºC.

Based on an integrated Hall element array, the angular position of a simple two-pole magnet is translated into analog output voltages. The angle information is provided by means of buffered sine and cosine voltages. This approach gives maximum flexibility in system design, as it can be directly integrated into existing architectures and optimized for various applications in terms of speed and accuracy.

An SSI Interface is implemented for signal path configuration as well as a one time programmable register block (OTP), which allows the customer to adjust the signal path gain to adjust for different mechanical constraints and magnetic field.

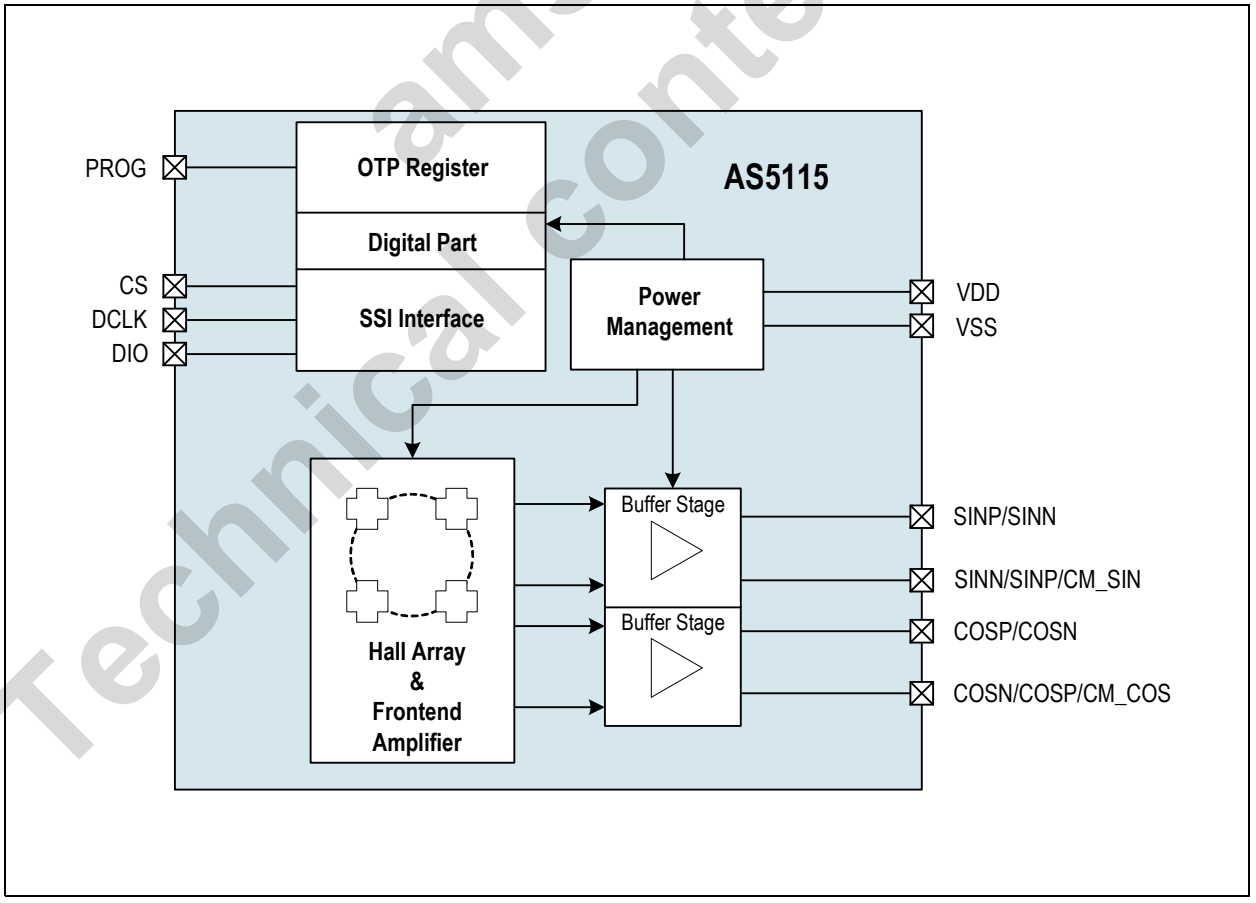
2 Key Features

- Contactless angular position encoding
- High precision analog output
- Buffered Sine and Cosine signals
- SSI Interface
- Low power mode
- Two programmable output modes: Differential or Single ended
- Wide magnetic field input range: 20 – 80 mT
- Wide temperature range: -40ºC to +150ºC
- Fully automotive qualified to AEC-Q100, grade 0
- SSOP-16 package

3 Applications

The AS5115 is ideal for several automotive and industrial applications.

Figure 1. AS5115 Block Diagram



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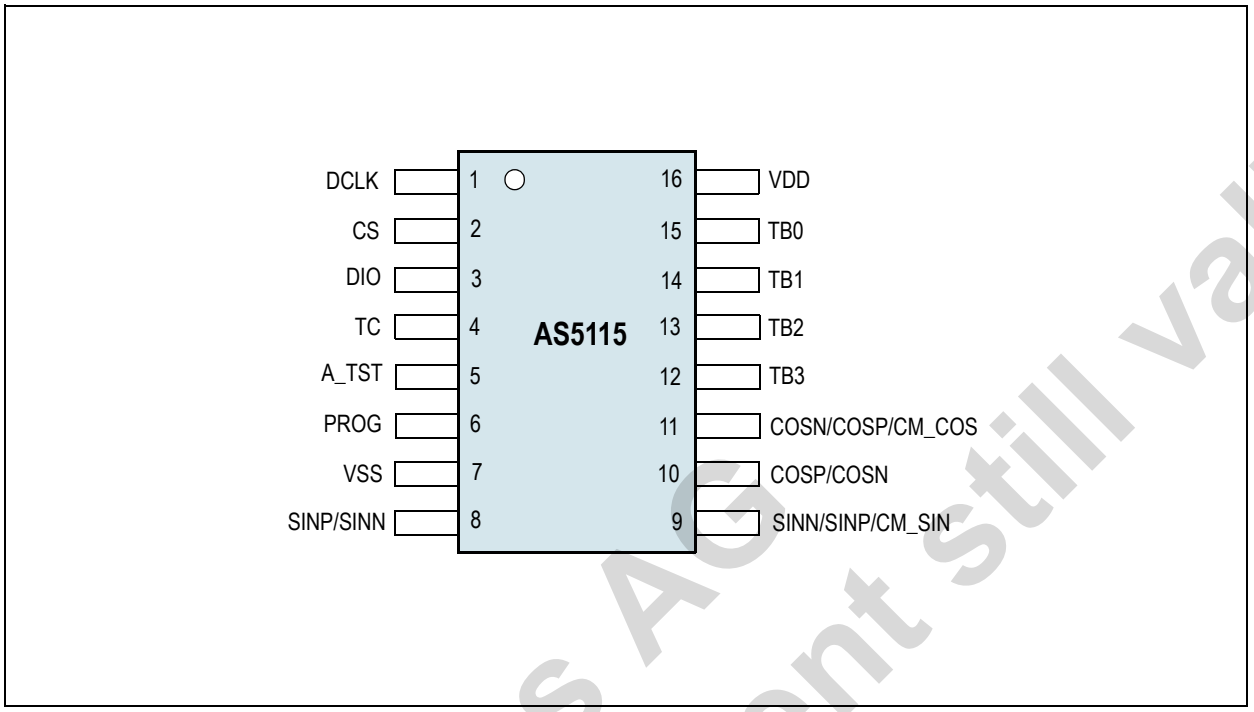
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
DCLK	1	Digital input with Schmitt trigger	Clock input for digital interface
CS	2		Clock input for digital interface, Scan enable
DIO	3	Digital input/output	Data I/O for digital interface, Scan input
TC	4	Analog input/output	Test coil
A_TST	5	Analog output/Digital output	Analog test pin, Scan output
PROG	6	Supply pad	OTP Programming Pad
VSS	7		Also used as VSS of test coil + EasyZapp (double bond)
SINP/SINN	8	Analog output	Buffered analog output
SINN/SINP/CM_SIN	9		
COSP/COSN	10		
COSN/COSP/CM_COS	11		
TB3	12	Analog output/Digital input	Test bus, analog output
TB2	13		
TB1	14		Test bus, analog output; external clock → sync. prod. test
TB0	15	Analog output	Test bus, analog output
VDD	16	Supply pad	Digital + analog supply

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
Supply voltage (V_{DD})	-0.3	7	V	
Input pin voltage (V_in)	-0.3	V_{DD}+0.3	V	
Input current (latchup immunity), I_scr	-100	100	mA	Norm: EIA/JESD78 Class II Level A
Electrostatic Discharge				
Electrostatic discharge (ESD)		±2	kV	Norm: JESD22-A114E
Continuous Power Dissipation				
Total power dissipation (P_{tot})		275	mW	
Package thermal resistance (Θ_JA)		27	°C/W	Velocity =0; Multi Layer PCB; Jedec Standard Testboard
Temperature Ranges and Storage Conditions				
Storage temperature (T_strg)	-65	150	°C	
Package body temperature (T_body)		260	°C	Norm: IPC/JEDEC J-STD-020. *The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level (MSL)	3			Represents a maximum floor time of 168h

6 Electrical Characteristics

Unless otherwise noted in this specification, all defined tolerances of parameters are assured over the whole operation conditions range and also over lifetime.

Table 3. Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Positive Supply Voltage		4.5		5.5	V
VSS	Negative Supply Voltage		0.0		0.0	V
T_amb	Ambient temperature		-40		150	ºC

Table 4. DC/AC Characteristics for Digital Inputs and Outputs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CMOS Input						
V_IH	High level input voltage		0.7 * VDD		VDD	V
V_IL	Low level input voltage		0		0.3 * VDD	V
I_LEAK	Input Leakage Current				1	µA
CMOS Output						
V_OH	High level output voltage	4mA	VDD - 0.5		VDD	V
V_OL	Low level output voltage	4mA	0		VSS + 0.4	V
C_L	Capacitive Load				35	pF
CMOS Output Tristate						
I_OZ	Tristate Leakage Current				1	µA

Table 5. Magnetic Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
B_{Zpp}	Magnetic input field amplitude	Peak to peak at the radius (=1mm) of the hall array	32		160	mT
B_offset	Magnetic field offset	Within the linear range of the magnet	-10		+10	mT
f_{rot}	Rotational speed	Maximum 30,000 RPM	0		500	Hz

Table 6. Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDD	Current Consumption	Maximum value derived at maximum I_H (Hall Bias Current)			28	mA
t_{power_on}	Power up time				1.275	ms
t_{prop}	Propagation delay	-40ºC to 150ºC	18	22	30	µs
M	Magnetic Sensitivity	Version: AS5115	10		60	mV / mT
		Version: AS5115A	20.72	28	35.28	
V_{PP}	Analog output voltage amplitude (peak to peak)		1.38	1.94	2.5	V
AM_{Temp}	AM tracking accuracy over temperature	-40ºC to 150ºC	-1		+1	%
AM	Sin / Cos Amplitude mismatch	25ºC	-2		+2	%
$V_{offset1}$	Output DC offset voltage	At no input signal; programmable OTP setting (see page 8)	1.47	1.5	1.53	V
$V_{offset2}$			2.45	2.5	2.55	
$DC_{offdrift}$	DC Offset Drift	-40ºC to 150ºC	-50		+50	µV/ºC

Table 6. Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOUT	Analog output range		VSS + 0.25		VDD - 0.5	V
IOUT	Output Current		-1		1	mA
CLOAD	Capacitive Load				1000	pF

6.1 Timing Characteristics

Table 7. Timing Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t1_3	Chip select to positive edge of DCLK	see Figure 5 and Figure 6	30		-	ns
t2_3	Chip select to drive bus externally		0		-	ns
t3	Setup time command bit Data valid to positive edge of DCLK		30		-	ns
t4	Hold time command bit Data valid after positive edge of DCLK		15		-	ns
t5	Float time Positive edge of DCLK for last command bit to bus float		-		$\frac{1}{(2+0)*f\_DCLK}$	ns
t6	Bus driving time Positive edge of DCLK for last command bit to bus drive		$\frac{1}{(2+0)*f\_DCLK}$		-	ns
t7	Data valid time Positive edge of DCLK to bus valid		$\frac{1}{(2+0)*f\_DCLK}$		$\frac{1}{(2+30)*f\_DCLK}$	ns
t8	Hold time data bit Data valid after positive edge of DCLK		$\frac{1}{(2+0)*f\_DCLK}$		-	ns
t9_3	Hold time chip select Positive edge DCLK to negative edge of chip select		$\frac{1}{(2+0)*f\_DCLK}$		-	ns
t10_3	Bus floating time Negative edge of chip select to float bus		-		30	ns
t11	Setup time data bit at write access Data valid to positive edge of DCLK		30		-	ns
t12	Hold time data bit at write access Data valid after positive edge of DCLK		15		-	ns
t13_3	Bus floating time Negative edge of chip select to float bus		-		30	ns

Remark: The digital interface will be reset during the low phase of the CS signal.

7 Detailed Description

The benefits of AS5115 are as follows:

- Complete system-on-chip, no angle calibration required
- Ideal for applications in harsh environments due to magnetic sensing principle
- High reliability due to non-contact sensing
- Robust system, tolerant to horizontal misalignment, temperature variations and external magnetic fields

7.1 Sleep Mode

The target is to provide the possibility to reduce the total current consumption. No output signal will be provided when the IC is in sleep mode. Enabling or disabling sleep mode is done by sending the SLEEP or WAKEUP commands via. the SSI interface. Analog blocks are powered down with respect to fast wake up time.

7.2 SSI Interface

The setup for the device is handled by the digital interface. Each communication starts with the rising edge of the chip select signal. The synchronization between the internal free running analog clock oscillator and the external used digital clock source for the digital interface is done in a way that the digital clock frequency can vary in a wide range.

Table 8. SSI Interface Pin Description

Port	Symbol	Function
Chip select	CS	Indicates the start of a new access cycle to the device CS = LO → reset of the digital interface
DCLK	DCLK	Clock source for the communication over the digital interface
Bidirectional data input output	DIO	Command and data information over one single line The first bit of the command defines a read or write access

Table 9. SSI Interface Parameter Description

Symbol	Parameter	Notes	Min	Typ	Max	Unit
f_DCLK	Clock frequency at normal operation	The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	no limit	5	6	MHz
f_EZ_RW	Clock frequency at easy zap read write access		no limit	5	6	kHz
f_EZ_PROG	Clock frequency at easy zap access program OTP	Correct access to the programmable zener diode block needs a strict timing – the zap pulse is exact one period. The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	200	-	650	kHz
f_EZ_ARB	Clock frequency at easy zap analog readback	20pF external load allowed. The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	no limit	156.3	162.5	kHz

Parameter	Notes
Interface General at normal mode	
Protocol: 5 command bit + 16 data input output	
Command	5-bit command: cmd<4:0> ← bit<21:16>
Data	16-bit data: data<15:0> ← bit<15:0>
Interface General at extended mode	
Protocol: 5 command bit + 46 data input output	

Parameter	Notes
Command	5-bit command: cmd<4:0> ← bit<50:46>
Data	34-bit data: data<45:0> ← bit<45:0>
Interface Modes	
Normal read operation mode	cmd<4:0> = <00xxx> → 1 DCLK per data bit
Extended read operation mode	cmd<4:0> = <01xxx> → 4 DCLK per data bit
Normal write operation mode	cmd<4:0> = <10xxx> → 1 DCLK per data bit
Extended write operation mode	cmd<4:0> = <11xxx> → 4 DCLK per data bit

7.3 Device Communication / Programming

Table 10. Digital Interface at Normal Mode

#	command	bin	mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	WRITE_CONFIG	10111	write	go2sleep	gen_rst					analog_sig	OB_bypassed								
16	EN_PROG	10000	write	1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	0

Name	Functionality
go2sleep	Enter/leave low power mode (no output signals)
gen_rst	Generates global reset
analog_sig	Switches the channels to the test bus after the PGA
OB_bypassed	Disable and bypass output buffer for testing purpose

Table 11. Digital Interface at Extended Mode

#	command	bin	mode	Factory Settings								User Settings					
				<45:44>	<43:26>	<25:23>	<22:20>	<19:18>	<17:14>	<13>	<12>	<11>	<10>	<9>	<8:7>	<6>	<5:0>
31	WRITE_OTP	11111	xt write	r	r	r	r	r	r	r	r	invert_channel	cm_sin	cm_cos	gain	dc_offset	hall_bias
25	PROG_OTP	11001	xt write	r	r	r	r	r	r	r	r	invert_channel	cm_sin	cm_cos	gain	dc_offset	hall_bias
15	RD_OTP	01111	xt read	r	r	r	r	r	r	r	r	invert_channel	cm_sin	cm_cos	gain	dc_offset	hall_bias
9	RD_OTP_ANA	01001	xt read														

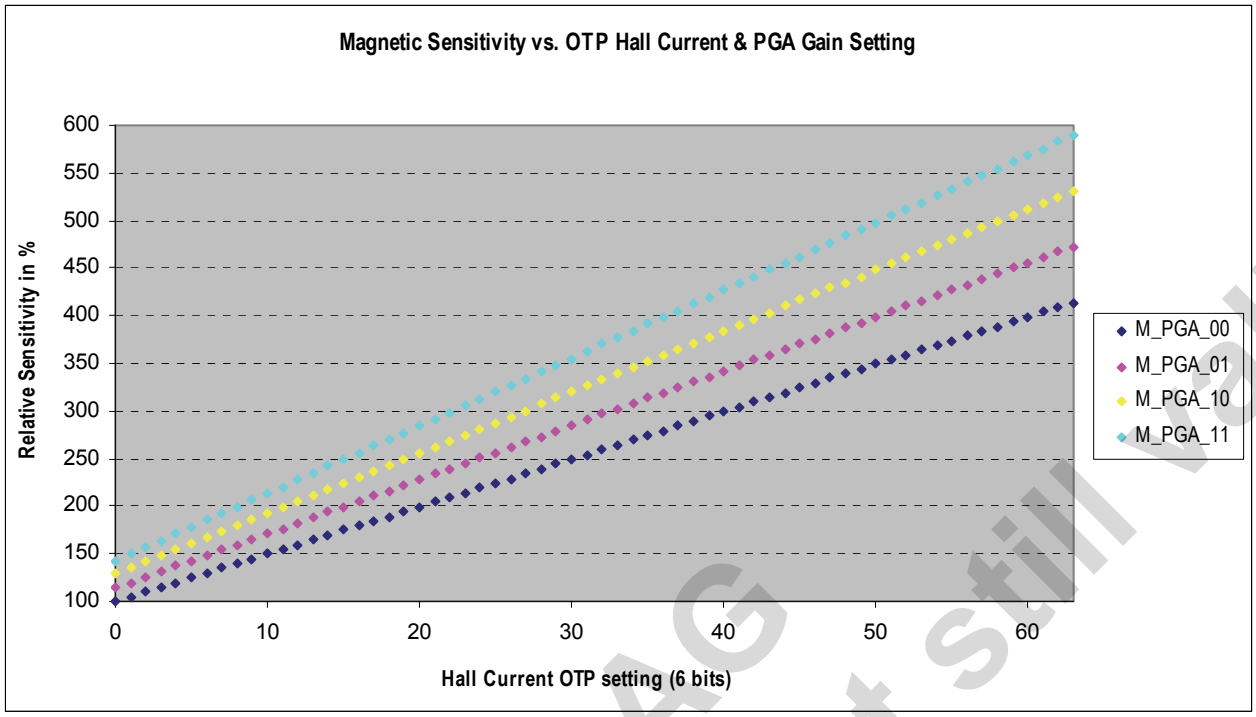
Note: "r" stands for reserved bits. They must not be modified, unless otherwise noted.

Remark:

1. Send EN PROG (command 16) in normal mode before accessing the OTP in extended mode.
2. OTP assignment will be defined/updated.

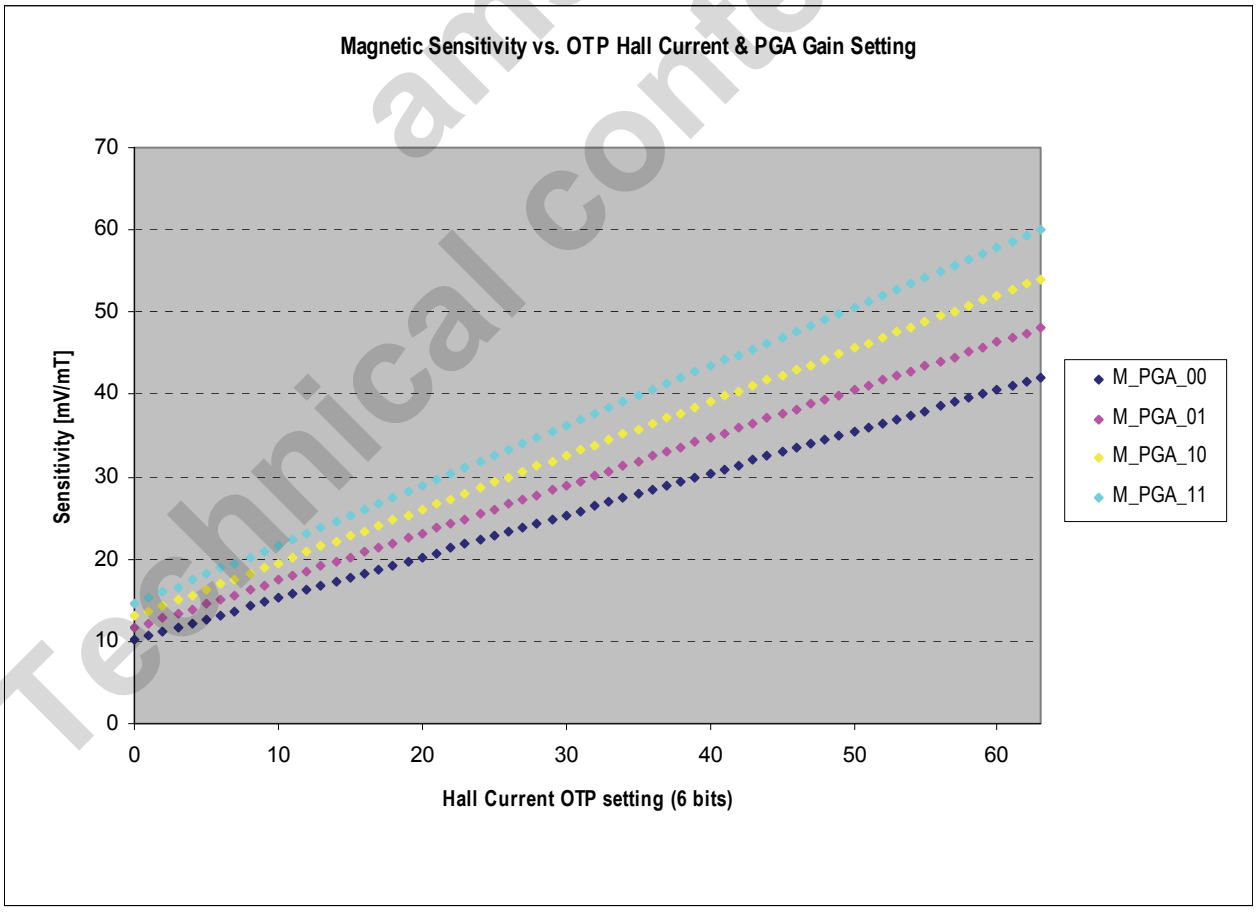
Name	Functionality
invert_channel Inverts	SIN and COS channel before the PGA for inverted output function (0 → SIN/COS, 1 → SINN/COSN)
cm_sin	Common mode voltage output enabled at SINN / CM pin (0 → differential, 1 → common)
cm_cos	Common mode voltage output enabled at COSN / CM pin (0 → differential, 1 → common)
gain	PGA gain setting (influences overall magnetic sensitivity), 2-bit
dc_offset	Output DC bias offset (0 → Voffset1=1.5V, 1 → Voffset2=2.5V)
Hall_b	Hall bias setting (influences overall magnetic sensitivity), 6-bit

Figure 3. Sensitivity Gain Settings - Relative Sensitivity in %



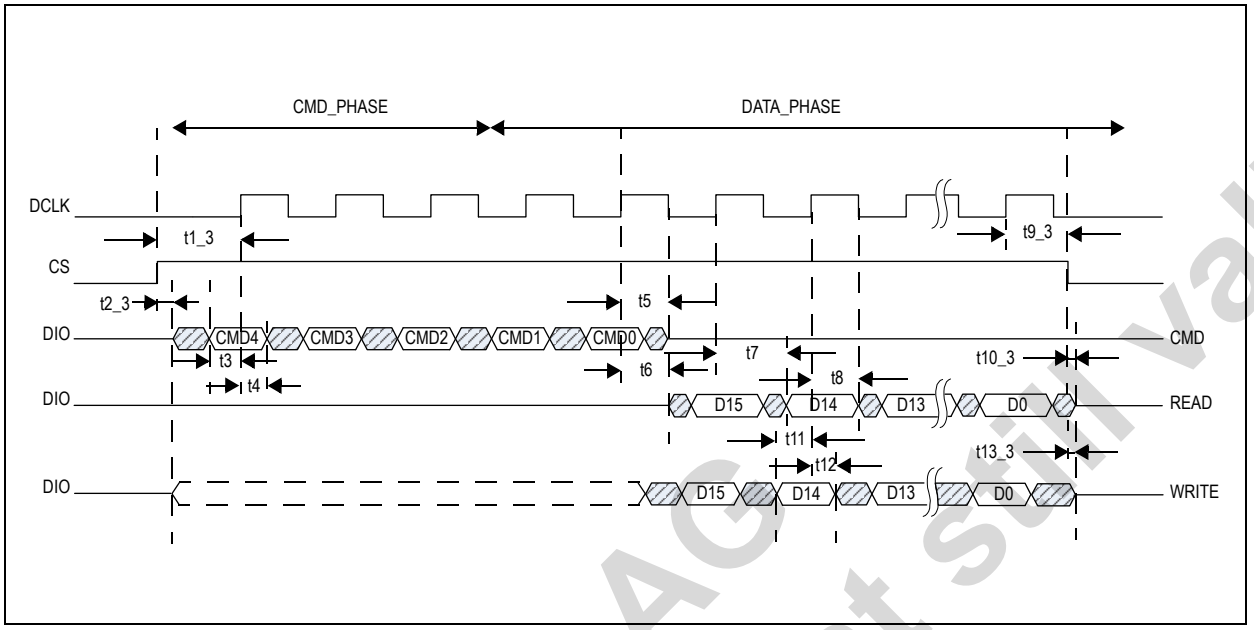
The amplitude of the output signal is programmable via sensitivity (6bit) and/or gain (2bit) settings (see Figure 3).

Figure 4. Sensitivity Gain Settings - Sensitivity [mV/mT]



7.4 Waveform – Digital Interface at Normal Operation Mode

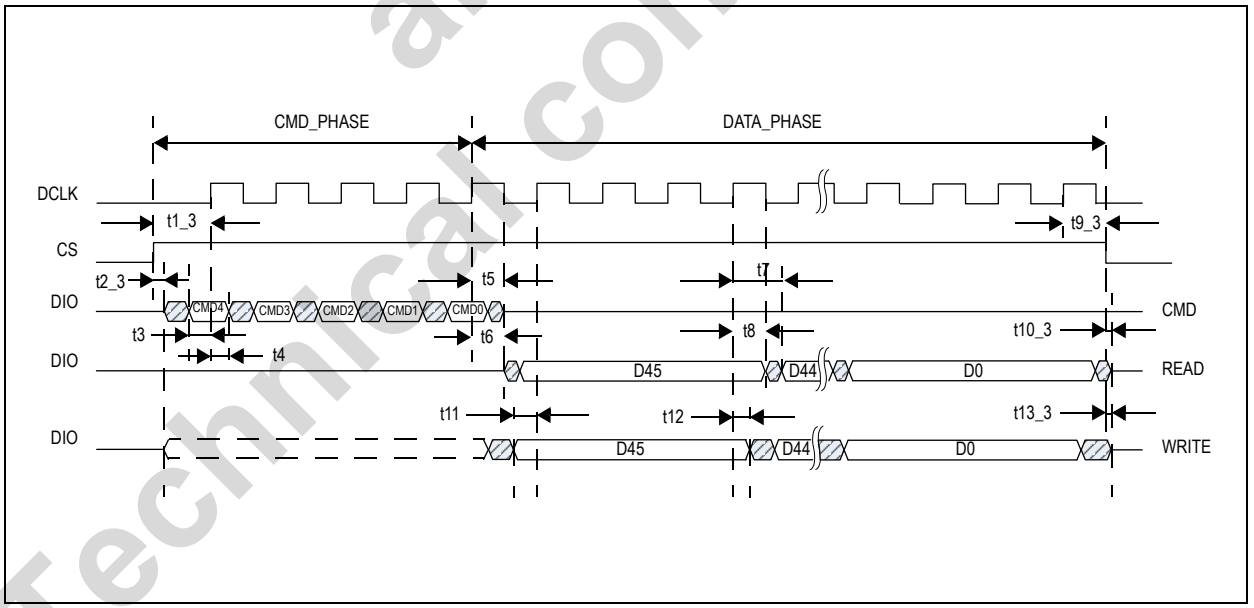
Figure 5. Digital Interface at Normal Operation Mode



7.5 Waveform – Digital Interface at Extended Mode

In the extended mode, the digital interface needs four clocks for one data bit due to the internal structure. During this time, the device is able to handle internal signals for special access (e.g. the easy zap interface).

Figure 6. Digital Interface at Extended Mode



7.6 Waveform – Digital Interface at Analog Readback of the Zener Diodes

To be sure that all Zener-Diodes are correctly burned, an analog readback mechanism is defined. Perform the 'READ OTP ANA' sequence according to the command table and measure the value of the diode at the end of each phase.

Figure 7. Digital Interface at Analog Readback of Zener Diodes

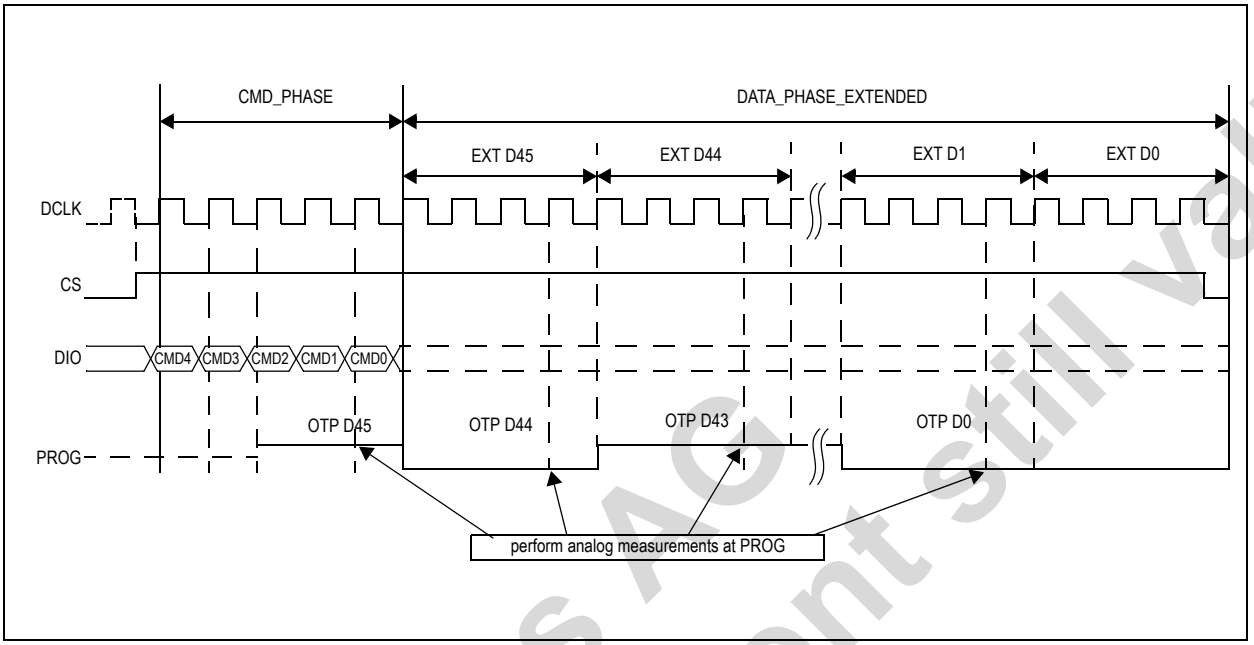


Table 12. Serial Bit Sequence (16-bit read / write)

Write Command					Read / Write Data														
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

7.7 One Time Programming Content

The AS5115 die has an integrated 46-bit OTP ROM (Easyzapp) for trimming and configuration purposes. The PROM can be programmed via. the serial interface. For irreversible programming, an external programming voltage at PROG pin is needed. For security reasons, the factory trim bits can be locked by a lock bit.

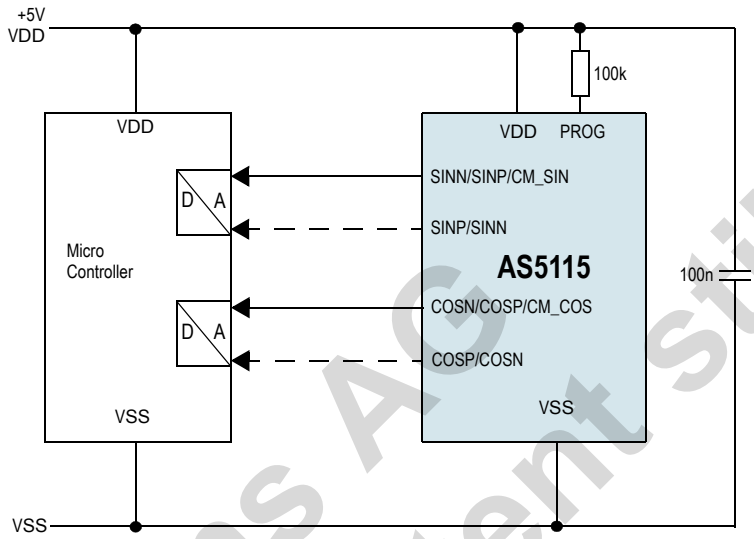
As shown in the table below, the OTP holds 46 bits. Bit number 44 and 45 are used for OTP testing purposes and ESD protection of the remaining cells.

Name	Bit Count	OTP Start	OTP End	Access	Comments
Hall_b	6	0	5	user	Sets overall sensitivity
dc_offset	1	6	6	user	Output DC offset setting
gain	2	7	8	user	Output Buffer Gain setting
Lock	1	13	13	austriamicrosystems	Set in production test
invert_channel	1	11	11	user	Inverts SIN and COS channel before the PGA for inverted output function
cm_sin	1	10	10	user	Common mode voltage output enabled at SINN / CM pin
cm_cos	1	9	9	user	Common mode voltage output enabled at COSN / CM pin

Remark: OTP assignment will be defined/updated.

7.8 Analog Sin/Cos Outputs with External Interpolator

Figure 8. Sine and Cosine Outputs for External Angle Calculation



Notes:

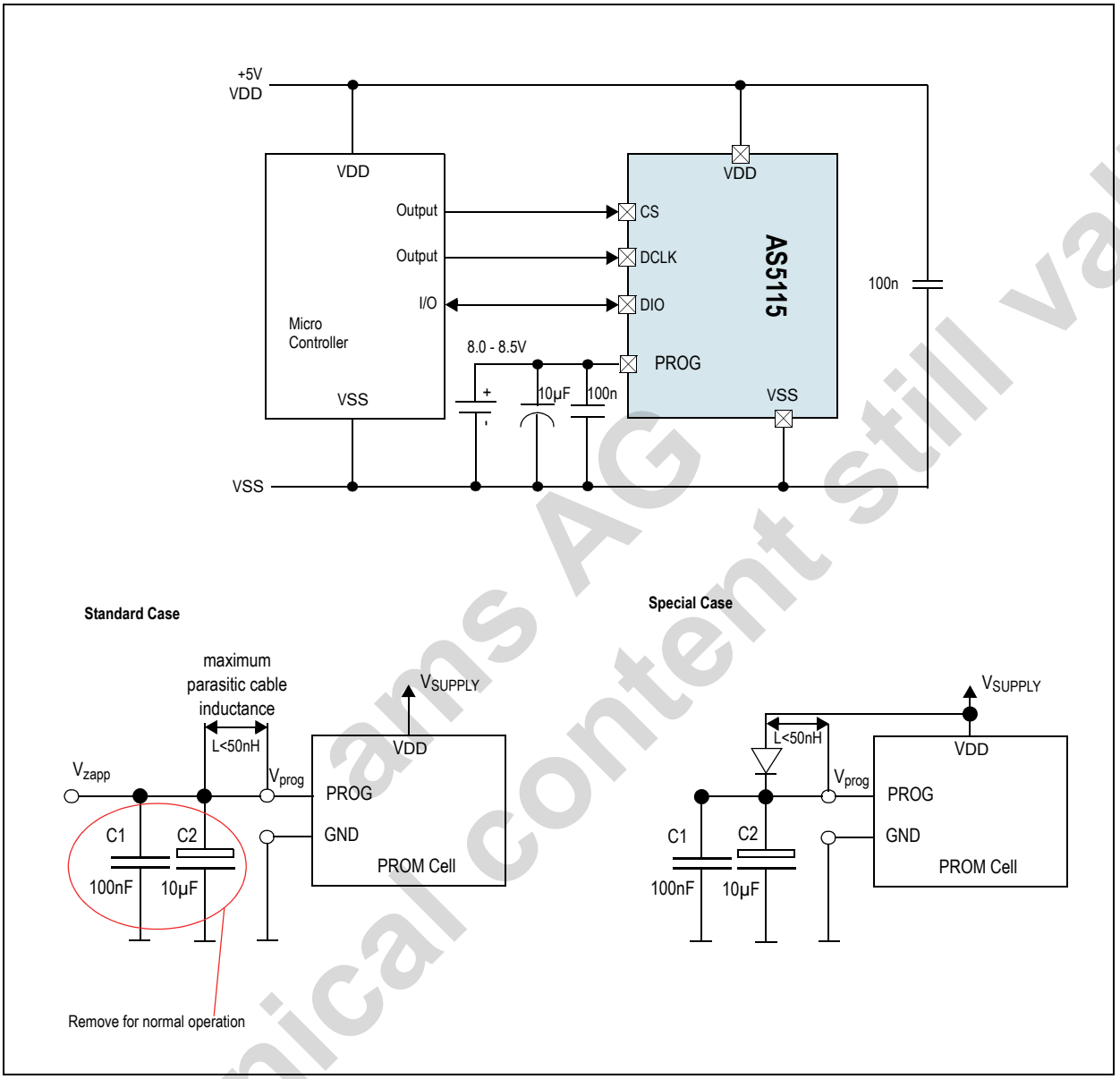
1. We recommend to use a 100k pull-up resistance.
2. Default conditions for unused pins are: DCLK, CS, DIO, TC, A_TST, TBO, TB1, TB2, TB3 connect to VSS

The AS5115 provides analog Sine and Cosine outputs (SINP, COSP) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + µC, e.g. to compute the angle with a high resolution. The signal lines must be kept as short as possible. In the case of longer lines, they must be shielded in order to achieve best noise performance.

Through the programming of one bit, you have the possibility to choose between the analog Sine and Cosine outputs (SINP, COSP) and their inverted signals (SINN, COSN). Furthermore, by programming the bits <9:10> you can enable the common mode output signals of SIN and COS.

7.9 OTP Programming and Verification

Figure 9. OTP Programming Connection



Note: The maximum capacitive load at PROG in normal operation should be less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and VDD as shown in Figure 9 (special case setup), if the capacitors can not be removed at final assembly.

Due to D1, the capacitors C1+C2 are loaded with VDD - 0.7V at startup, hence not influencing the readout of the internal OTP registers. During programming the OTP, the diode ensures that no current is flowing from PROG (8V - 8.5V) to VDD (5V).

In the standard case (see Figure 9), the verification of a correct OTP readout can be done by analog readback of the OTP register.

As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

For programming of the OTP, an additional voltage has to be applied to the pin PROG. It has to be buffered by a fast 100nF capacitor (ceramic) and a 10µF capacitor. The information to be programmed is set by command 25. The OTP bits 16 until 45 are used for AMS factory trimming and cannot be overwritten.

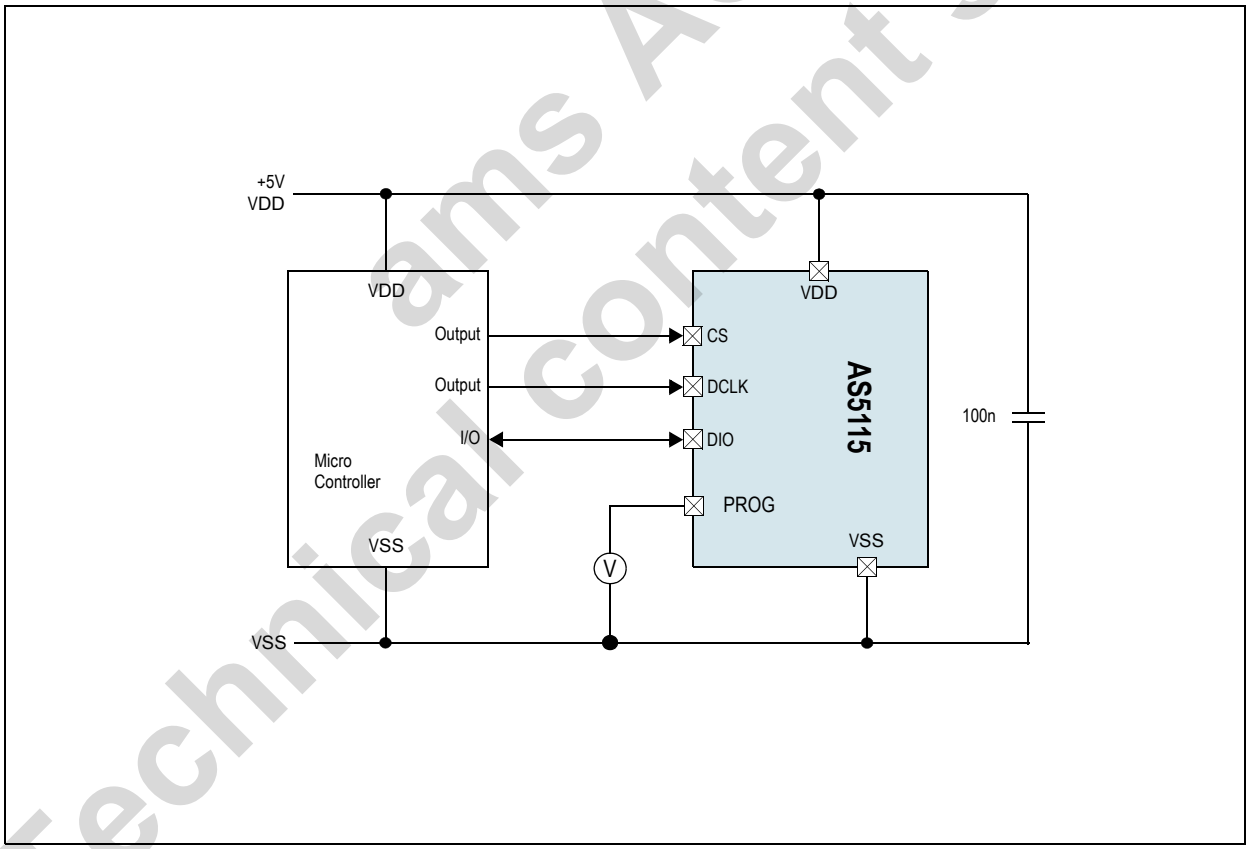
Symbol	Parameter	Min	Max	Unit	Note
VDD	Supply Voltage	5	5.5	V	
GND	Ground level	0	0	V	
V_zapp	Programming Voltage	8	8.5	V	At pin PROG
T_zapp	Temperature	0	85	ºC	
f_clk	CLK Frequency		100	kHz	At pin DCLK

After programming, the programmed OTP bits can be verified in two ways:

By Digital Verification: This is simply done by sending a READ OTP command (#15). The structure of this register is the same as for the OTP PROG or OTP WRITE commands.

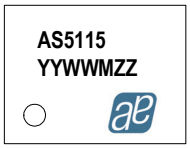
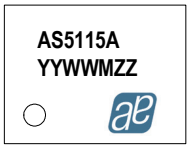
By Analog Verification: By switching into Extended Mode and sending an ANALOG OTP READ command (#9), pin PROG becomes an output, sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D45). A voltage of <500mV indicates a correctly programmed bit (“1”) while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit (“0”). Any voltage level in between indicates incorrect programming.

Figure 10. Analog OTP Verification



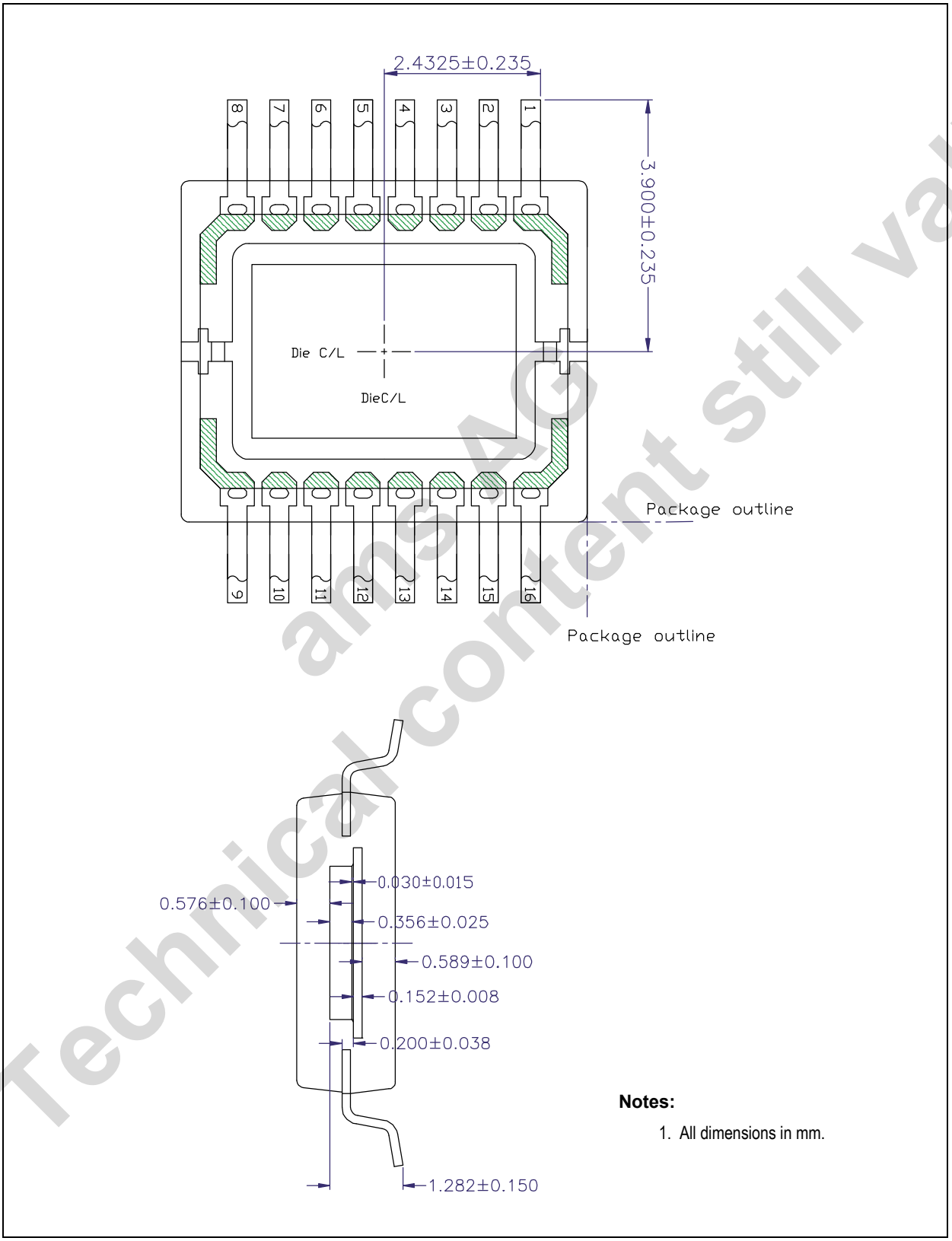
7.10 Pre-programmed Version

Table 13. Pre-programmed Version

Version	Marking	Sensitivity	Output	Output DC Offset	PGA Gain Setting	Hall Bias Current
AS5115		Not programmed	1.5V	0	Not programmed	Untrimmed
AS5115A		28 mV/mT	2.5V	1	00	12.15µA

8 Application Information

Figure 11. Vertical Cross Section of SSOP-16



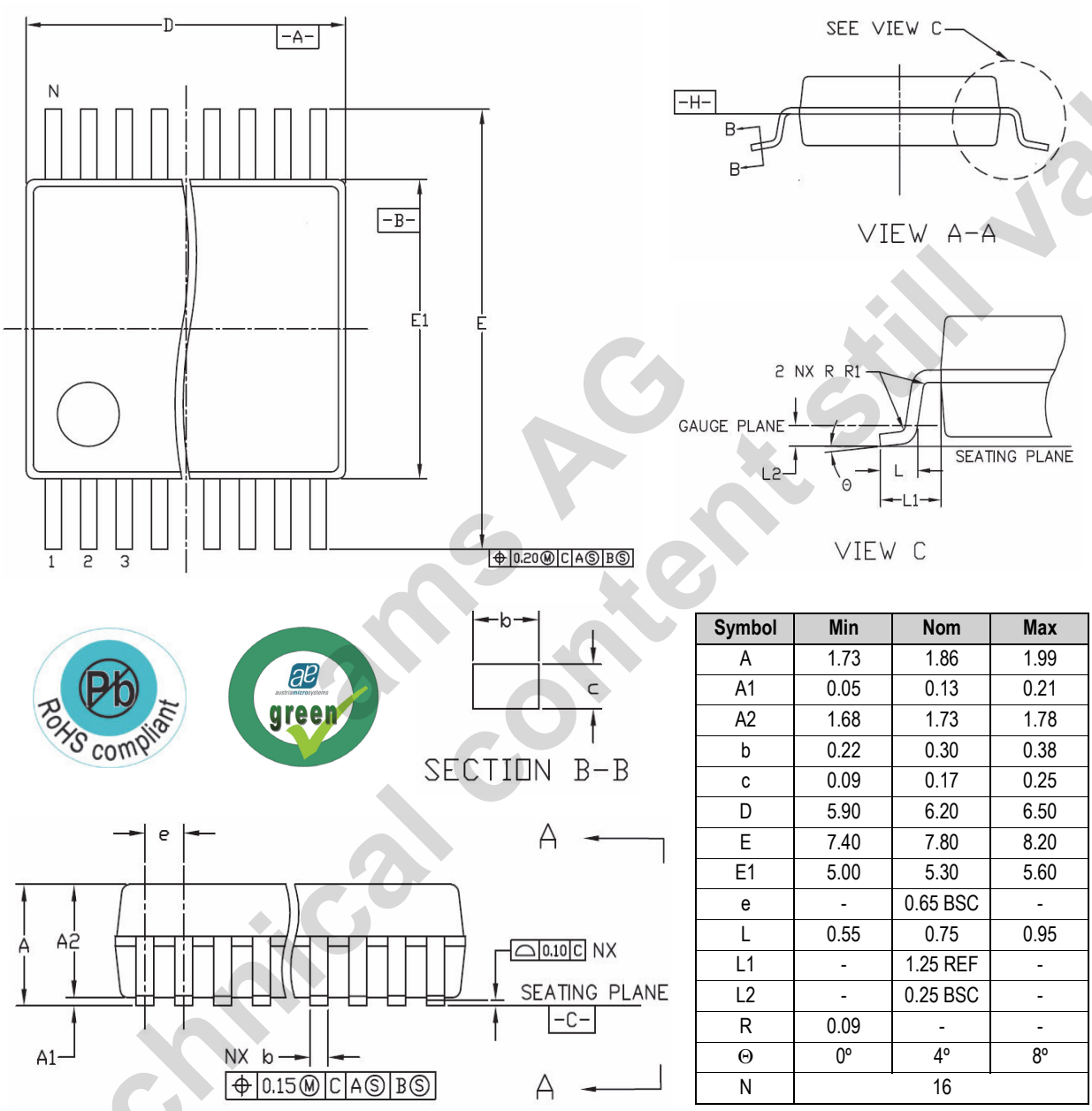
Notes:

1. All dimensions in mm.

9 Package Drawings and Markings

The devices are available in a 16-Lead Shrink Small Outline package.

Figure 12. Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.30	0.38
c	0.09	0.17	0.25
D	5.90	6.20	6.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
Θ	0°	4°	8°
N	16		

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.

Marking: YYWWMZZ.

YY	WW	M	ZZ
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Assembly traceability code

Revision History

Revision	Date	Owner	Description
1.0	Jul 03, 2008	apg	Initial revision
1.1	Jul 15, 2008		Key Features and pin description updated.
1.2	Jul 14, 2009		Updated min, typ, max values for 'Power up time' parameter in Table 6.
1.3	Nov 30, 2009		Deleted 'Displacement' parameter from Table 5. Updated the following parameters in Table 6: - Values and conditions updated for 1. Propagation delay 2. Amplitude ratio tracking accuracy over temperature 3. DC Offset Drift - Deleted the 'Output Offset' parameter from the table. Updated following bits related information on page 8 - invert_channel, cm_sin, cm_cos, gain, dc_offset, Hall_b Inserted Figure 3 and Figure 4 Updated Key Features (page 1), Table 11, and Figure 8 Hall Array Radius value updated from 1.1mm to 1mm
1.4	Dec 11, 2009		Updated values for 'Magnetic Sensitivity' parameter in Table 6.
1.5	Mar 02, 2010		Updated 'Interface General at extended mode' (see Table 9) Updated values for 'Power up time' parameter in Table 6. Added pin type in Table 1, updated reserved bits information in Table 11.
	Mar 19, 2010		Added 'Current Consumption' parameter in Table 6.
	Nov 10, 2010	sti	Updated Table 5 and Table 6.
1.6	Feb 07, 2011	mub	Added Figure 11. Updated Package Drawings and Markings (page 17), Table 2 and Table 5. Removed magnet related detailed info.
1.7	Feb 16, 2011	sti	Updated Table 5.
1.8	Mar 22, 2011	mub	Updated Package Drawings and Markings (page 17).
	Apr 07, 2011	apg	Deleted Tubes variant in Ordering Information (page 19).
	May 26, 2011	mub	Updated Key Features, OTP Programming and Verification, Table 4, Table 6.
	Jun 10, 2011		Updated Absolute Maximum Ratings (page 4).
1.9	Sep 19, 2011		Updated Ordering Information (page 19).
1.10	Dec 14, 2011	ekno	Added subversion AS5115A info in the datasheet.
	Feb 10, 2012		Updated Figure 9 added Note on page13.
1.11	Mar 06, 2012		Updated Table 6 and Figure 9

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 14.

Table 14. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5115-HSST	Buffered Sine and Cosine output signals	Tape & Reel	16-pin SSOP
AS5115-HSSM		Tape & Reel	16-pin SSOP

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