



128K x 8 SRAM RUGGEDIZED PLASTIC HIGH SPEED SRAM

FEATURES

- Access times of 15, 20 and 25 ns
- Fast output enable (t_{AOE}) for cache applications
- Low active power
- Low standby power
- Fully static operation, no clock or refresh required
- TTL Compatible Inputs and Outputs
- Single +5V power supply
- Package in Industry-standard 32-pin SOJ

OPTIONS

- Timing
 - 15ns access
 - 20ns access
 - 25ns access

MARKING

-15	DJ	No. 905
-20		
-25		

- Package
Plastic SOJ*

- Operating Temperature Ranges
 - Military (-55°C to +125°C) XT
 - Industrial (-40°C to +85°C) IT

GENERAL DESCRIPTION

The ASI AS5C1008 is a high speed, low power, 128K by 8-bit ruggedized plastic (COTS) CMOS Static RAM. It is fabricated using high performance, CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns (Max) over the military and industrial temperature ranges.

When Chip Enable (CE) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 125mW (max) at CMOS input levels.

Easy memory expansion is provided by using asserted LOW CE and asserted HIGH CE₂, and asserted LOW write enable (WE) controls both writing and reading of the memory.

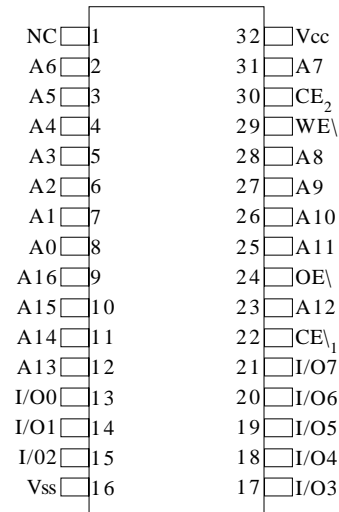
The AS5C1008 is pin-compatible with other 128K x 8 SRAM's in the SOJ package.

**For ceramic versions of this product, please see the MT5C1008 datasheet.*

PIN ASSIGNMENT

(Top View)

32-Pin Plastic SOJ (DJ)



PIN FUNCTIONS

A0 - A16	Address Inputs
WE	Write Enable
CE ₁ , CE ₂	Chip Enable
OE	Output Enable
I/O ₀ - I/O ₇	Data Inputs/Outputs
V _{CC}	Power
V _{SS}	Ground
NC	No Connection

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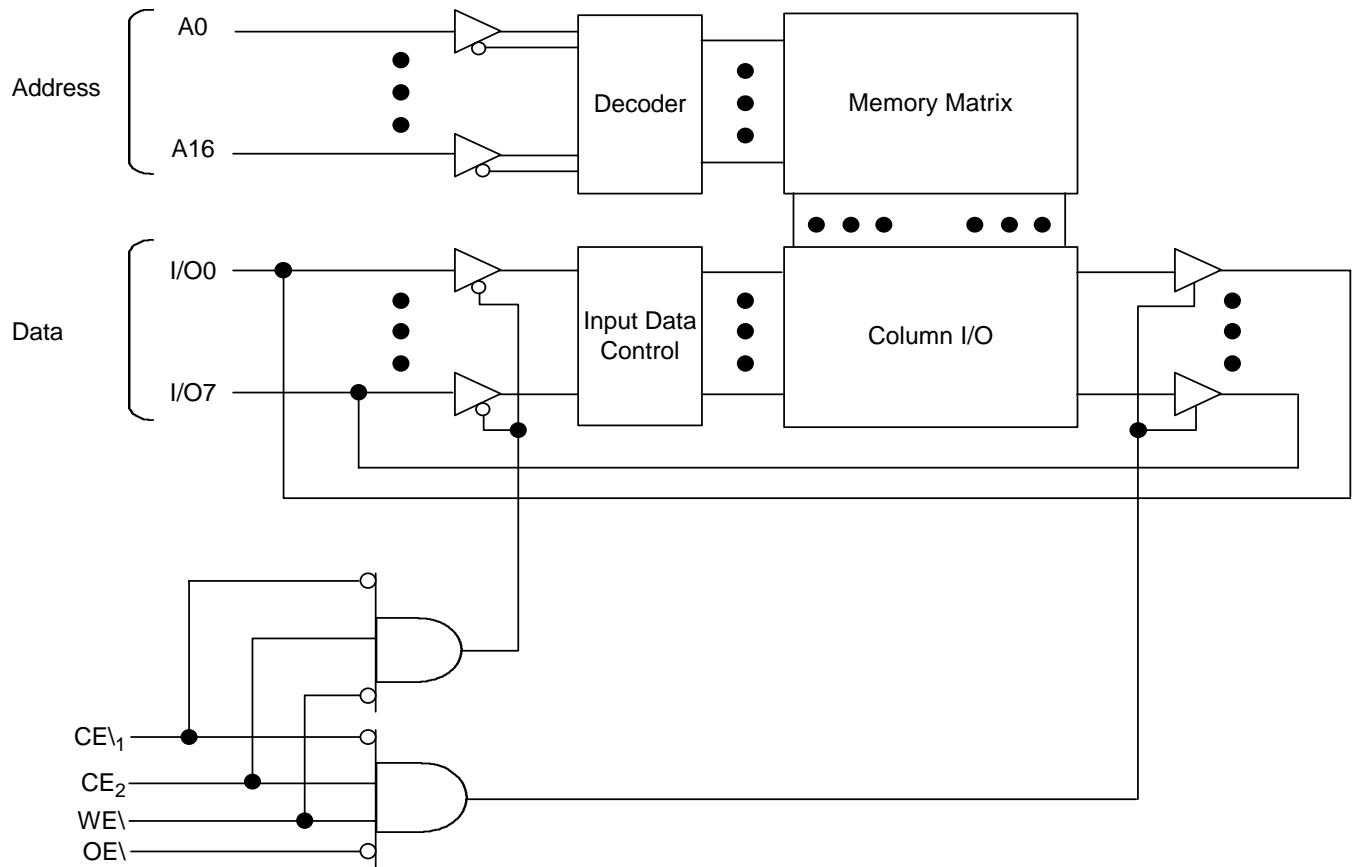


ABSOLUTE MAXIMUM RATINGS*

Vcc Supply Relative to GND.....-0.5V to +7.0V
Voltage on any pin Relative to GND.....-0.5V to Vcc +7.0V
Storage Temperature-65°C to +150°C
Ambient Temperature with Power Applied.....-55°C to +125°C
Short Circuit Output Current.....260°C
Power Dissipation.....1.0W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL BLOCK DIAGRAM





ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 10\%$)

PARAMETER	CONDITIONS	SYMBOL	-15		-20		-25		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Dynamic Operating Current	$V_{CC} = \text{MAX}$, $I_{OUT} = 0\text{mA}$, $CE_1 = V_{IL}$ and $CE_2 = V_{IH}$, $f = f_{max}$	I_{CC1}		180		150		140	mA
TTL Standby Current - TTL Inputs	$V_{CC} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} , $CE_1 \geq V_{IH}$ and $CE_2 \geq V_{IL}$, $f = f_{max}$	I_{SB1}		90		75		70	mA
CMOS Standby Current - CMOS Inputs	$V_{CC} = \text{MAX}$, $CE_1 \geq V_{CC} - 0.2\text{V}$, or $CE_2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ and $V_{IN} \leq 0.2\text{V}$, $f = 0$	I_{SB2}		10		10		10	mA
Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	I_{LI}	-10	10	-10	10	-10	10	μA
Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ Output Disabled	I_{LO}	-10	10	-10	10	-10	10	μA
Output High Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -4.0\text{mA}$	V_{OH}	2.4		2.4		2.4		V
Output Low Voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 8.0\text{mA}$	V_{OL}		0.4		0.4		0.4	V
Input High Voltage		V_{IH}	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
Input Low Voltage		V_{IL}	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

PIN DESCRIPTIONS

A0 - A16: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

CE₁: Chip Enable 1 Input

CE₁ is asserted LOW to read from or write to the device. If Chip Enable 1 is deasserted, the device is deselected and is in standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

CE₂: Chip Enable 2 Input

CE₂ is asserted HIGH to read from or write to the device. If Chip Enable 2 is deasserted, the device is deselected and is in standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

OE: Output Enable Input

The Output Enable Input is asserted LOW. If asserted LOW while CE₁ is asserted (LOW) and CE₂ is asserted (HIGH) and WE is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when OE is deasserted.

WE: Write Enable Input

The Write Enable input is asserted LOW and controls read and write operations. When CE₁ and WE are both asserted (LOW) and CE₂ is asserted (HIGH) input data present on the I/O pins will be written into the selected memory location.



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 10\%$)

DESCRIPTION	SYMBOL ¹	-15		-20		-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Enable Access Time	t_{ACE}		15		20		25	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Enable to Output in Low-Z	t_{LZCE}	3		3		3		ns
Chip Disable to Output in High-Z	t_{HZCE}		7		8		10	ns
Output Enable Access Time	t_{AOE}		7		7		10	ns
Output Enable to Output in Low-Z	t_{LZOE}	0		0		0		ns
Output Disable to Output in High-Z	t_{HZOE}		7		8		10	ns
WRITE CYCLE								
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Enable to End of Write	t_{CW}	12		15		20		ns
Address Valid to End of Write	t_{AW}	12		15		20		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Hold from End of Write	t_{AH}	0		0		0		ns
Write Pulse Width ($OE \geq V_{IH}$)	t_{WP}	12		15		20		ns
Data Set-up Time	t_{DS}	8		10		15		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Disable to Output in Low-Z	t_{LZWE}	5		5		5		ns
Write Enable to Output in High-Z	t_{HZWE}		7		9		10	ns

NOTE: 1. t_{LZCE} , t_{LZWE} , t_{HZCE} , t_{LZOE} , and t_{HZOE} are simulated values.



CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

PARAMETER	CONDITION	SYMBOL	MAX	UNIT
Input Capacitance	$V_{IN} = 0V$	C_{IN}	6	pF
Output Capacitance	$V_{OUT} = 0V$	C_{OUT}	8	pF

AC TEST CONDITIONS

Input Pulse Levels.....	GND to 3.0V
Input Rise and Fall Times.....	3ns
Input Timing Reference Levels.....	1.5V
Output Reference Levels.....	1.5V
Output Load.....	See Figure 1

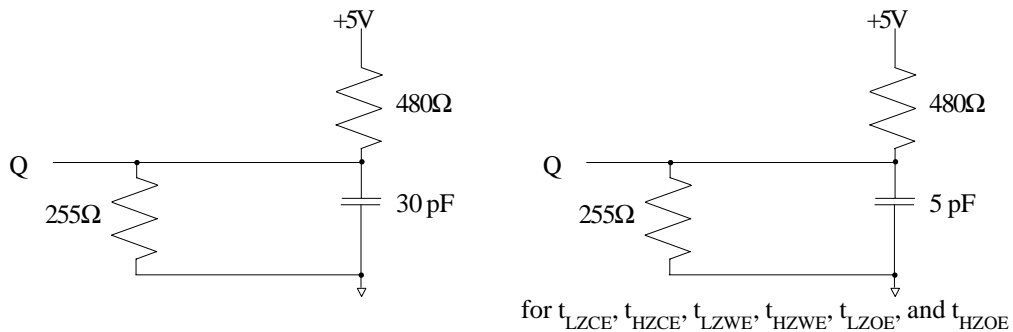
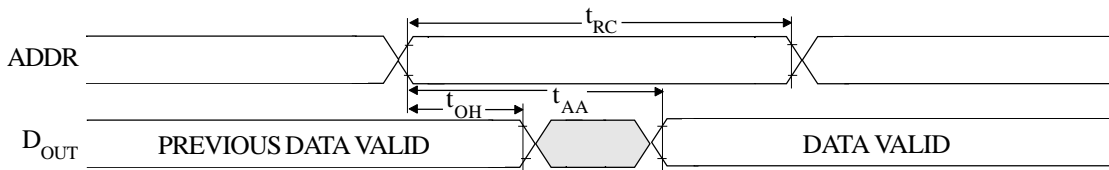


Fig. 1 OUTPUT LOAD EQUIVALENT

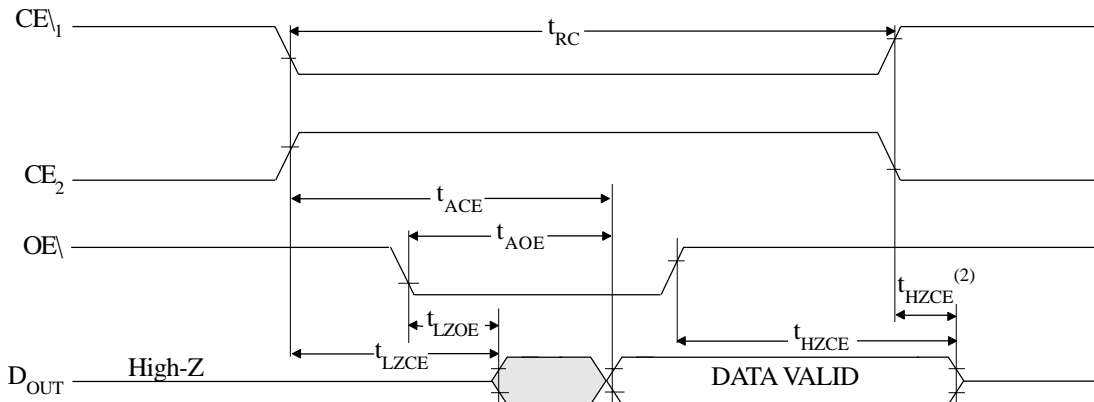


READ CYCLE TIMING 1⁽¹⁾



NOTE: 1. $CE\setminus$ is HIGH for READ cycle.

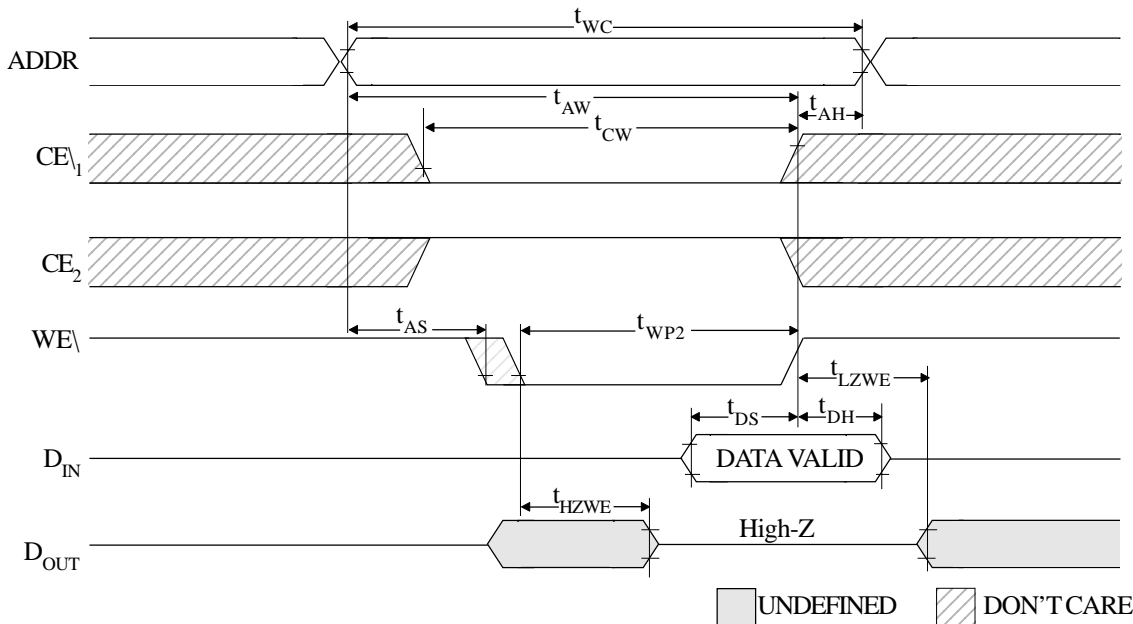
READ CYCLE TIMING 2⁽¹⁾



NOTES: 1. $CE\setminus$ is HIGH for READ cycle.

2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .

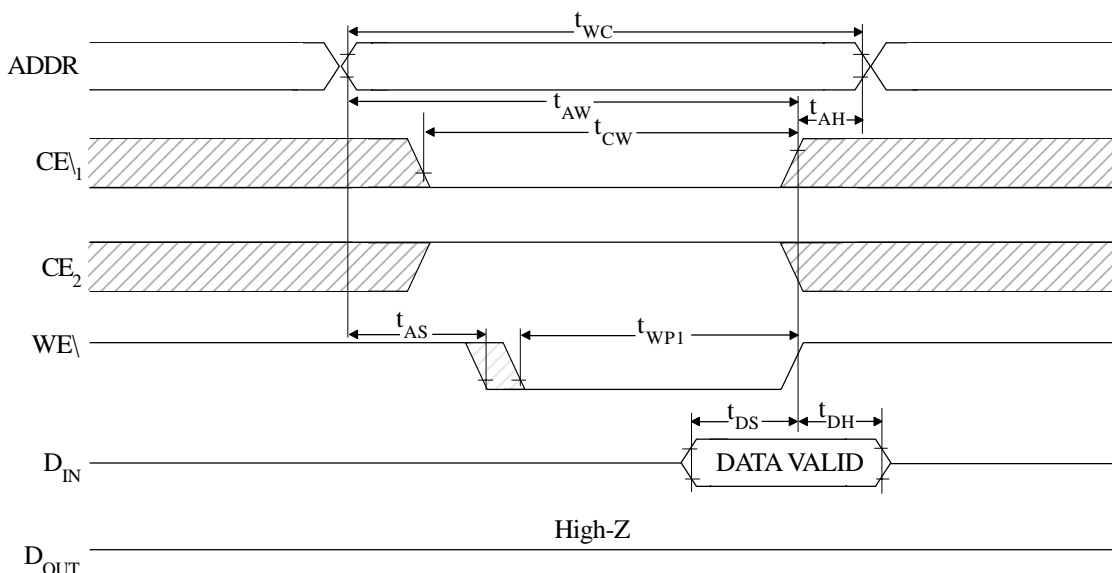
WRITE CYCLE TIMING ($WE\setminus$ CONTROLLED, $OE\setminus =$ LOW)



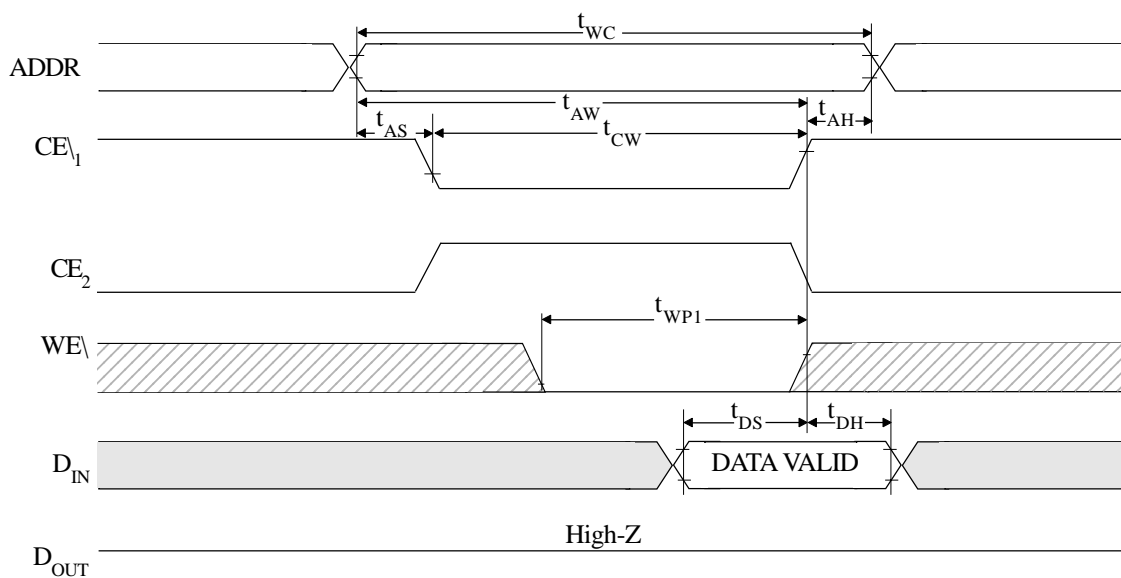
■ UNDEFINED ■ DON'T CARE



WRITE CYCLE TIMING (CE₁ CONTROLLED, OE₁ = LOW)



WRITE CYCLE TIMING (CE₂ CONTROLLED, OE₁ = LOW)

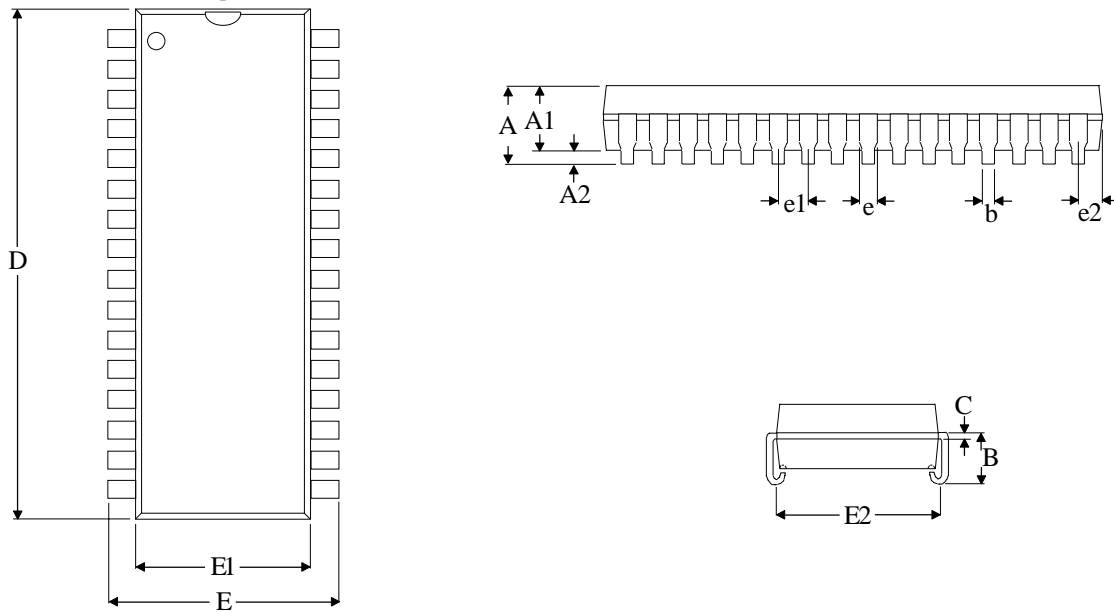


UNDEFINED DON'T CARE



MECHANICAL DEFINITION*

ASI Case #905 (Package Designator DJ)



SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	0.140 BSC	
A1	0.105	0.115
A2	0.027 TYP	
B	0.082	---
b	0.018 TYP	
C	0.010 TYP	
D	0.820	0.880
E	0.430	0.445
E1	0.395	0.405
E2	0.360	0.380
e	0.025	0.032
e1	0.050 TYP	
e2	---	0.045

* All measurements are in inches.



ORDERING INFORMATION

EXAMPLE: AS5C1008DJ-25/XT

Device Number	Package Type	Speed ns	Process
AS5C1008	DJ	-15	/*
AS5C1008	DJ	-20	/*
AS5C1008	DJ	-25	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range
XT = Extended Temperature Range

-40°C to +85°C
-55°C to +125°C