32K x 8 SRAM
SRAM MEMORY ARRAY

FEATURES
- Access Times: 12, 15, & 20ns
- Fast output enable (tDOE) for cache applications
- Low active power: 400 mW (TYP)
- Low power standby
- Fully static operation, no clock or refresh required
- High-performance, low-power CMOS double-metal process
- Single +5V (±10%) Power Supply
- Easy memory expansion with CE\
- All inputs and outputs are TTL compatible

OPTIONS MARKING

- Timing
  - 12ns access* -12
  - 15ns access -15
  - 20ns access -20

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- Package(s)**
  - Plastic SOJ DJ No. 906

- Operating Temperature Ranges
  - Military -55°C to +125°C XT
  - Industrial -40°C to +85°C IT

***** *-12 available in IT only.*

****** *For ceramic version of this product, see the MT5C2568 data sheet.*

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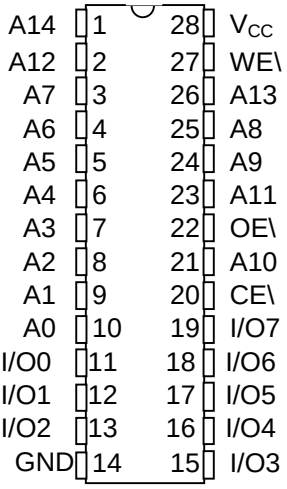
PIN ASSIGNMENT
(Top View)

28-PIN PSOJ (DJ)



GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low power CMOS designs using a four-transistor memory cell. These SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (CE\) and output enable (OE\) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

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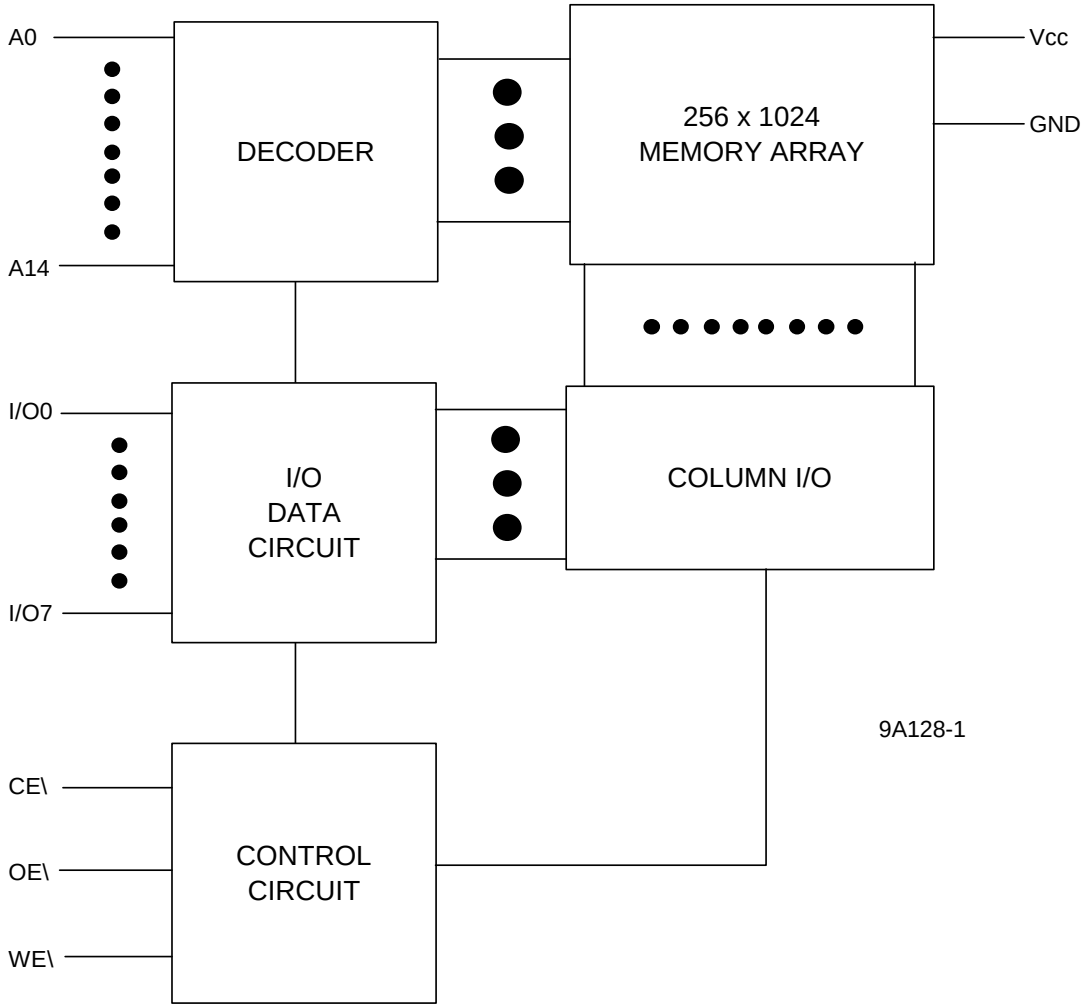
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE\	CE\	WE\	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Input or DQ Relative to Vss.....-0.5V to Vcc +0.5V
Voltage on Vcc Supply Relative to Vss.....-1V to +7V
Storage Temperature.....-65°C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....20mA
Lead Temperature (soldering 10 seconds).....+260°C
Max. Junction Temperature.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_C \leq 125^oC$ or -40^oC to $+85^oC$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq Vcc$	IL_I	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq Vcc$	IL_O	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

DESCRIPTION		CONDITIONS	SYM	MAX -12	MAX -15	MAX -20	UNITS	NOTES
Power Supply Current: Operating		CE\≤V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC (MIN) Output Open	Icc	190	165	150	mA	3
Power Supply Current: Standby	TTL_1	CE\≤V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC (MIN) Outputs Open	I_{SBT1}	60	50	45	mA	
	TTL_2	CE\≤V_{IH}; All Other Inputs ≤ V_{IL} or ≥ V_{IH}, Vcc = MAX f = 0 Hz	I_{SBT2}	25	25	25	mA	
	CMOS	CE\≥Vcc-0.2V; Vcc = MAX $V_{IN} \leq$ Vss+0.2V or $V_{IN} \geq$ Vcc -0.2V; f = 0 Hz	I_{SBC1}	5	5	5	mA	

CAPACITANCE

PARAMETER	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25_oC$, f = 1MHz Vcc = 5V	C_{IN}	8	pF	4
Input/Output Capacitance		C_{IO}	10	pF	4

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{o}C \leq T_C \leq 125^{o}C$ or $-40^{o}C$ to $+85^{o}C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYM	-12		-15		-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE									
READ cycle time	t_{RC}	12		15		20		ns	
Address access time	t_{AA}		12		15		20	ns	
Chip enable access time	t_{ACE}		12		15		20	ns	
Output hold from address change	t_{OH}	2		2		2		ns	
Chip enable to output in Low-Z	t_{LZCE}	2		2		2		ns	7
Chip disable to output in High-Z	t_{HZCE}		7		8		9	ns	6, 7
Chip enable to power-up time	t_{PU}	0		0		0		ns	4
Chip disable to power-down time	t_{PD}		12		15		20	ns	4
Output enable to access time	t_{AOE}		6		7		8	ns	
Output enable to output in Low-Z	t_{LZOE}	0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		6		7		8	ns	6
WRITE CYCLE									
WRITE cycle time	t_{WC}	12		15		20		ns	
Chip enable to end of write	t_{CW}	9		10		12		ns	
Address valid to end of write	t_{AW}	9		10		12		ns	
Address setup time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		ns	
WRITE pulse width	t_{WP}	10		12		15		ns	
Data setup time	t_{DS}	7		8		10		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		ns	7
Write enable to output in High-Z	t_{HZWE}	0	7	0	7	0	9	ns	6, 7

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AC TEST CONDITIONS

Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 & 2

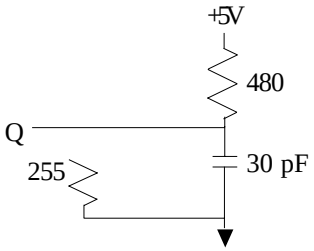


Fig. 1
OUTPUT LOAD
EQUIVALENT

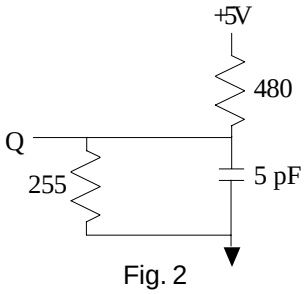


Fig. 2
OUTPUT LOAD
EQUIVALENT

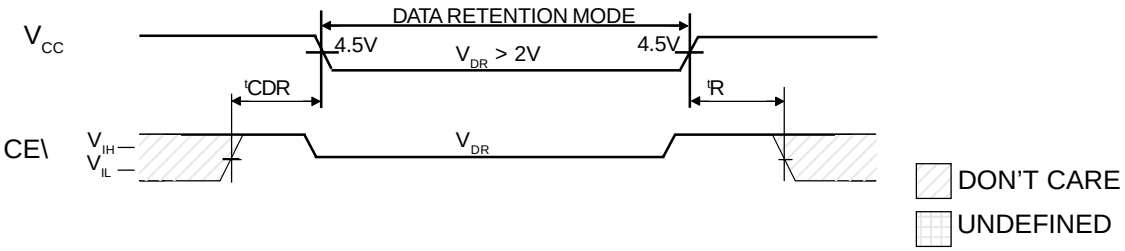
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and
   $$f = \frac{1}{{}^{t}RC\ (MIN)}\ Hz.$$
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^{t}HZCE$, ${}^{t}HZOE$ and ${}^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ${}^{t}HZCE$ is less than ${}^{t}LZCE$, and ${}^{t}HZWE$ is less than ${}^{t}LZWE$.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^{t}RC$ = Read Cycle Time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2	--	V	
Data Retention Current	CE\ ≥ (V_{CC} - 0.2V) V_{IN} ≥ (V_{CC} - 0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		1.0	mA	
		V_{CC} = 3V			2.0	mA	
Chip Deselect to Data Retention Time			${}^{t}CDR$	0	--	ns	4
Operation Recovery Time			${}^{t}R$	${}^{t}RC$		ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM



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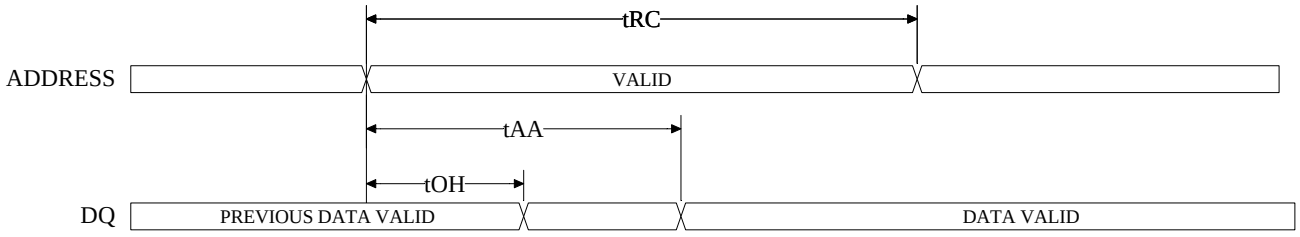
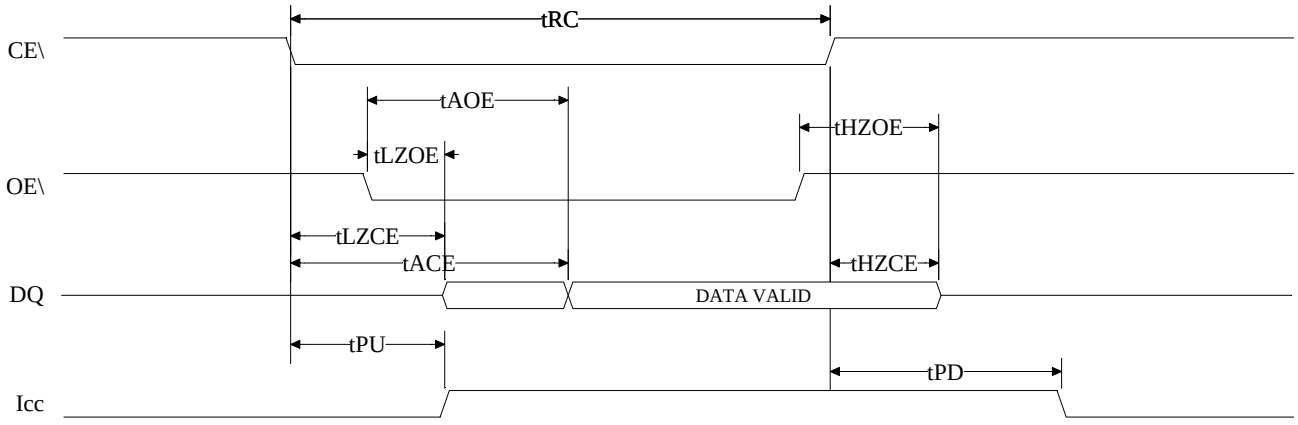
READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10, 12]

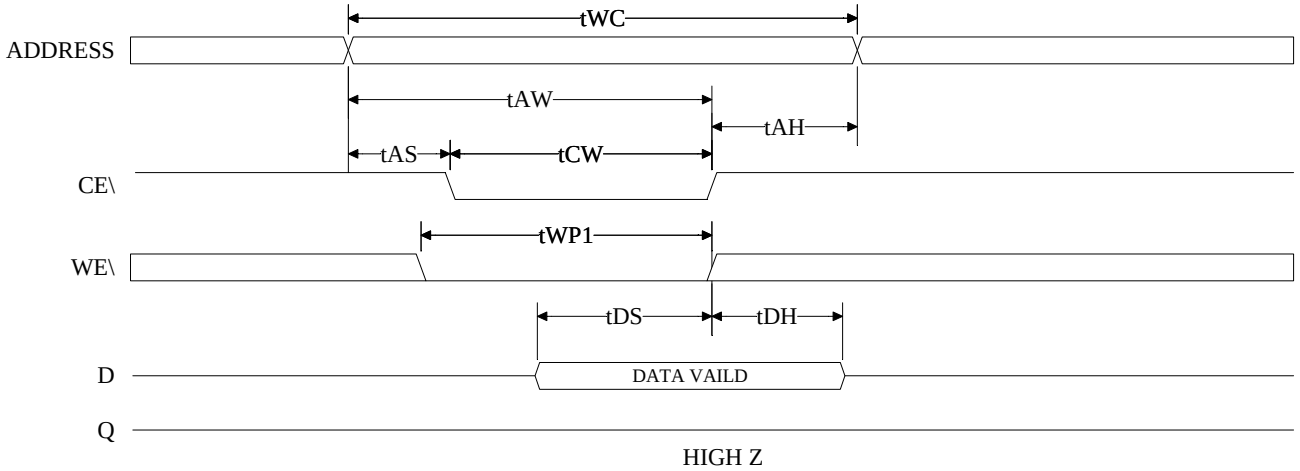


DON'T CARE

UNDEFINED

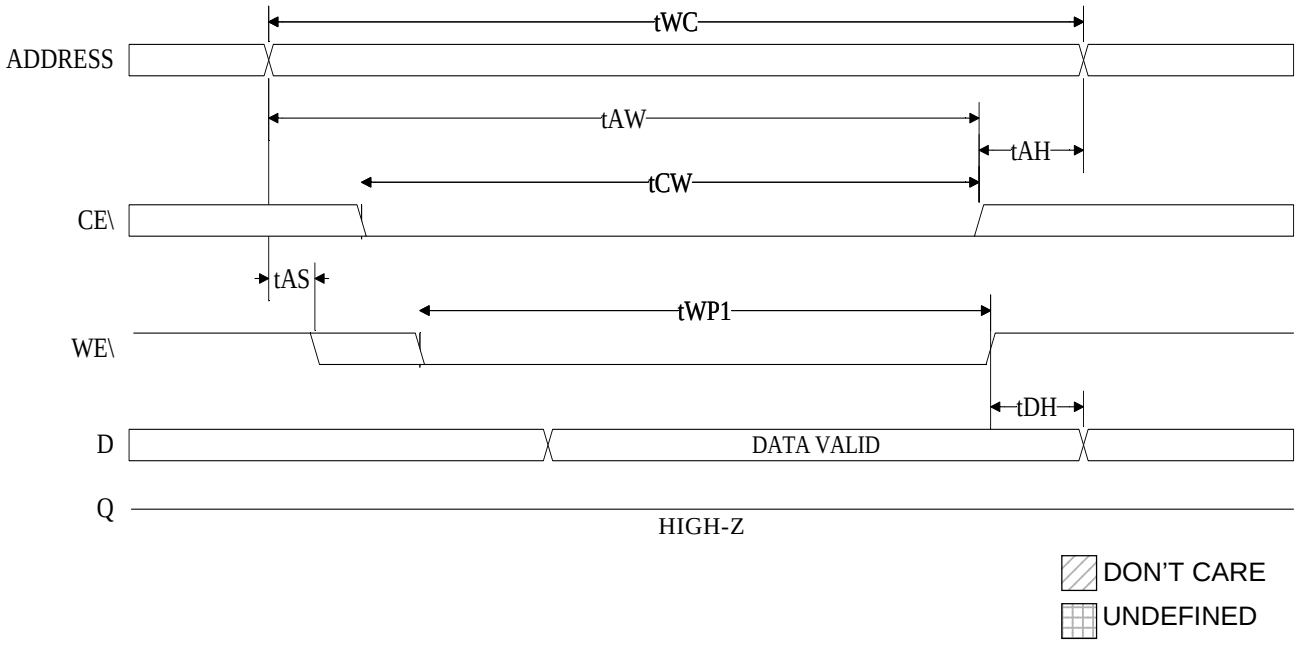
WRITE CYCLE NO. 1 [12]

(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [7, 12]

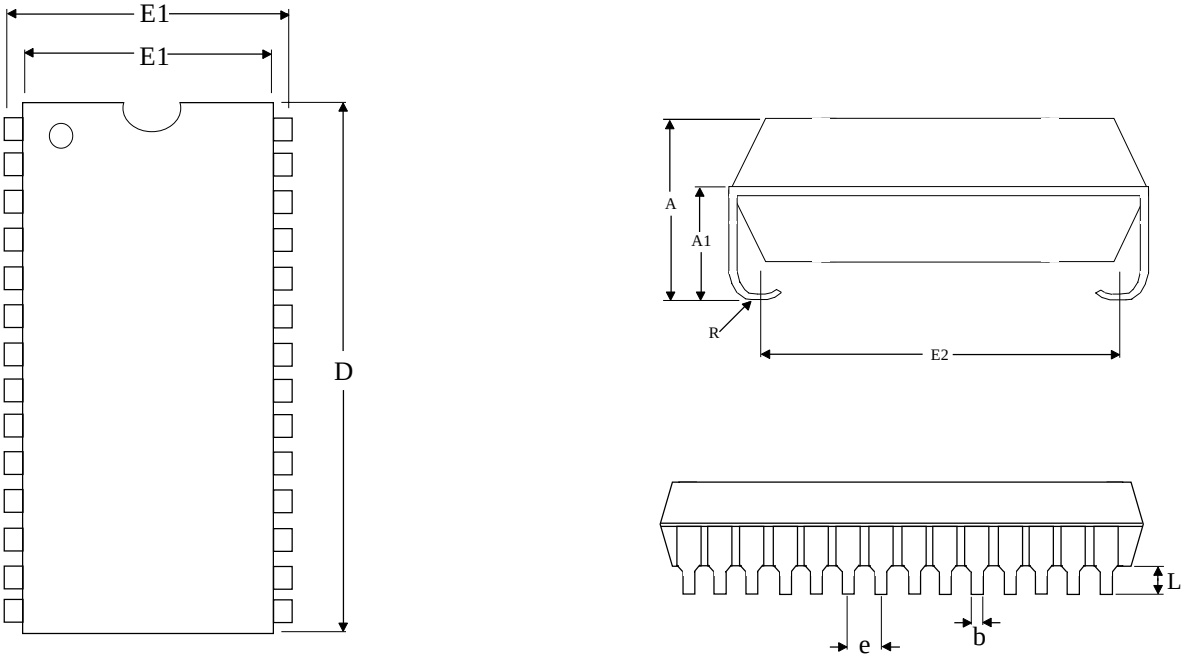
(Write Enabled Controlled)



NOTE: Output enable (OE\) is inactive (HIGH).

MECHANICAL DEFINITIONS*

ASI Case #906 (Package Designator DJ)



SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	---	0.140
b	0.018 TYP	
D	---	0.73
E	0.327	0.347
E1	0.295	0.305
E2	0.245	0.285
e	0.050 BSC	
L	0.025	---

**** All measurements are in inches.***

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ORDERING INFORMATION

EXAMPLE: AS5C2568DJ-15/IT

Device Number	Package Type	Speed ns	Process
AS5C2568	DJ	-12	/*
AS5C2568	DJ	-15	/*
AS5C2568	DJ	-20	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

12ns offered in IT only