



## 128K x 8 SRAM

High-Speed CMOS SRAM with  
3.3V Revolutionary Pinout

### FEATURES

- High-speed access times of 10, 12, 15 and 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with CE\ and OE\ options
- CE\ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply

### OPTIONS

- Timing
  - 10ns access
  - 12ns access
  - 15ns access
  - 20ns access

### MARKING

- Package
 

Plastic SOJ (32-pin, 400-mil)	DJ	No. 906
*Ceramic SOJ (32-pin, 400-mil)	DCJ	No. 501
- Operating Temperature Ranges
 

-Military (-55°C to +125°C)	XT
-Industrial (-40°C to +85°C)	IT

*\*Consult Factory, Possible Future Offering*

### GENERAL DESCRIPTION

The ASI AS5LC1008 is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM in revolutionary pinout. The AS5LC1008 is fabricated using high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

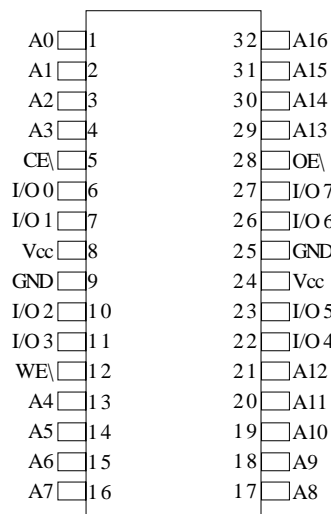
When CE\ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250μW (typical) with CMOS input levels.

The AS5LC1008 operates from a single 3.3V power supply and all inputs are TTL-compatible.

### PIN ASSIGNMENT

(Top View)

32-Pin, 400-mil  
Plastic SOJ (DJ) & Ceramic SOJ (DCJ)



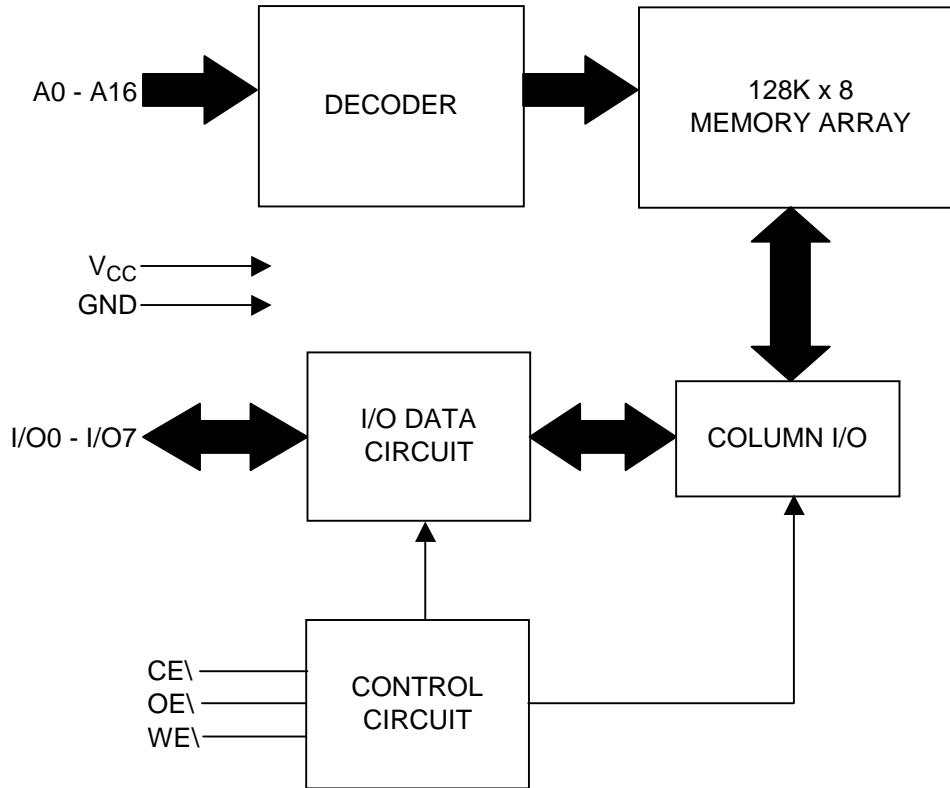
### PIN FUNCTIONS

PIN	DESCRIPTION
A0 - A16	Address Inputs
CE\	Chip Enable Input
OE\	Output Enable Input
WE\	Write Enable Input
I/O0 - I/O7	Bidirectional Ports
V <sub>CC</sub>	Power
GND	Ground

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**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS\***

Terminal Voltage with Respect to GND ( $V_{TERM}$ ).....	-0.5V to $V_{CC} + 0.5V$
Temperature Under Bias ( $T_{BIAS}$ ).....	-55°C to +125°C
Storage Temperature ( $T_{STG}$ ).....	-65°C to +150°C
Power Dissipation ( $P_T$ ).....	1.0W

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TRUTH TABLE**

Mode	WE\	CE\	OE\	I/O Operation	$V_{CC}$ Current
Not Selected (Power-down)	X	H	X	High-Z	$I_{SB1}, I_{SB2}$
Output Disabled	H	L	H	High-Z	$I_{CC1}, I_{CC2}$
Read	H	L	L	$D_{OUT}$	$I_{CC1}, I_{CC2}$
Write	L	L	X	$D_{IN}$	$I_{CC1}, I_{CC2}$



**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(-55°C < T<sub>A</sub> < +125°C or -40°C to +85°C; V<sub>CC</sub> = 3.3V ±0.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0mA	2.4	---	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0mA	---	0.4	V
Input HIGH Voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> + 0.3	V
Input LOW Voltage <sup>1</sup>	V <sub>IL</sub>		-0.3	0.8	V
Input Leakage	I <sub>LI</sub>	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-5	5	μA
Output Leakage	I <sub>LO</sub>	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> ; Outputs Disabled	-5	5	μA

NOTE: 1. V<sub>IL</sub> = -3.0V for pulse width less than 10ns.

**POWER SUPPLY CHARACTERISTICS<sup>1</sup>**

(-55°C < T<sub>A</sub> < +125°C or -40°C to +85°C; V<sub>CC</sub> = 3.3V ±0.3V)

PARAMETER	SYM	CONDITIONS	-10		-12		-15		-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub> Dynamic Operating Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = Max, CE\ = V <sub>IL</sub> , I <sub>OUT</sub> = 0 mA, f = Max	---	160	---	140	---	130	---	120	mA
TTL Standby Current (TTL Inputs)	I <sub>SB</sub>	V <sub>CC</sub> = Max, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , CE\ ≥ V <sub>IH</sub> , f = Max	---	45	---	40	---	35	---	30	mA
	I <sub>SB1</sub>	V <sub>CC</sub> = Max, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , CE\ ≥ V <sub>IH</sub> , f = 0	---	30	---	30	---	30	---	30	mA
CMOS Standby Current (CMOS Inputs)	I <sub>SB2</sub>	V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	---	10	---	10	---	10	---	10	mA

NOTE: 1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**CAPACITANCE<sup>1,2</sup>**

PARAMETER	SYMBOL	CONDITIONS	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	8	pF

NOTE:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1MHz, V<sub>CC</sub> = 3.3V.



**READ CYCLE SWITCHING CHARACTERISTICS<sup>1</sup>**

( $-55^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

PARAMETER	SYMBOL	-10		-12		-15		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	$t_{RC}$	10	---	12	---	15	---	20	---	ns
Address Access Time	$t_{AA}$	---	10	---	12	---	15	---	20	ns
Output Hold time	$t_{OHA}$	2	---	2	---	2	---	2	---	ns
CE\ Access Time	$t_{ACE}$	---	10	---	12	---	15	---	20	ns
OE\ Access Time	$t_{DOE}$	---	5	---	6	---	7	---	8	ns
OE\ to Low-Z Output	$t_{LZOE}^2$	0	---	0	---	0	---	0	---	ns
OE\ to High-Z Output	$t_{HZOE}^2$	0	5	0	6	0	7	0	8	ns
CE\ to Low-Z Output	$t_{LZCE}^2$	2	---	2	---	2	---	2	---	ns
CE\ to High-Z Output	$t_{HZCE}^2$	0	5	0	6	0	7	0	8	ns

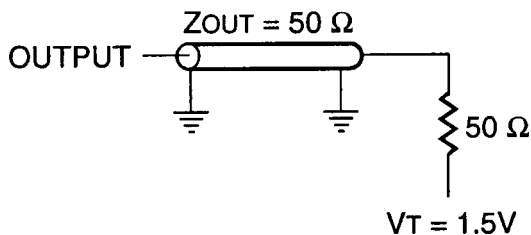
**NOTES:**

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and C1 output loading specified in Figure 1.
2. Tested with the C2 load in Figure 1. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

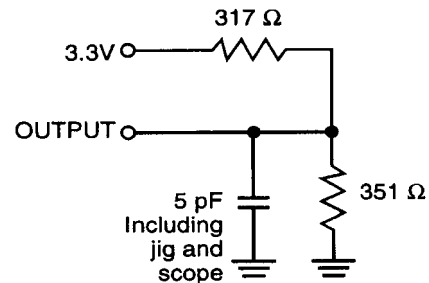
**AC TEST CONDITIONS**

PARAMETER	UNIT
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

**AC TEST LOADS**



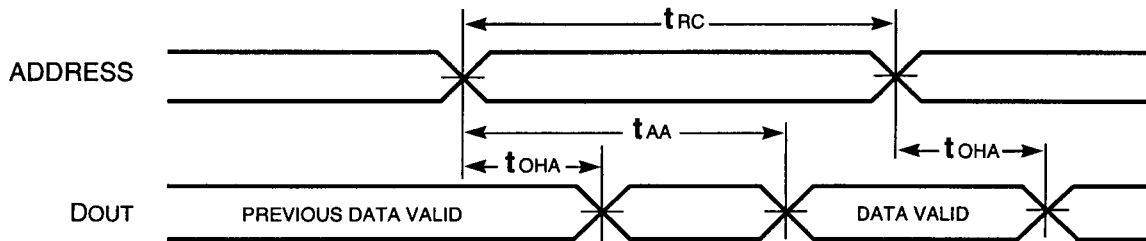
**FIGURE 1**



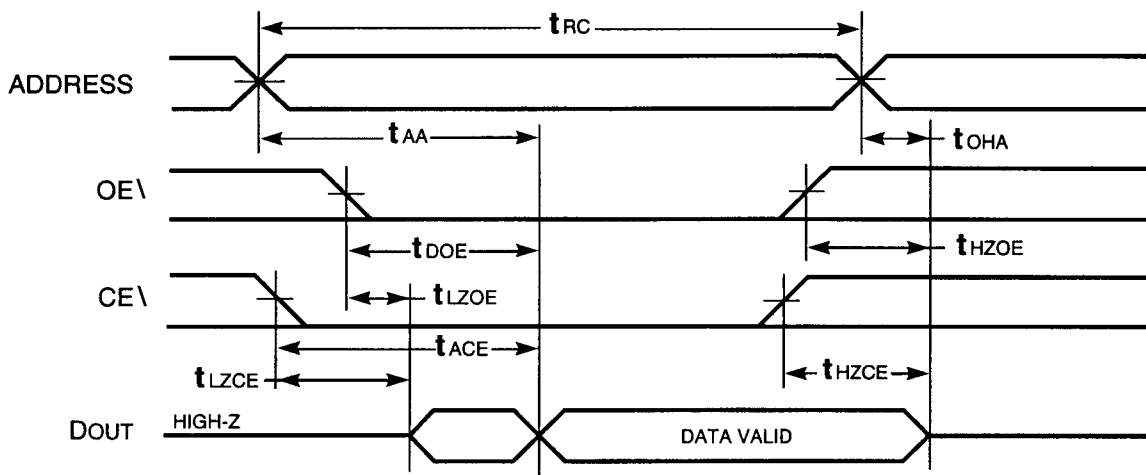
**FIGURE 2**



### READ CYCLE #1<sup>1,2</sup>



### READ CYCLE #2<sup>1,3</sup>



#### NOTES:

1.  $WE$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $OE$ ,  $CE$  =  $V_{IL}$ .
3. Address is valid prior to or coincident with  $CE$  LOW transitions.



**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>1,3</sup>**

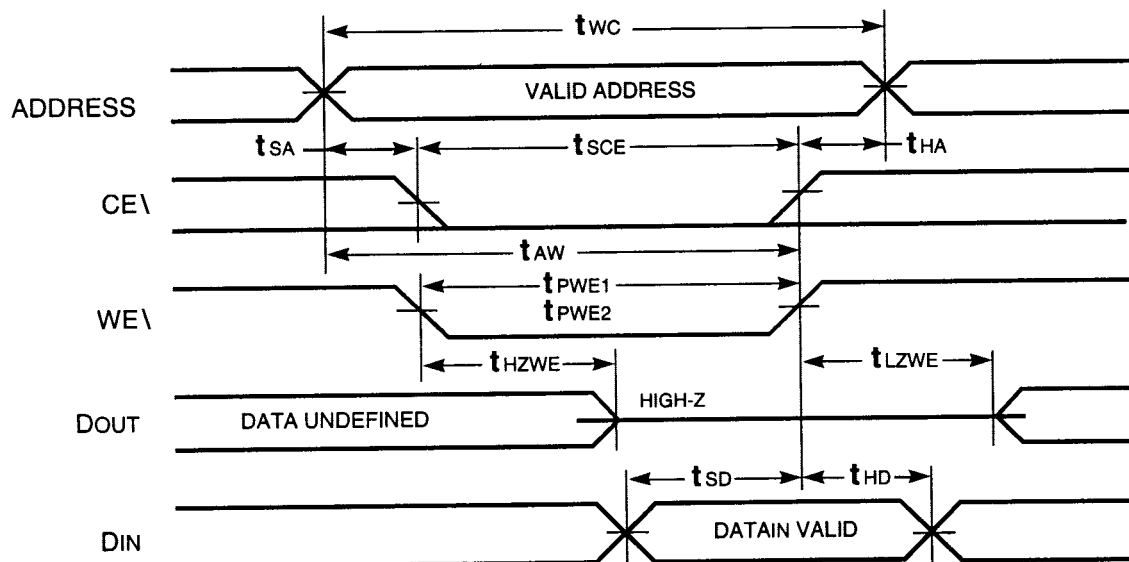
(-55°C < T<sub>A</sub> < +125°C or -40°C to +85°C; V<sub>cc</sub> = 3.3V ±0.3V)

PARAMETER	SYMBOL	-10		-12		-15		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t <sub>WC</sub>	10	---	12	---	15	---	20	---	ns
CE\ to Write End	t <sub>SCE</sub>	7	---	8	---	9	---	10	---	ns
Address Setup Time to Write End	t <sub>AW</sub>	8	---	9	---	10	---	12	---	ns
Address Hold from Write End	t <sub>HA</sub>	0	---	0	---	0	---	0	---	ns
Address Setup Time	t <sub>SA</sub>	0	---	0	---	0	---	0	---	ns
WE\ Pulse Width (OE\ HIGH)	t <sub>PWE1</sub> <sup>1</sup>	7	---	8	---	9	---	10	---	ns
WE\ Pulse Width (OE\ LOW)	t <sub>PWE2</sub> <sup>2</sup>	10	---	12	---	12	---	15	---	ns
Data Setup to Write End	t <sub>SD</sub>	5	---	6	---	7	---	8	---	ns
Data Hold to Write End	t <sub>HD</sub>	0	---	0	---	0	---	0	---	ns
WE\ LOW to High-Z Output	t <sub>HZWE</sub> <sup>2</sup>	---	5	---	6	---	7	---	8	ns
WE\ HIGH to Low-Z Output	t <sub>LZWE</sub> <sup>2</sup>	2	---	2	---	2	---	2	---	ns

**NOTES:**

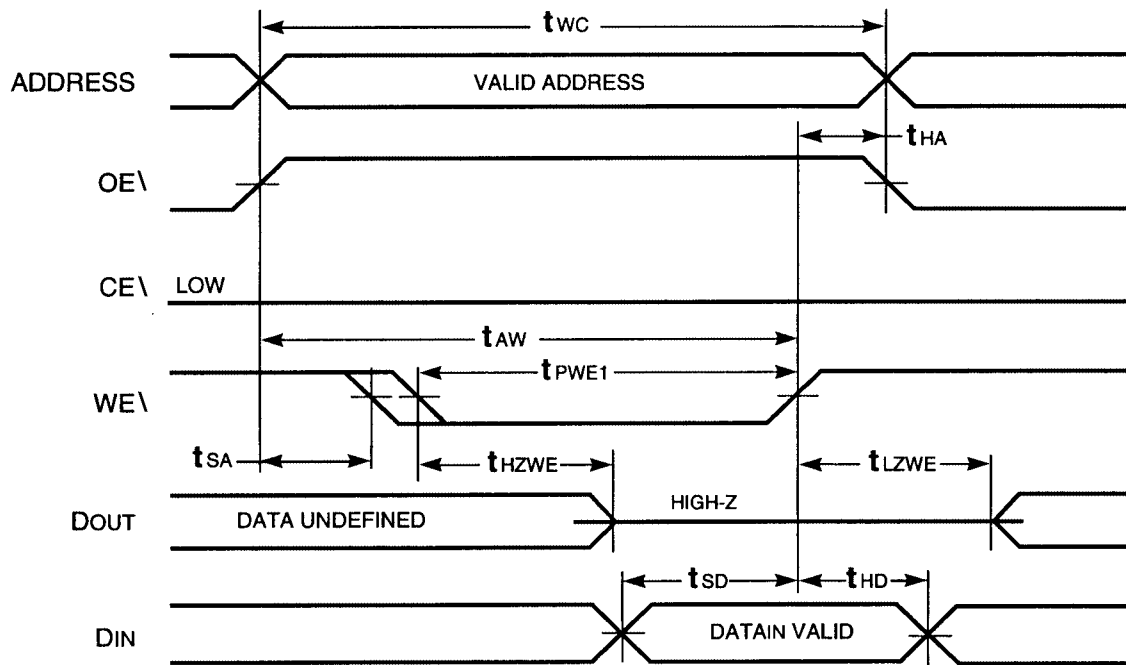
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE\ LOW and WE\ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

**WRITE CYCLE #1<sup>1,2</sup> (CE\ Controlled, OE\ = HIGH or LOW)**

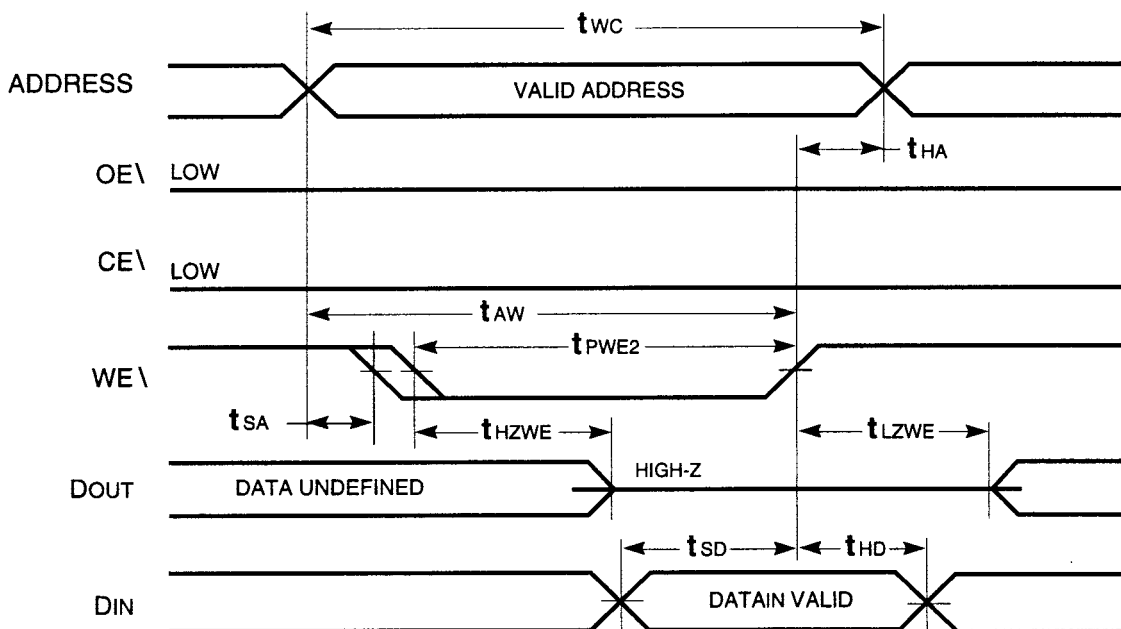




**WRITE CYCLE #2<sup>1</sup>** (WE\ Controlled, OE\ = HIGH during Write Cycle)



**WRITE CYCLE #3** (WE\ Controlled, OE\ = LOW during Write Cycle)

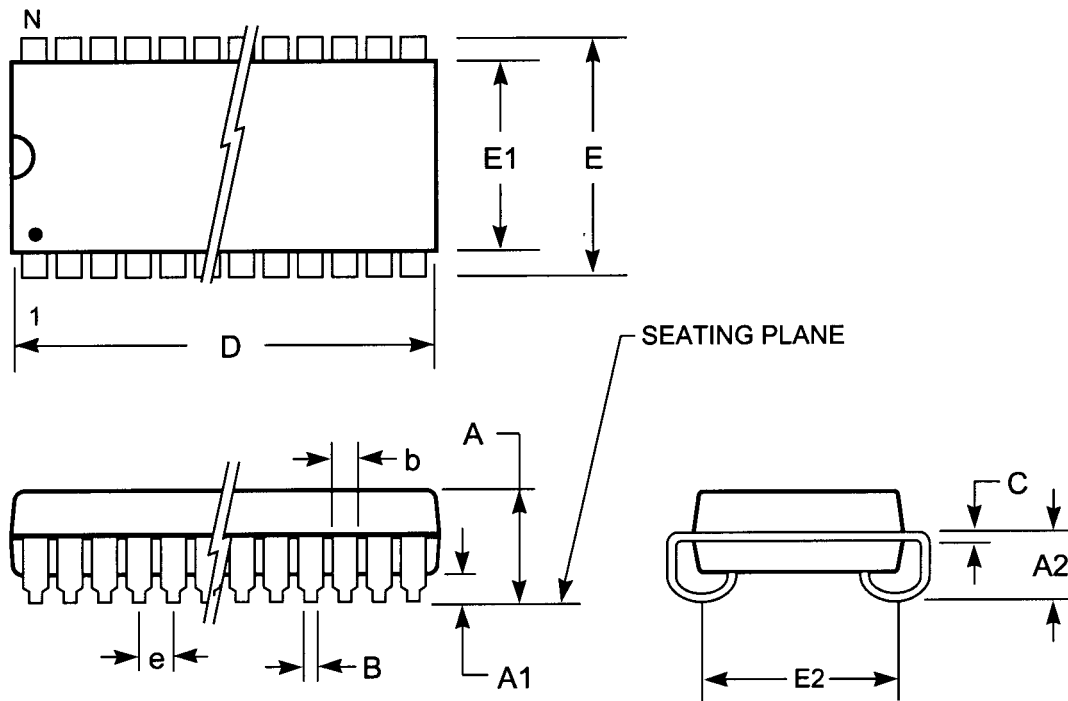


**NOTES:**

1. The internal write time is defined by the overlap of CE\ LOW and WE\ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if OE\ • V<sub>IH</sub>.

### MECHANICAL DEFINITION\*

ASI Case #906 (Package Designator DJ)



SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	0.128	0.148
A1	0.025	---
A2	0.082	---
B	0.015	0.020
b	0.026	0.032
C	0.007	0.013
D	0.820	0.830
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
e	0.050 BSC	

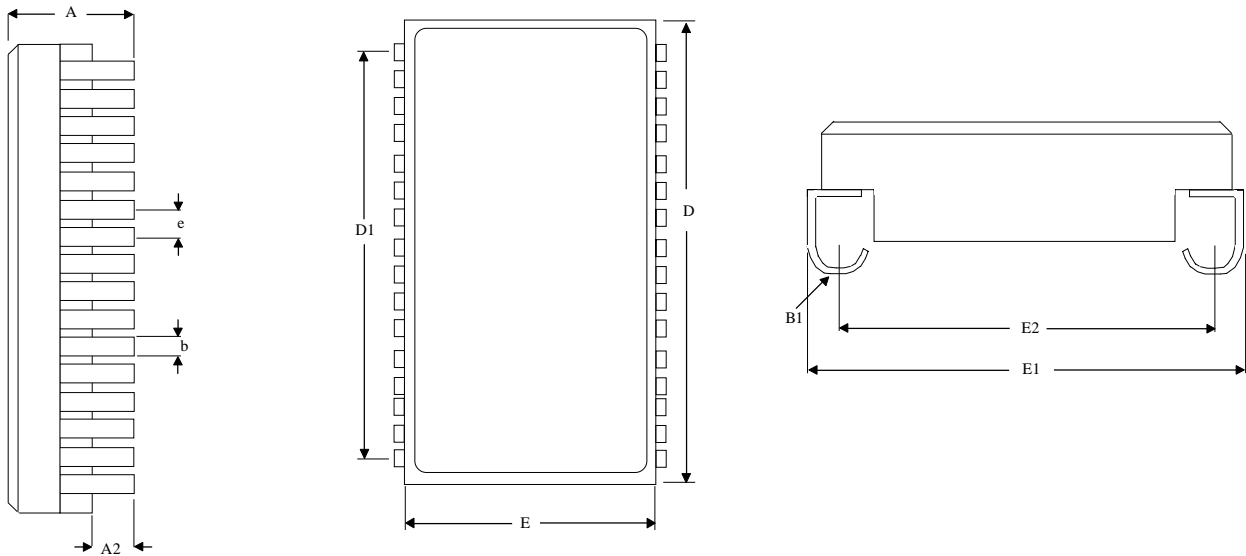
\* All measurements are in inches.





**MECHANICAL DEFINITIONS\***

ASI Case #501 (Package Designator DCJ)  
POSSIBLE FUTURE OFFERING, CONTACT FACTORY



SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	0.132	0.144
A2	0.026	0.036
B1	0.030	0.040
B1	0.015	0.019
D	0.812	0.828
D1	0.740	0.760
E	0.405	0.415
E1	0.435	0.445
E2	0.360	0.380
e	0.050 BSC	

\*All measurements are in inches.



## ORDERING INFORMATION

EXAMPLE: AS5LC1008DJ-12/XT

Device Number	Package Type	Speed ns	Process
AS5LC1008	DJ	-10	/*
AS5LC1008	DJ	-12	/*
AS5LC1008	DJ	-15	/*
AS5LC1008	DJ	-20	/*

EXAMPLE: AS5LC1008DCJ-10/IT

Device Number	Package Type	Speed ns	Process
AS5LC1008	DCJ	-10	/*
AS5LC1008	DCJ	-12	/*
AS5LC1008	DCJ	-15	/*
AS5LC1008	DCJ	-20	/*

### \*AVAILABLE PROCESSES

IT = Industrial Temperature Range

XT = Military Temperature Range

-40°C to +85°C

-55°C to +125°C