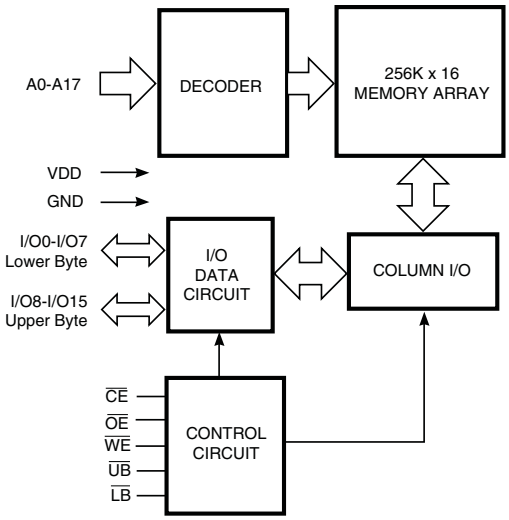
256K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM

FEATURES

- High-speed access time: 10, 15 & 20ns
- Available in Mil-Temp*, Enhanced & Industrial Ranges
- Low Active Power: 85 mW (typical)
- Low Standby Power: 7 mW (typical) CMOS standby
- Single power supply: V_{DD} = 3.3V ± 5%
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- TSOPII in copper lead frame for superior thermal performance
- RoHs compliant options available

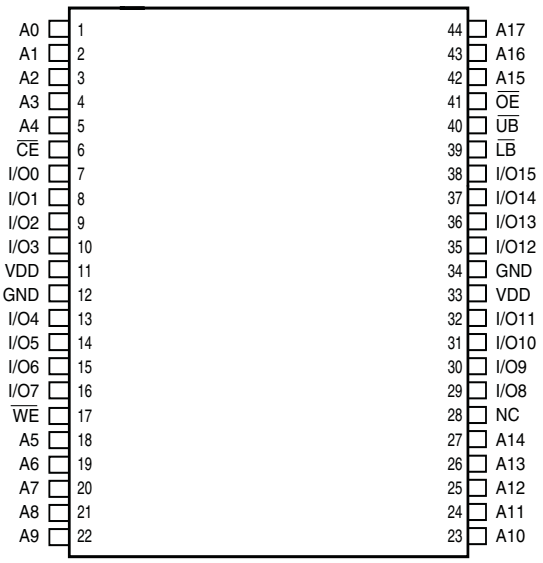
*Consult factory for /XT product.

FUNCTIONAL BLOCK DIAGRAM



For more products and information please visit our web site at
www.micross.com

PIN CONFIGURATIONS
44-pin TSOPII



A0-A17	Address Inputs
I/Oo-I/O15	Data Inputs / Outputs
CE\	Chip Enable Input
OE\	Output Enable Input
WE\	Write Enable Input
LB\	Lower-byte Control (I/O0-I/O7)
UB\	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

GENERAL DESCRIPTION

The Micross AS5LC256K16 is a high-speed, 4,194,304-bit static RAM organized as 262,144 words by 16 bits. It is fabricated using Micross' high performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CE\ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, CE\ and OE\. The active LOW Write Enable (WE\) controls both writing and reading of the memory. A data byte allows Upper Byte (UB) and Lower Byte (LB) access.

The AS5LC256K16 is packaged in JEDEC standard 44-pin TSOPII in copper lead frame for superior thermal performance. RoHs compliant options are available.

TRUTH TABLE

Mode	WE\	CE\	OE\	LB\	UB\	I/O PIN		V_{DD} Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)
V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	-	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	-	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		-0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	-1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	-1	1	µA

Note:

1. V_{IL}(min.) = –0.3V DC; Vil (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

THERMAL RESISTANCE

Parameter	Description	Test Conditions	44 TSOPII	Unit
Θ JA	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	51.4	°C/W
Θ JC	Thermal Resistance (Junction to Case)		9.64	°C/W

AC TEST CONDITIONS

Parameter	V_{DD} = 3.3V ±5%
Input Pulse Level	0V to 3V
Input Rise and Fall Times	1V/ns
Input and Output Timing and Reference Level (V_{REF})	1.5V
Output Load	See Figures 1 & 2

AC TEST LOADS

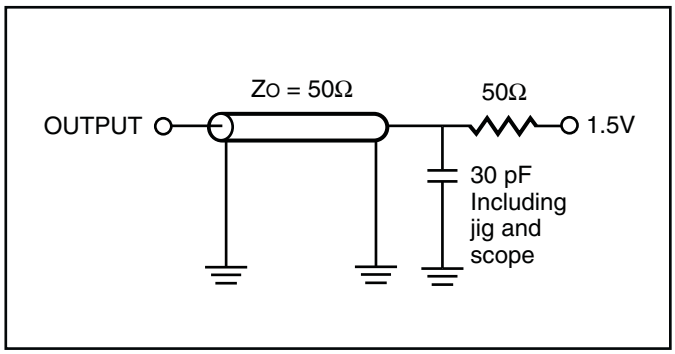


Figure 1.

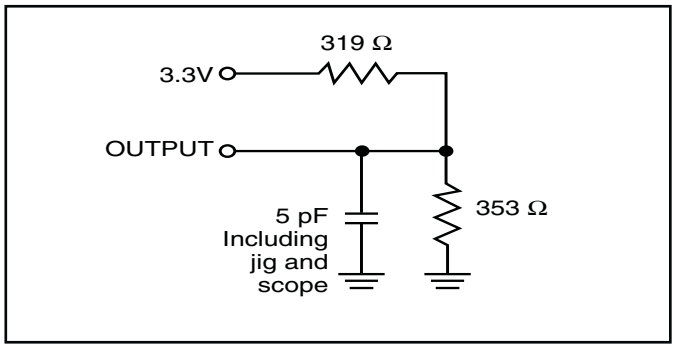


Figure 2.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
V_{DD}	V_{DD} Relates to GND	-0.3 to 4.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max	Min
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: Ta = 25°C, f = 1 MHz, Vdd = 3.3V.

OPERATING RANGE (V_{DD}=3.3V ±5%)

Range	Ambient Temperature
Industrial	-40°C to +85°C
Enhanced	-40°C to +105°C
Military	-55°C to +125°C

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Condition	-10	-15	-20	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	65	60	60	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	60	60	60	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL}, CE\ ≥V_{IH}, f=0	30	30	30	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., CE\ ≥V_{DD} - 0.2V, V_{IN} ≥V_{DD} - 0.2V, or V_{IN}≤0.2V, F=0	20	20	20	mA

Notes:

1. At f = fmax, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at Vdd = 3.3V, Ta = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

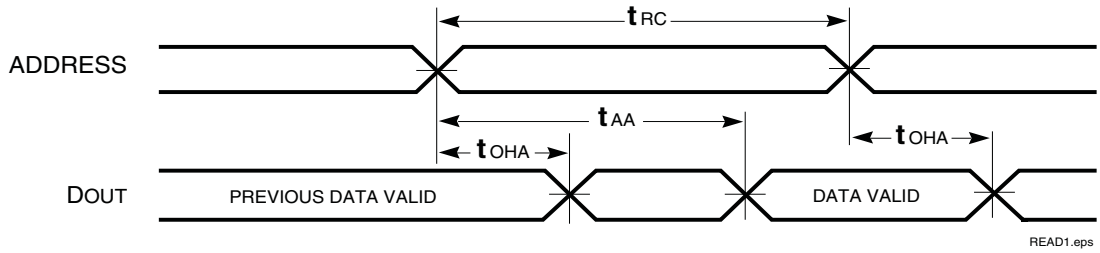
Symbol	Parameter	-10		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10	-	15	-	20	-	ns
t_{AA}	Address Access Time	0	10	-	15	-	20	ns
t_{CHA}	Output Hold Time	2.0	-	2.0	-	2	-	ns
t_{ACE}	CE\ Access Time	-	10	-	15	-	20	ns
t_{DOE}	OE\ Access Time	-	4.5	-	6	-	8	ns
t_{HZOE}[2]	OE\ to High-Z Output	-	4	-	6	-	8	ns
t_{LZOE}[2]	OE\ to Low-Z Output	0	-	0	-	0	-	ns
t_{HZCE}[2]	CE\ to High-Z Output	0	4	0	6	0	8	ns
t_{LZCE}[2]	CE\ to Low-Z Output	2	-	2	-	2	-	ns
t_{BA}	LB\, UB\ Access Time	-	6.5	-	7	-	8	ns
t_{HZB}[2]	LB\, UB\ to High-Z Output	0	4	0	6	0	8	ns
t_{LZB}[2]	LB\, UB\ to Low-Z Output	0	-	0	-	0	-	ns

Notes:

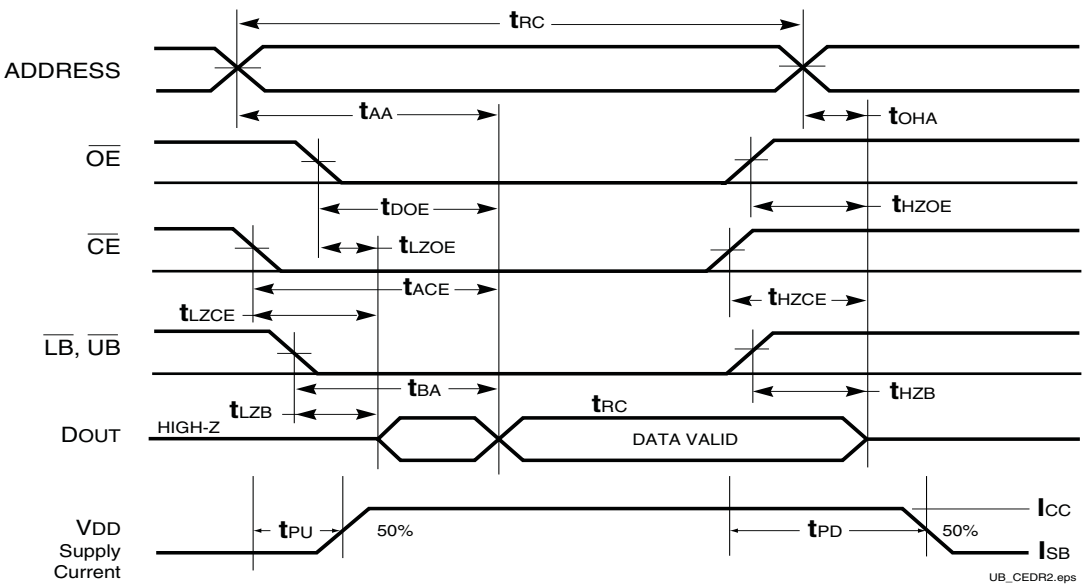
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) (CE\ = OE\ = V_{IL}, UB\ or LB\ = V_{IL})



READ CYCLE NO. 2[1,3]



NOTES:

1. WE\ is HIGH for a Read Cycle.
2. The device is continuously selected. OE\, CE\, UB\, or LB\ = V_{IL}.
3. Address is valid prior to or coincident with CE\ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10	-	15	-	20	-	ns
t_{SCE}	CE\ to Write End	8	-	10	-	12	-	ns
t_{AW}	Address to Setup Time to Write End	8	-	10	-	12	-	ns
t_{HA}	Address Hold from Write End	0	-	0	-	0	-	ns
t_{SA}	Address Setup Time	0	-	0	-	0	-	ns
t_{PWB}	LB\, UB\ Valid to End of Write	8	-	10	-	12	-	ns
t_{PWE1}	WE\ Pulse Width	8	-	10	-	12	-	ns
t_{PWE2}	WE\ Pulse Width (OE\=LOW)	10	-	15	-	17	-	ns
t_{SD}	Data Setup to Write End	6	-	7	-	9	-	ns
t_{HD}	Data Hold from Write End	0	-	0	-	0	-	ns
$t_{HZWE}2$	WE\ LOW to High-Z Output	-	5	-	7	-	9	ns
$t_{LZWE}2$	WE\ HIGH to Low-Z Output	1	-	1	-	1	-	ns

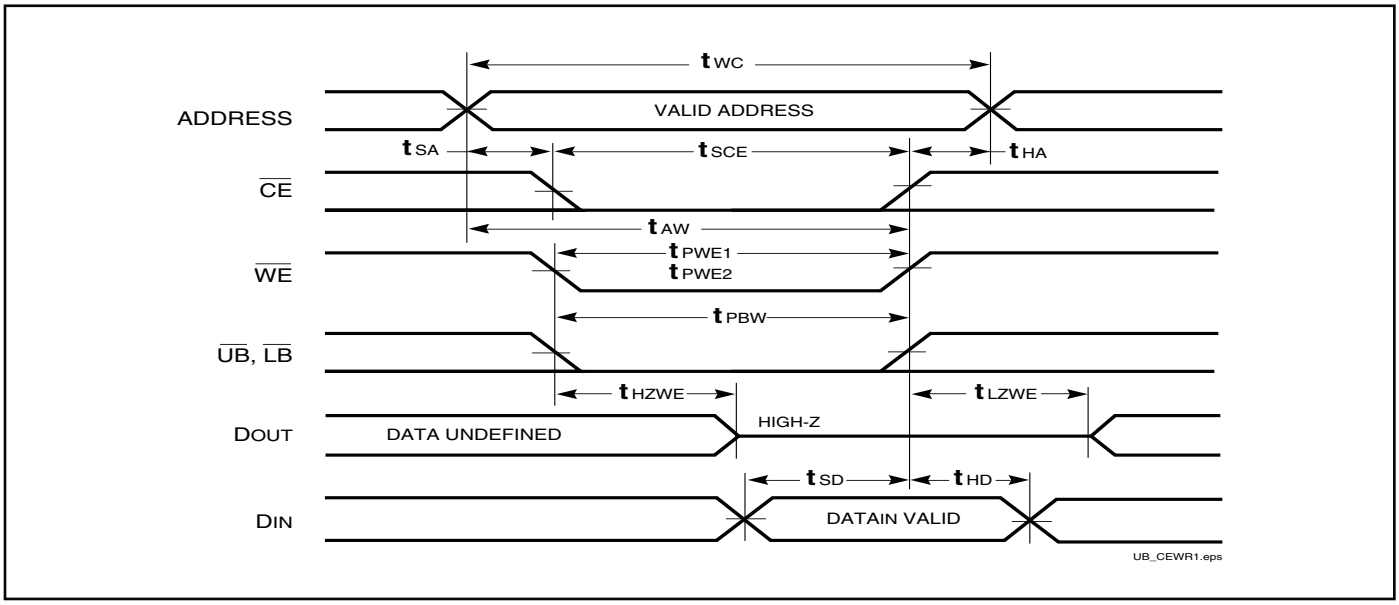
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.

2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

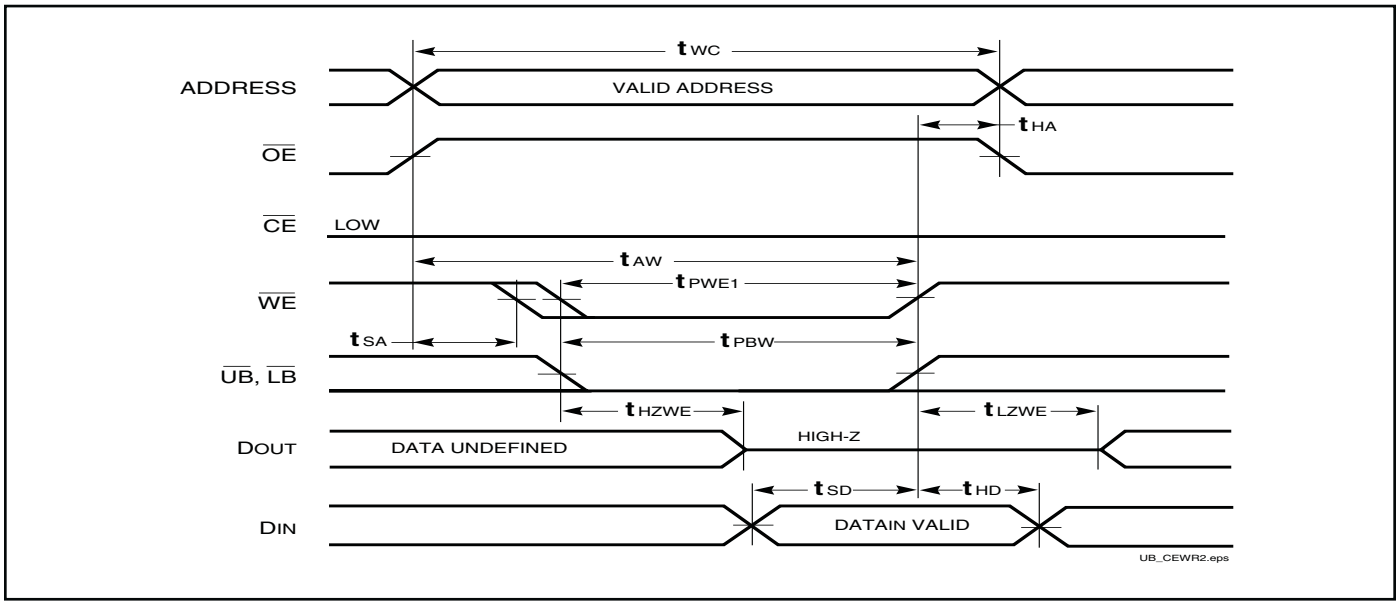
3. The internal write time is defined by the overlap of CE\ LOW and UB\ or LB\, and WE\ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE #1 (CE\ Controlled, OE\ is HIGH or LOW)[1]

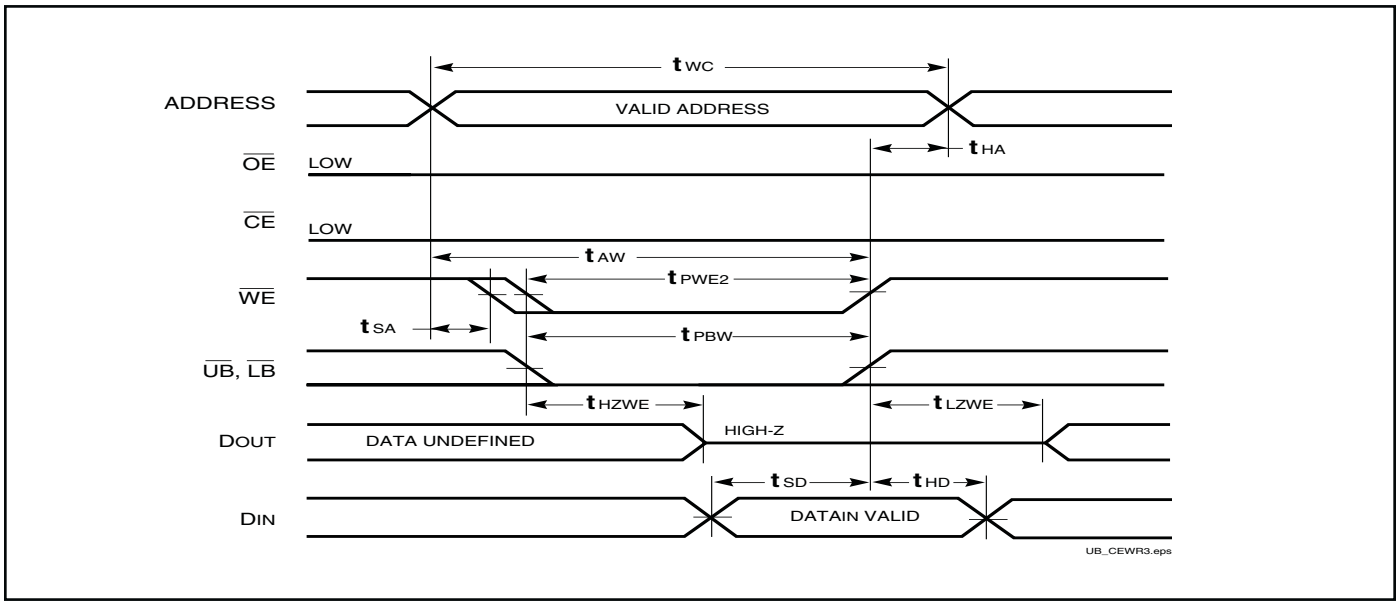


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

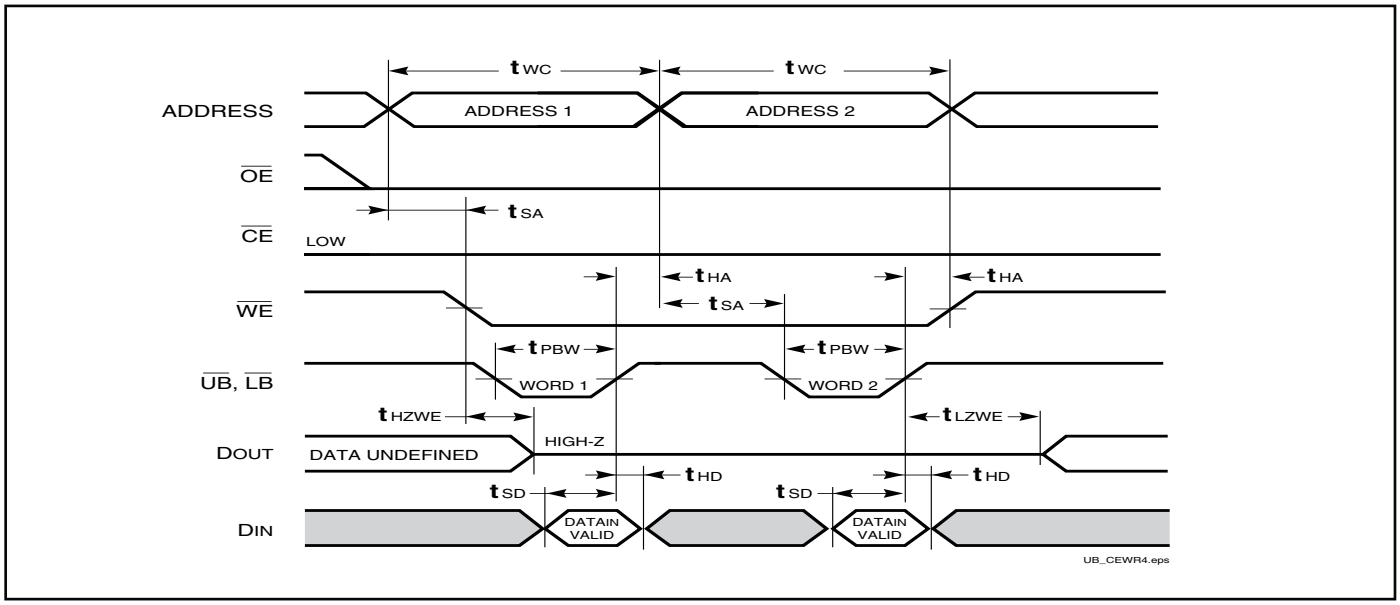
WRITE CYCLE #2 (WE\ Controlled, OE\ = HIGH during Write Cycle)[1,2]



WRITE CYCLE #3 (WE\ Controlled, OE\ is LOW During Write Cycles)[1]



WRITE CYCLE #4 (LB\, UB\ Controlled, Back to Back Write)[1,3]



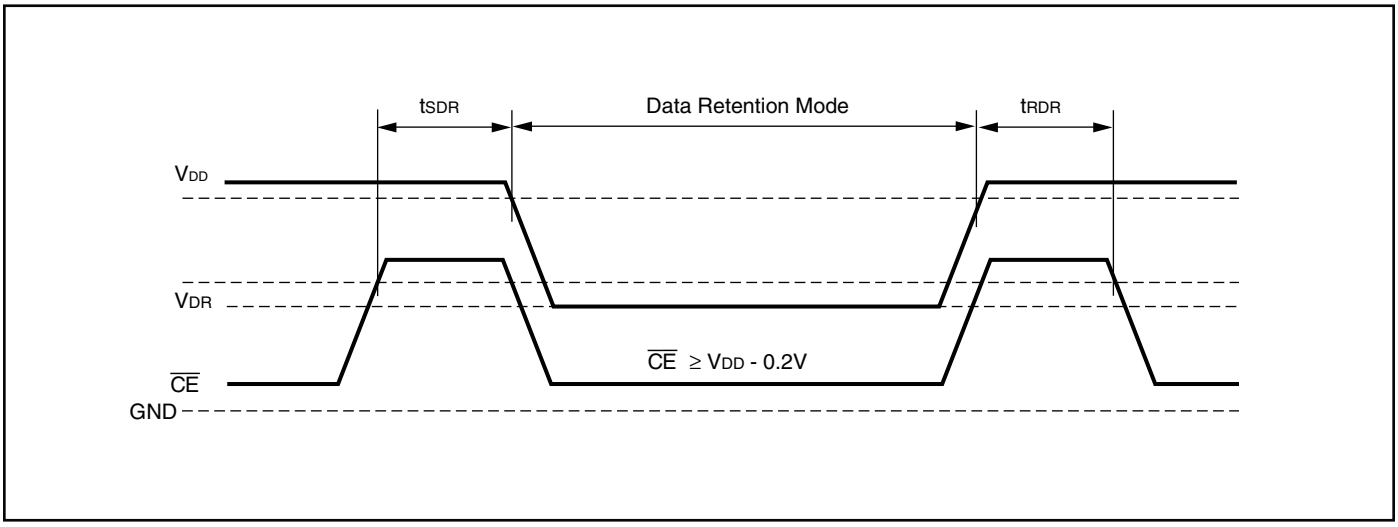
Notes:

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW, $\overline{UB}$ and/or $\overline{LB}$ = LOW, and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{LB}$, $\overline{UB}$ pins can be used to control the Write function.

DATA RETENTION SWITCHING CHARACTERISTICS (Low Power "L" Version)

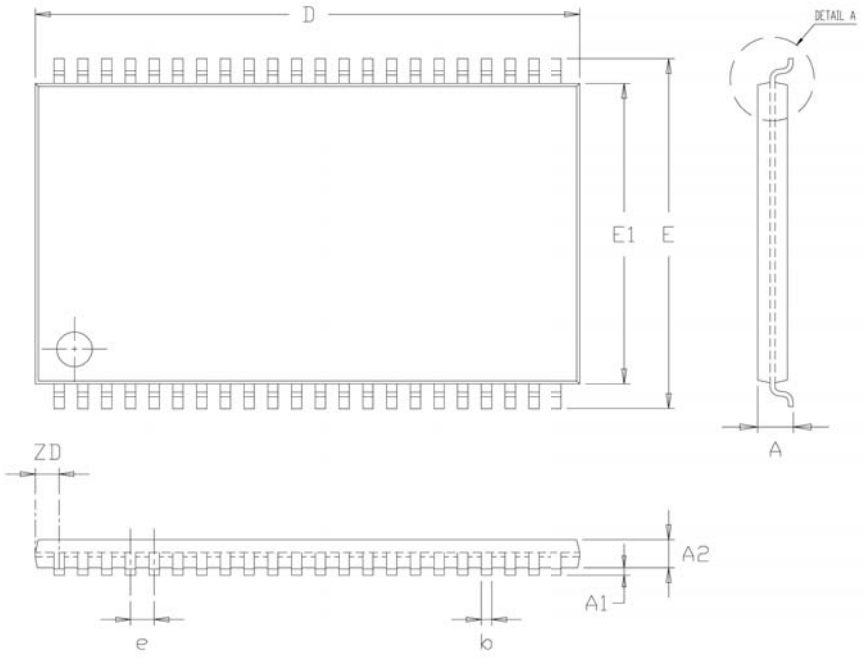
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0	-	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, CE\ ≥ V_{DD} – 0.2V	-	2	15	mA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	-	-	ns

DATA RETENTION WAVEFORM (CE\ Controlled)

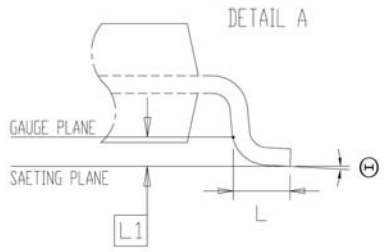


MECHANICAL DEFINITION

44-Pin TSOPII (Package Designator DGC & DGCR)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0	—	8°	0	—	8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ORDERING INFORMATION

44-pin TSOPII - Copper Lead Frame - Pb/Sn Lead Finish

Example: AS5SLC256K16DGC-10/IT

Device Number	Package Type	Speed (ns)	Option	Process
AS5LC256K16	DGC	-10	L	/*
AS5LC256K16	DGC	-15	L	/*
AS5LC256K16	DGC	-20	L	/*

44-pin TSOPII - Copper Lead Frame - NiPdAu Lead Finish (RoHS Compliant)

Example: AS5LC256K16DGCR-10/IT

Device Number	Package Type	Speed (ns)	Option	Process
AS5LC256K16	DGCR	-10	L	/*
AS5LC256K16	DGCR	-15	L	/*
AS5LC256K16	DGCR	-20	L	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range -40°C to +85°C
ET = Enhanced Temperature Range -40°C to +105°C
XT = Military Temperature Range -55°C to +125°C (Consult Factory)

**OPTION DEFINITIONS

L = 2V Data Retention / Low Power

DOCUMENT TITLE

256K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM

Rev #	History	Release Date	Status
0.0	Initial Release	May 2011	Preliminary
0.1	Added Thermal Resistance chart on page 2.	September 2011	Preliminary