36Mb Pipelined Sync SRAM

FEATURES

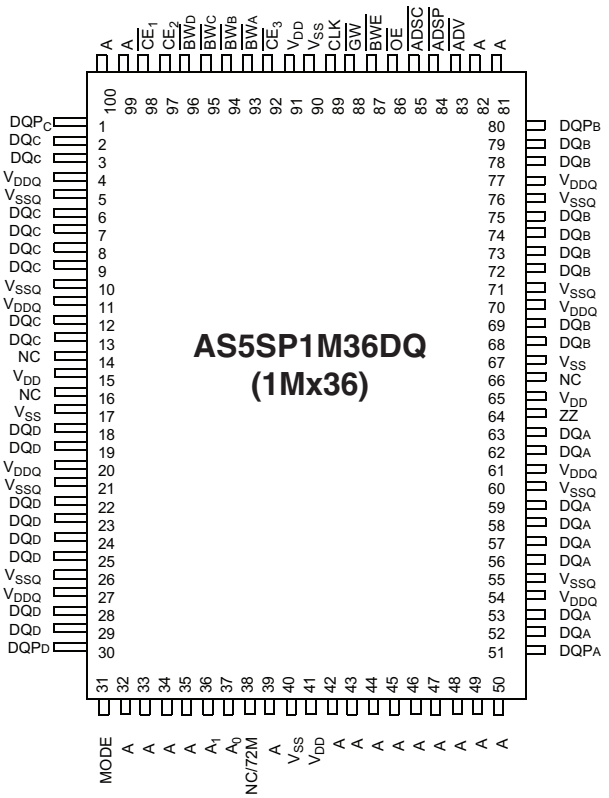
- Supports bus operation up to 200 MHz
- Available speed grades are 200 and 166 MHz
- Registered inputs and outputs for pipelined operation
- 3.3V core power supply
- 2.5V/3.3V I/O power supply
- Fast clock-to-output times
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel®
- Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Single Cycle Chip Deselect
- Available in lead-free 100-pin TQFP package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- "ZZ" Sleep Mode Option

OPTION MARKING

Temperature Range

Military Temp (-55°C to +125°C)	/XT
Industrial (-40°C to +85°C)	/IT
Enhanced (-40°C to +105°C)	/ET

FIGURE 1: PIN ASSIGNMENT
(Top View)



SELECTION GUIDE

	200MHz	166MH	Unit
Maximum Access Time	3.2	3.4	ns
Maximum Operating Current	425	375	mA
Maximum CMOS Standby Current	120	120	mA

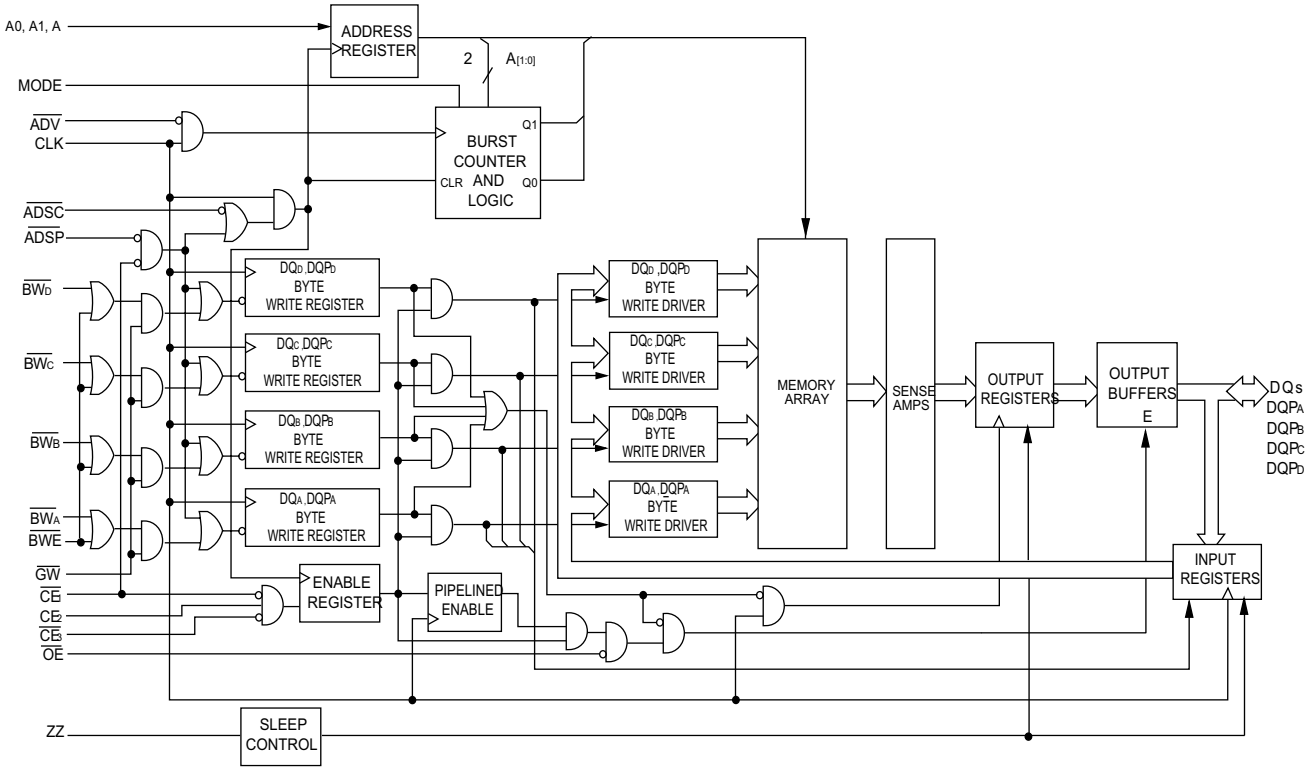
GENERAL DESCRIPTION

The AS5SP1M36DQ SRAM integrates 1M x 36/2M x 18 and 512K x 72 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable (CE_1), depth-expansion Chip Enables (CE_2 and CE_3), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables (BWx and BWE), and Global Write (GW). Asynchronous inputs include the Output Enable (OE) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle.This part supports Byte Write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. GW when active LOW causes all bytes to be written. The AS5SP1M36DQ operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

LOGIC BLOCK DIAGRAM



PIN DEFINITIONS

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[2] are sampled active. A1: A0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_C$, $\overline{BW}_E$, $\overline{BW}_G$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.

PIN DEFINITIONS (continued)

Name	I/O	Description
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. Not available for AJ package version. Not connected for BGA. Where referenced, $\overline{CE}_3$ is assumed active throughout this document for BGA. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQP_X	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die
NC/72M	–	**No Connects**. Not internally connected to thedie. NC/72M are address expansion pins & are not internally connected to the die.

FUNCTIONAL OVERVIEW

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.2ns (200-MHz device).

The AS5SP1M36DQ supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486∀! processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BWx) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects (CE_1, CE_2, CE_3) and an asynchronous Output Enable (OE) provide for easy bank selection and output tri-state control. ADSP is ignored if CE_1 is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) CE_1, CE_2, CE_3 are all asserted active, and (3) the Write signals (GW, BWE) are all deserted HIGH. ADSP is ignored if CE_1 is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.2ns (200-MHz device) if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tri-state immediately.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) CE_1, CE_2, CE_3 are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The Write signals (GW, BWE, and BWx) and ADV inputs are ignored during this first cycle.

ADSP-triggered Write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the Write operation is controlled by BWE and BWx signals.

The AS5SP1M36DQ provides Byte Write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write (BWx) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because AS5SP1M36DQ is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs inputs.Doing so will tri-state the output drivers. As a safety precaution, DQs are utomatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and BWx) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because AS5SP1M36DQ is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

FUNCTIONAL OVERVIEW (continued)

Burst Sequences

The AS5SP1M36DQ provides a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Asserting ADV LOW at clock rise will automatically
increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CE_1, CE_2, CE_3, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE=Floating or V_DD)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE=GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} - 0.2V			mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ VDD - 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery times	ZZ ≤ 0.2V	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is samples		$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is samples	0		ns

Truth Table [2,3,4,5,6,7]

Operation	Add. Used	CE1\	CE2	CE3\	ZZ	ADSP\	ADSC\	ADV\	WRITE\	OE\	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	TRI-STATE
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	TRI-STATE
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	TRI-STATE
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	TRI-STATE
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L-H	TRI-STATE
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	TRI-STATE
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	TRI-STATE
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	TRI-STATE
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	TRI-STATE
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	TRI-STATE
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	C	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	TRI-STATE
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	TRI-STATE
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes:
2. X=Don't Care, H=Logic HIGH, L=Logic LOW
3. WRITE\=L when any one or more Byte Write enable signals and BWE\=L or GW\=L. WRITE\=H when all Byte write enable signals, BWE\, GW\=H.
4. The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not samples with the clock.
5. CE1\, CE2, CE3\ are available only in the TQFP package. BGA package has only 2 chip selects CE1\ and CE2.
6. The SRAM always initiates a read cycle when ADSP\ is asserted, regardless of the state of GW\, BWE\, or BWX\. Writes may occur only on subsequent clocks after the ADSP\ or with the assertion of ADSC\. As a result, OE\ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. OE\ is a don't care for the remainder of the write cycles.
7. OE\ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when OE\ is inactive or when the device is deselected, and all data bits behave as output when OE\ is active (LOW).

Truth Table for Read/Write [4, 8, 9]

Function	GW\	BWE\	BW_D\	BW_C\	BW_B\	BW_A\
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A- (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B- (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C- (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D- (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D,B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

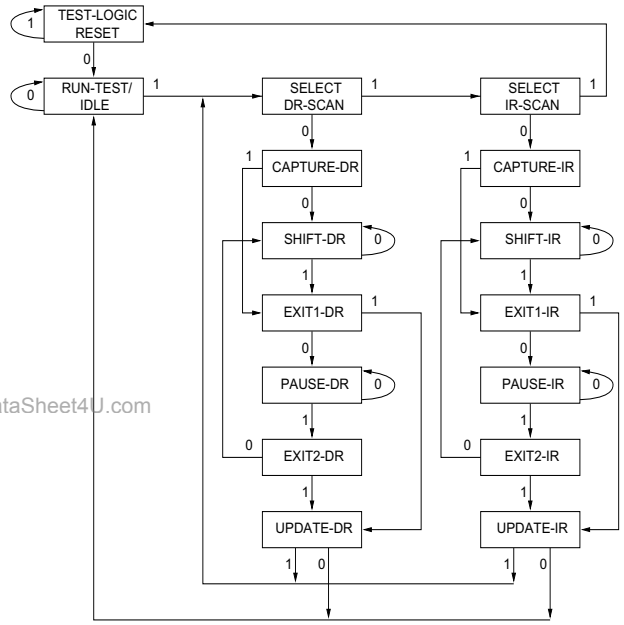
Notes:
8. BWX\ represents any byte write signal. To enable any byte write BWX\, a Logic LOW signal should be applied at clock rise. Any number of byte writes can be enabled at the same time for any given write.
9. Table only lists a partial listing of the byte write combinations. Any combination of BWX\ is valid. Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The AS5SP1M36DQ incorporates a serial boundary scan test access port (TAP). This part is fully compliant with IEEE Standard 1149.1. The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels. The AS5SP1M36DQ contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature
It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

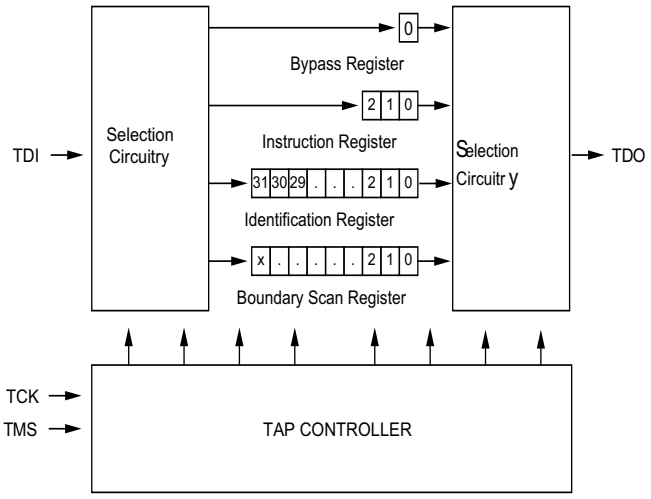
Test Clock (TCK)
The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)
The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)
The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

Test Data-Out (TDO)
The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

TAP Controller Block Diagram



Note: The JTAG feature is not tested. GBNT.

Performing a TAP Reset
A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers
Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register
Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register
To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register
The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register
The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set
Overview
Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

IDCODE
The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z
The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is given during the "Update IR" state.

SAMPLE/PRELOAD
SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be

possible. To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins. PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST
The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction alsoselects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

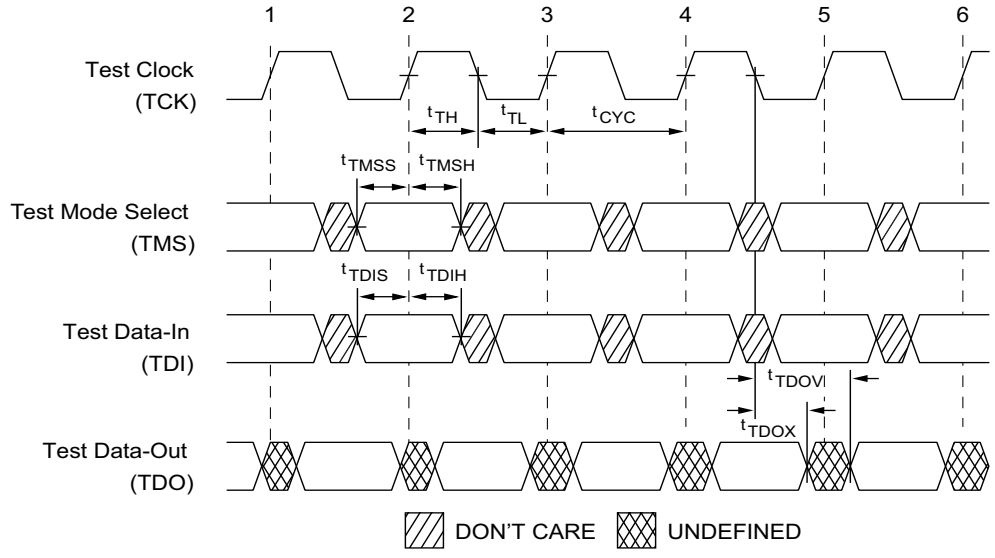
EXTEST OUTPUT BUS TRI-STATE
IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at, bit #89 (for 165-FBGA package) or bit #138 (for 209-FBGA package). When this scan cell, called the "extest output bus tri-state", is latched into the preload register during the "Update-DR" state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR", the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

Reserved
These instructions are not implemented but are reserved for future use. Do not use these instructions.

Tap Timing



TAP AC Switching Characteristics Over the operating range [10,11]

Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH Time	20		ns
t_{TL}	TCK Clock LOW Time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	5		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	5		ns
t_{CS}	Capture Set-upo to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

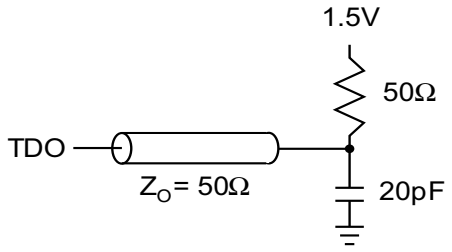
3.3V TAP AC Test Conditions

Input pulse levels.....Vss to 3.3V
Input rise and fall times.....1ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Test load termination supply voltage 1.5V

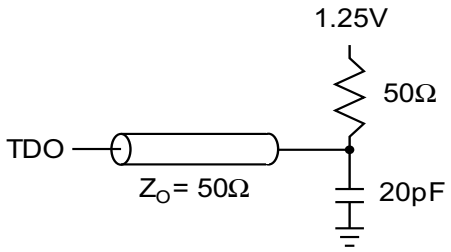
2.5 TAP AC Test Conditions

Input pulse levels.....Vss to 2.5V
Input rise and fall times.....1ns
Input timing reference levels.....1.25V
Output reference levels.....1.25V
Test load termination supply voltage 1.25V

3.3V TAP AC Output Load Equivalent



2.5 TAP AC Output Load Equivalent



Notes:
10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

TAO DC Electrical Characteristics and Operating Conditons

0°C<TA<+70°C; V_{DD}=3.135 to 3.6V unless otherwise noted) [12]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH}=-4.0mA, V_{DDQ}=3.3V		2.4		V
		I_{OH}=-1.0mA, V_{DDQ}=2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH}=-100µA	V_{DDQ}=3.3V	2.9		V
			V_{DDQ}=2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL}=8.0mA	V_{DDQ}=3.3V		0.4	V
		I_{OL}=1.0mA	V_{DDQ}=2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OH}=100µA	V_{DDQ}=3.3V		0.2	V
			V_{DDQ}=2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ}=3.3V	2.0	V_{DD}+0.3	V
			V_{DDQ}=2.5V	1.7	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ}=3.3V	-0.3	0.8	V
			V_{DDQ}=2.5V	-0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		-5	5	µA

Identification Register Definitions

Instruction Field	1M x 36	Description
Revision Number (31:29)	000	Describes the version number
Device Depth (28:24) [13]	01011	Reserved for Internal Use
Architecture / Memory Type (23:18)	000000	Defines memory type and architecture
Bus Width / Density (17:12)	100111	Defines width and density
JEDEC ID Code (11:1) +	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (x36)
Instruction	3
Bypass	1
ID	32

Notes:
12. All voltages referenced to V_{SS} (GND).
13. Bit #24 is '1' in the ID Register Definitions for both 2.5V and 3.3V versions of this device.

+ Austin Semiconductor uses Cypress die so this code reflects Cypress.

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the I/O ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do not use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do not use: This instruction is reserved for future use.
RESERVED	110	Do not use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C
Ambient Temperature with
Power Applied.....–55°C to +125°C
Supply Voltage on V_{DD} Relative to GND..... –0.3V to +4.6V
Supply Voltage on V_{DDQ} Relative to GND ..... –0.3V to +V_{DD}
DC Voltage Applied to Outputs
in Tri-State..... –0.5V to V_{DDQ} + 0.5V
DC Input Voltage ..... –0.5V to V_{DD} + 0.5V
Current into Outputs (LOW)..... 20 mA
Static Discharge Voltage..... > 2001V
(per MIL-STD-883, Method 3015)
Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V -5%/+10%	2.5V-5% to V_{DD}
Industrial	-40°C to +85°C		
Enhanced	-40°C to +105°C		
Military	-55°C to +125°C		

Electrical Characteristics Over the Operating Range [17, 18]

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3V I/O		3.135	V_{DD}	V
		for 2.5V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3V I/O, I_{OH}=-4.0mA		2.4		V
		for 2.5V I/O, I_{OH}=-1.0ma		2.0		V
V_{OL}	Output LOW Voltage	for 3.3V I/O, I_{OH}=8.0mA			0.4	V
		for 2.5V I/O, I_{OH}=1.0ma			0.4	V
V_{IH}	Input HIGH Voltage [17]	for 3.3V I/O		2.0	V_{DD}+0.3V	V
		for 2.5V I/O		1.7	V_{DD}+0.3V	V
V_{IL}	Input LOW Voltage [17]	for 3.3V I/O		-0.3	0.8	V
		for 2.5V I/O		-0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_1 ≤ V_{DDQ}		-5	5	µA
	Input Current of MODE	Input = V_{SS}		-30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		-5		µA
		Input = V_{DD}			30	µA
Ioz	Output Leak Current	GND ≤ V_1 ≤ V_{DDQ}, Output Disabled		-5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	5-ns cycle, 200 MHz		425	mA
			6-ns cycle, 167 MHz		375	mA
I_{SB1}	Automatic CE Power Down Current TTL Inputs	V_{DD} = Max, Device Deselected V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	All Speeds		225	mA
I_{SB2}	Automatic CE Power Down Current CMOS Inputs	V_{DD} = Max, Device Deselected V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} - 0.3V, f = 0	All Speeds		120	mA
I_{SB3}	Automatic CE Power Down Current CMOS Inputs	V_{DD} = Max, Device Deselected V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} - 0.3V, f = f_{MAX} = $1/t_{CYC}$	All Speeds		200	mA
I_{SB4}	Automatic CE Power Down Current TTL Inputs	V_{DD} = Max, Device Deselected V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All Speeds		135	mA

Notes:

17. Overshoot: V_{IH} (AC) < V_{DD} +1.5V (Pulse width less than $T_{CYC}/2$), undershoot: V_{IL} (AC) > -2V (Pulse width less than $t_{CYC}/2$)

18. $T_{power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD} (min) within 200ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

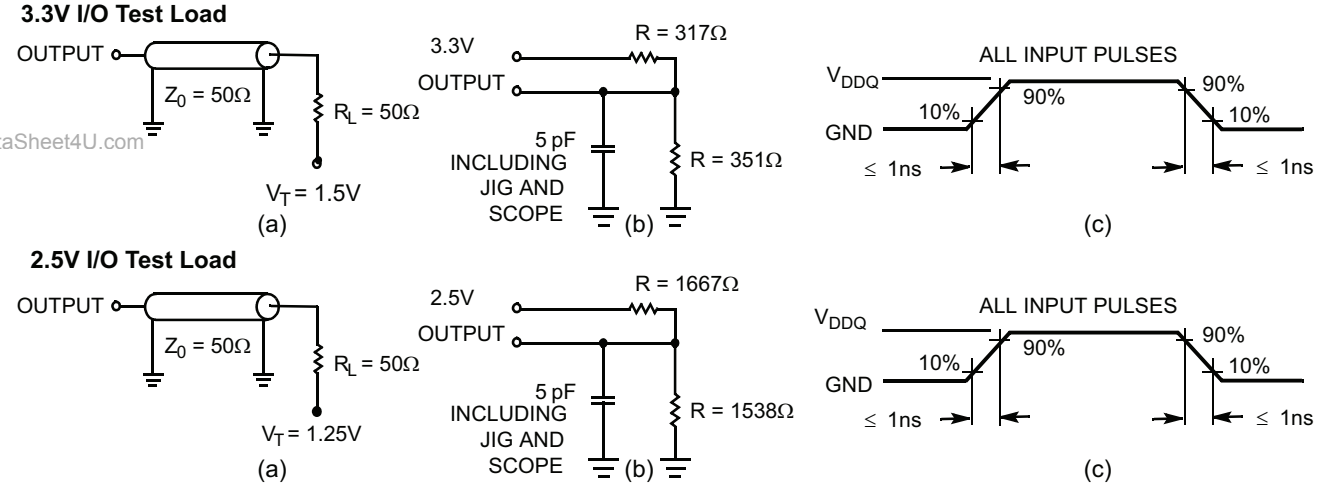
Capacitance [19]

Parameter	Description	Test Conditions	100 TQFP Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f=1MHz,	6.5	pF
C_{CLK}	Clock Input Capacitance	V_{DD} = 3.3V	3	pF
$C_{I/O}$	Input/Output Capacitance	V_{DDQ} = 2.5V	5.5	pF

Thermal Resistance [19]

Parameter	Description	Test Conditions	100 TQFP Package	Unit
ΘJA	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	25.21	°C/W
Θ JC	Thermal Resistance (Junction to Case)		2.28	°C/W

AC Test Loads and Waveforms



Note:
19. Tested initially and after any design or process change that may affect these parameters.

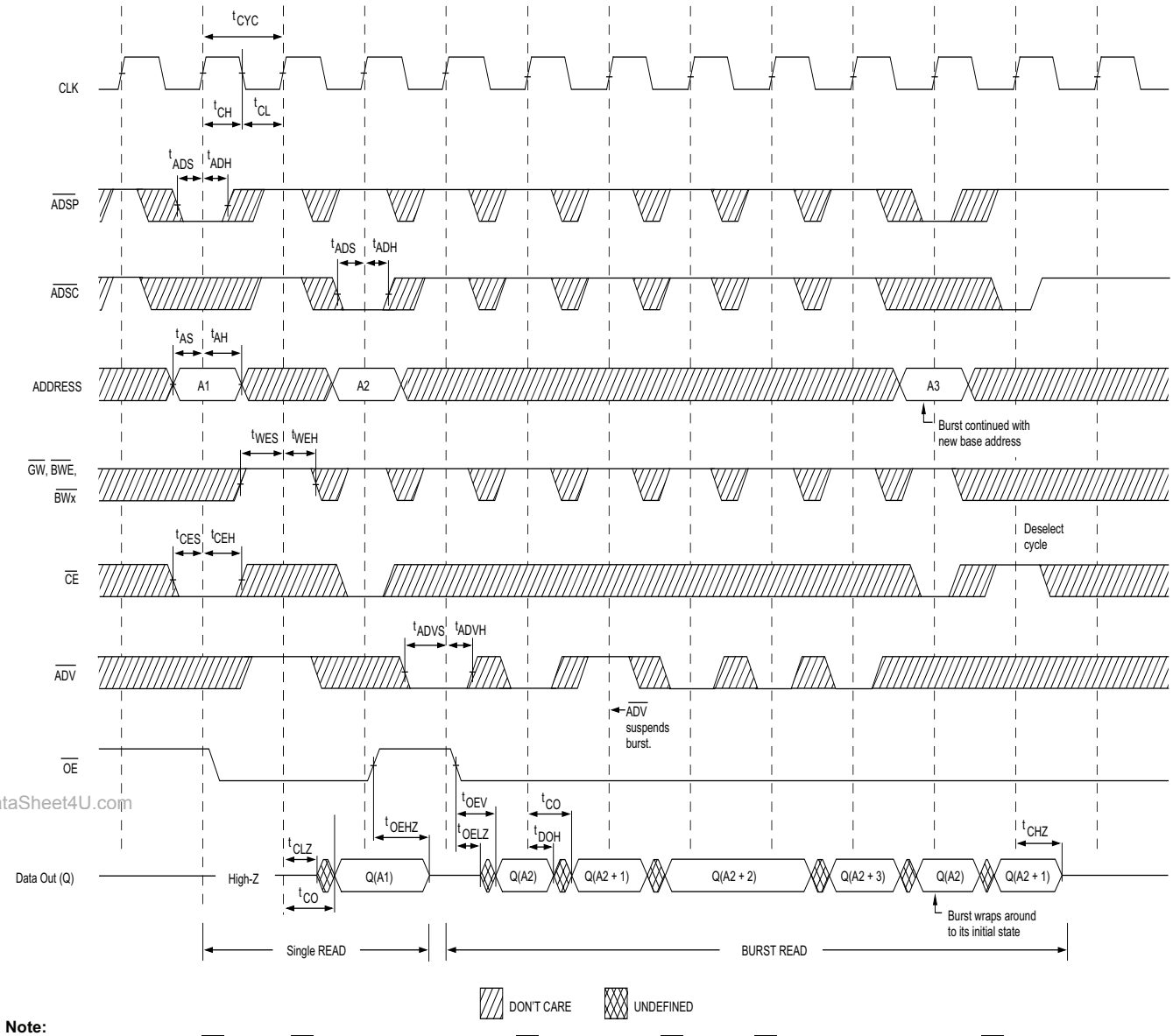
Switching Characteristics Over the Operating Range [24, 25]

Parameter	Description [20]	-200		-166		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD} (Typical) to the first access [20]	1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	5		6		ns
t_{CH}	Clock HIGH	2.0		2.4		ns
t_{CL}	Clock LOW	2.0		2.4		ns
Output Times						
t_{CO}	Data Output Valid After CLK Rise		3.2		3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5		1.5		ns
t_{CLZ}	Clock to Low-Z [21, 22, 23]	1.3		1.5		ns
t_{CHZ}	Clock to High-Z [21, 22, 23]		3.0		3.4	ns
t_{OEV}	OE\ LOW to Output Valid		3.0		3.4	ns
t_{OELZ}	OE\ LOW to Output Low-Z [21, 22, 23]	0		0		ns
t_{OEHZ}	OE\ HIGHto Output Low-Z [21, 22, 23]		3.0		3.4	ns
Set-Up Times						
t_{AS}	Address Set-up Before CLK Rise	1.4		1.5		ns
t_{ADS}	ADSC\, ADSP\ Set-up Before CLK Rise	1.4		1.5		ns
t_{ADVS}	ADV\ Set-up Before CLK Rise	1.4		1.5		ns
t_{WES}	GW\, BWE\ BWx\ Set-up Before CLK Rise	1.4		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.4		1.5		ns
t_{CES}	Chip Enable Set-up Before CLK Rise	1.4		1.5		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.4		0.5		ns
t_{ADH}	ADSP\, ADSC\ Hold After CLK Rise	0.4		0.5		ns
t_{ADVH}	ADV\ Hold After CLK Rise	0.4		0.5		ns
t_{WEH}	GW\, BWE\ BWx\ Set-up After CLK Rise	0.4		0.5		ns
t_{DH}	Data Input Set-up After CLK Rise	0.4		0.5		ns
t_{CEH}	Chip Enable Set-up After CLK Rise	0.4		0.5		ns

Notes:
20. This part has a voltage regulator internally; tPOWER is the time that the power needs to be supplied above VDD(minimum) initially before a read or write operation can be initiated.
21. tCHZ, tCLZ,tOELZ, and tOEHZ are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
22. At any given voltage and temperature, tOEHZ is less than tOELZ and tCHZ is less than tCLZ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
23. This parameter is sampled and not 100% tested.
24. Timing reference level is 1.5V when VDDQ = 3.3V and is 1.25V when VDDQ = 2.5V.
25. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Waveforms

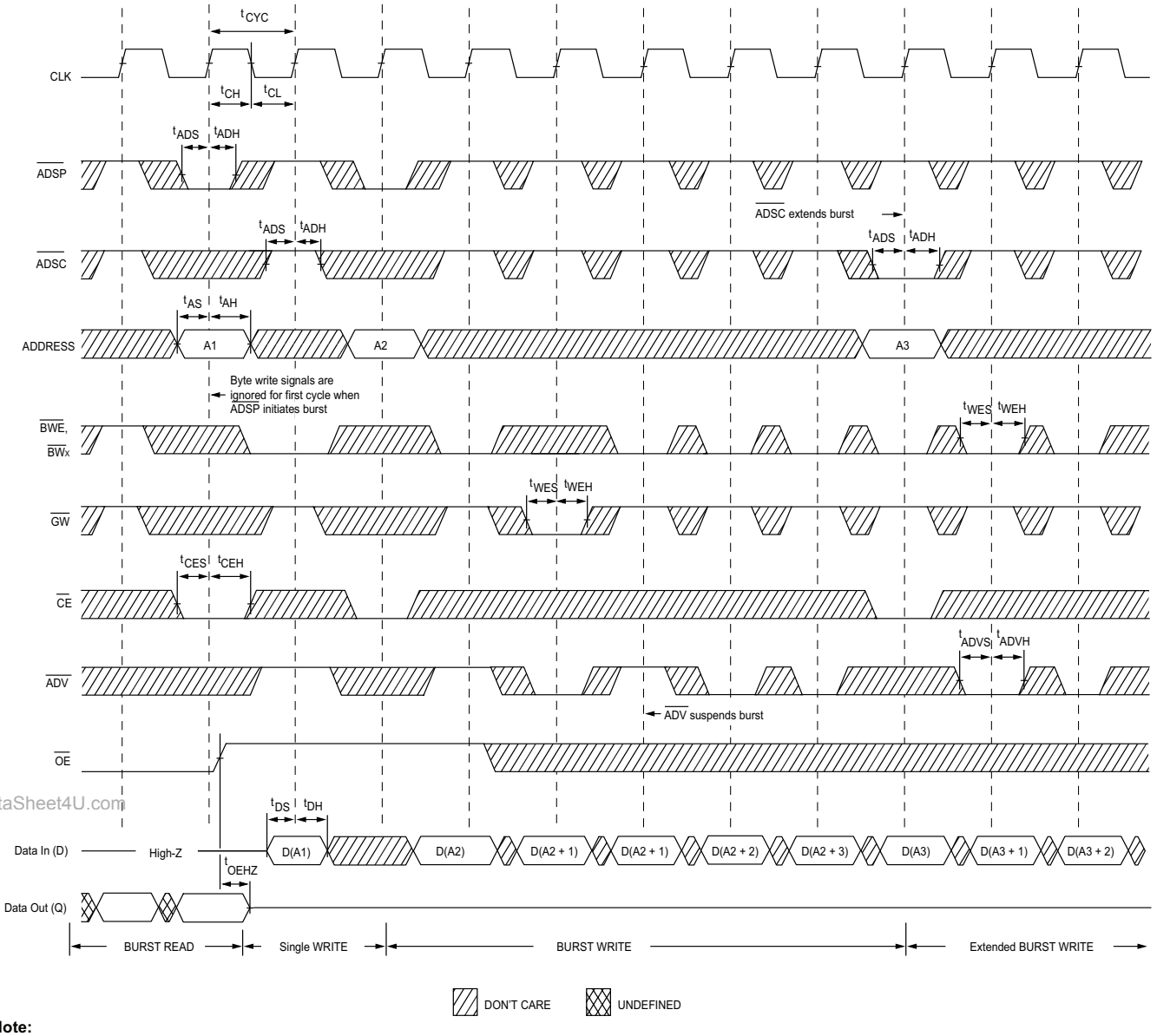
Read Cycle Timing[26]



Note:
26. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

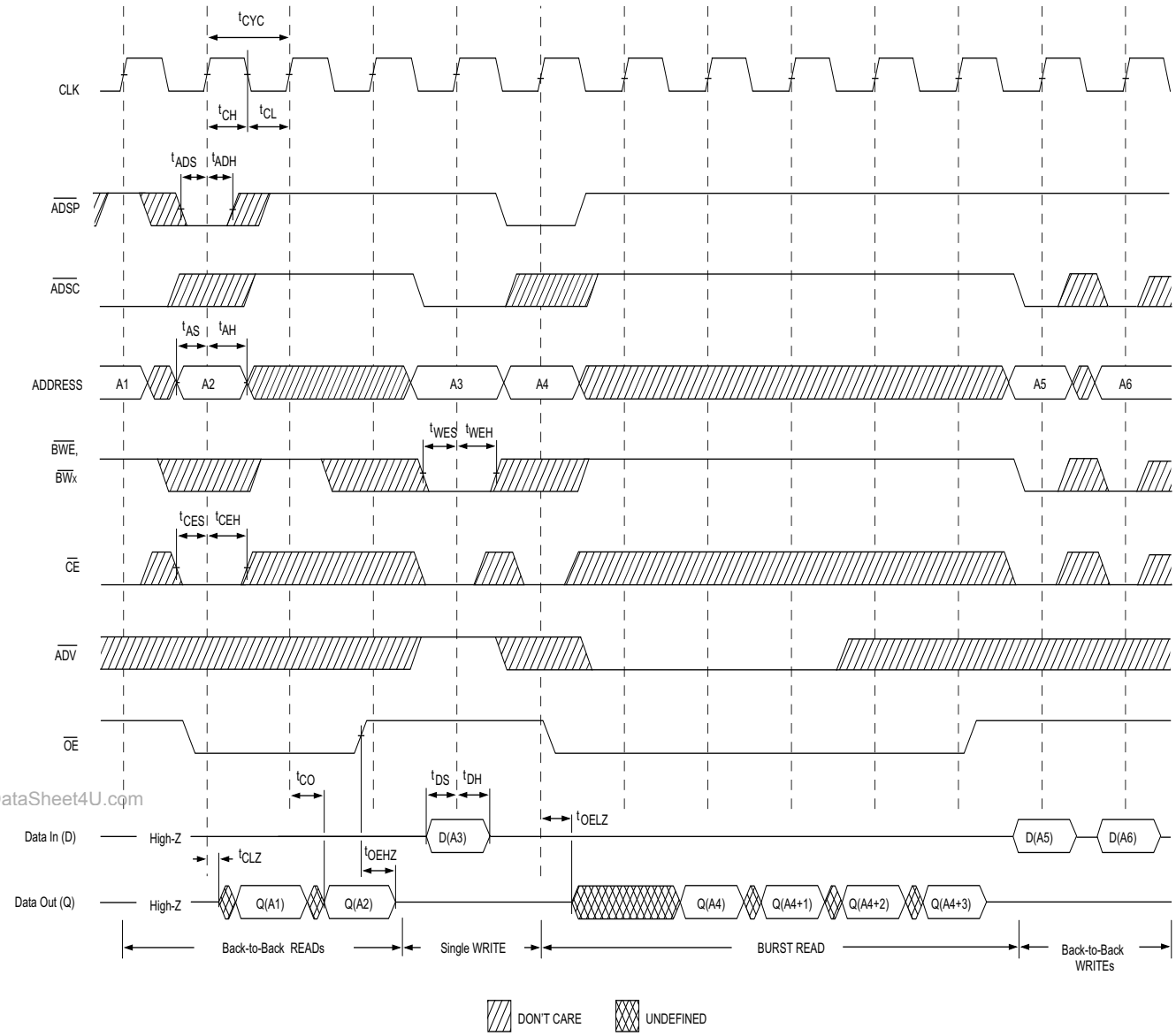
Write Cycle Timing[26, 27]



Note:
27. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Switching Waveforms (continued)

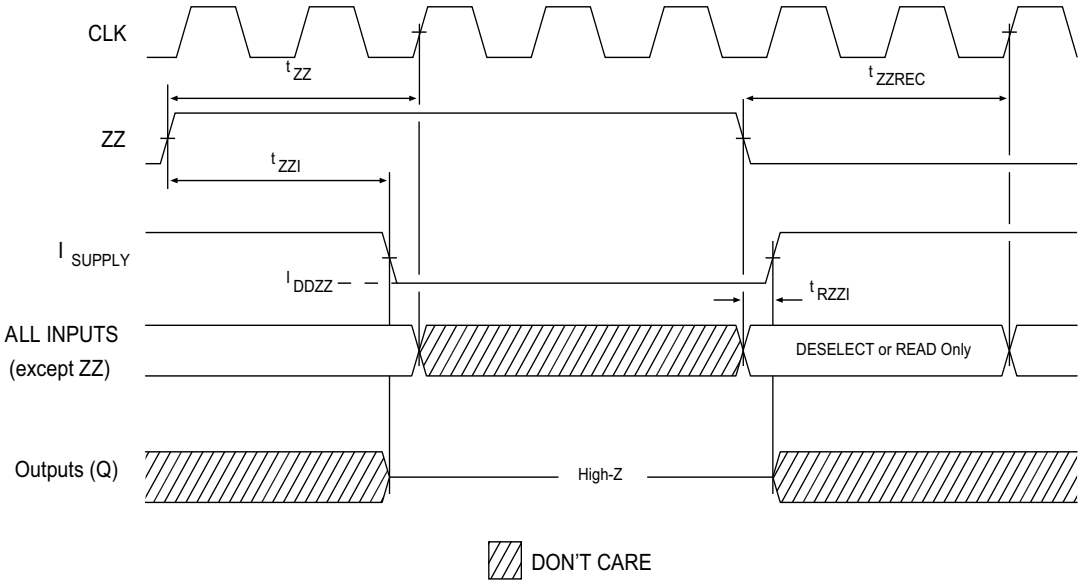
Read/Write Cycle Timing[26, 28, 29]



Notes:
28. The data bus (Q) remains in high-Z following a Write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
29. $\overline{GW}$ is HIGH.

Switching Waveforms (continued)

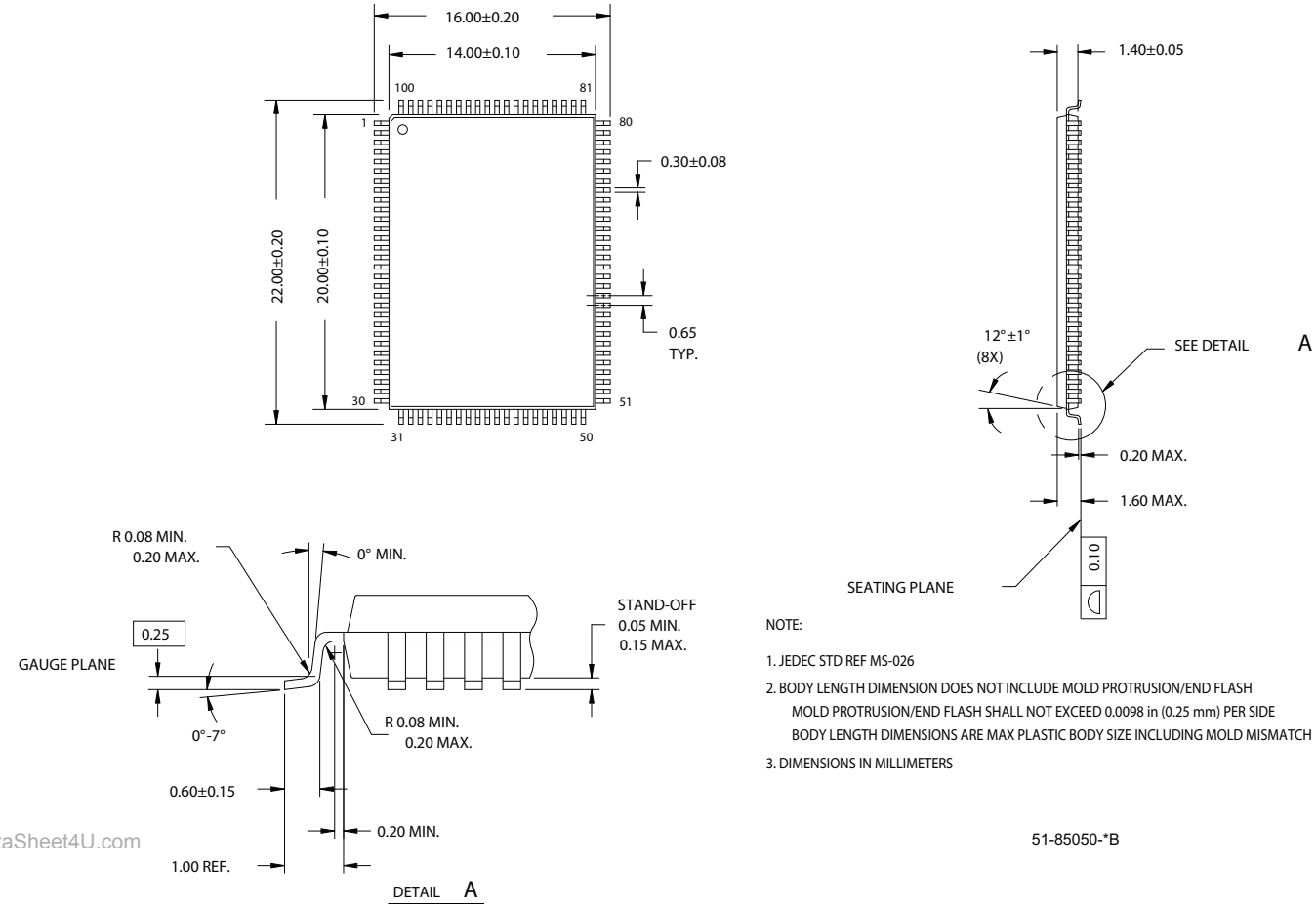
ZZ Mode Timing[30, 31]



Notes:
30. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
31. DQs are in high-Z when exiting ZZ sleep mode.

Package Diagrams

100-pin TQFP (14 x 20 x 1.4 mm) (51-85050)



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

ORDERING INFORMATION

Part Number	Configuration	Speed (MHz)	Pkg.
Industrial (-40°C to +85°C)			
AS5SP1M36DQ-167/IT	1M x 36 Pipelined Synch SRAM	167	100 Pin TQFP
AS5SP1M36DQ-200/IT	1M x 36 Pipelined Synch SRAM	200	100 Pin TQFP
Enhanced (-40°C to +105°C)			
AS5SP1M36DQ-167/ET	1M x 36 Pipelined Synch SRAM	167	100 Pin TQFP
AS5SP1M36DQ-200/ET	1M x 36 Pipelined Synch SRAM	200	100 Pin TQFP
Military Temp (-55°C to +125°C)			
AS5SP1M36DQ-167/XT	1M x 36 Pipelined Synch SRAM	167	100 Pin TQFP
AS5SP1M36DQ-200/XT	1M x 36 Pipelined Synch SRAM	200	100 Pin TQFP

PB OPTION (WHERE AVAILABLE)

Part Number	Configuration	Speed (MHz)	Pkg.
Industrial (-40°C to +85°C)			
AS5SP1M36DQR-167/IT	1M x 36 Pipelined Synch SRAM	167	100 Pin TQFP
AS5SP1M36DQR-200/IT	1M x 36 Pipelined Synch SRAM	200	100 Pin TQFP
Enhanced (-40°C to +105°C)			
AS5SP1M36DQR-167/ET	1M x 36 Pipelined Synch SRAM	167	100 Pin TQFP
AS5SP1M36DQR-200/ET	1M x 36 Pipelined Synch SRAM	200	100 Pin TQFP
Military Temp (-55°C to +125°C)			
AS5SP1M36DQR-167/XT	1M x 36 Pipelined Synch SRAM	167	100 Pin TQFP
AS5SP1M36DQR-200/XT	1M x 36 Pipelined Synch SRAM	200	100 Pin TQFP

Temperature Range
Military Temp (-55°C to +125°C)
Industrial (-40°C to +85°C)
Enhanced (-40°C to +105°C)

DOCUMENT TITLE

36Mb Pipelined Sync SRAM

REVISION HISTORY

Rev #	History	Release Date	Status
1.0	Datasheet Creation+	January 2009	Release
1.1	updated order chart	March 2009	Release
1.2	updated speeds (pg1, 15)	April 2009	Release

+ From baseline Cypress datasheet doc# 38-05383 Rev E