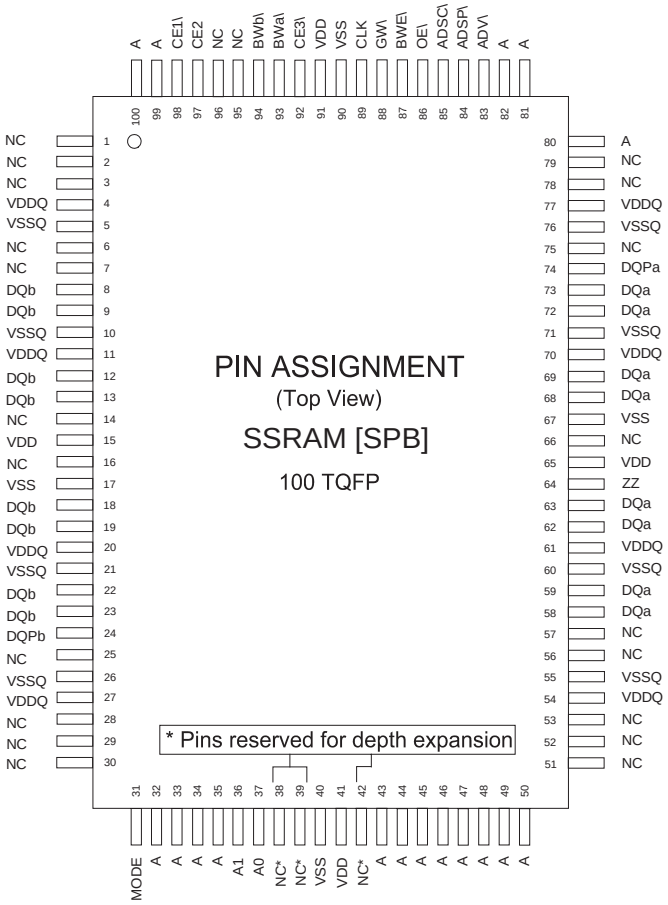
micross components
transforming specialty electronics

SSRAM
AS5SP512K18

Plastic Encapsulated Microcircuit
9Mb, 512K x 18, Synchronous SRAM
Pipeline Burst, Single Cycle Deselect

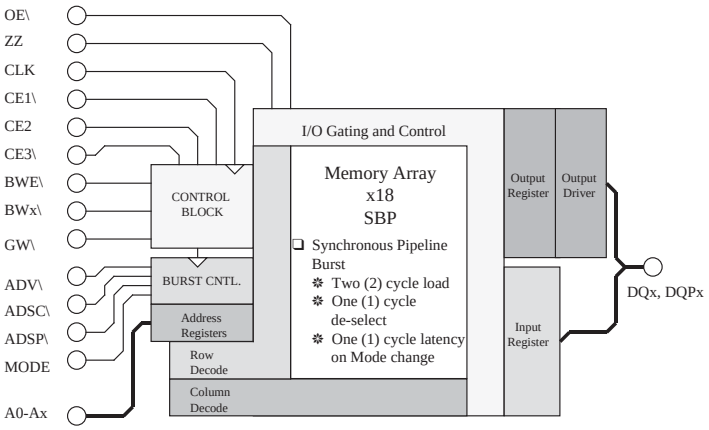
FEATURES
- Synchronous Operation in relation to the input Clock
- 2 Stage Registers resulting in Pipeline operation
- On chip address counter for Burst operations
- Self-Timed Write Cycles
- On-Chip Address and Control Registers
- Byte Write support
- Global Write support
- On-Chip low power mode [powerdown] via ZZ pin
- Interleaved or Linear Burst support via Mode pin
- Three Chip Enables for ease of depth expansion without Data Contention.
- Two Cycle load, Single Cycle Deselect
- Asynchronous Output Enable (OE\)
- Three Pin Burst Control (ADSP\, ADSC\, ADV\)
- 3.3V Core Power Supply
- 3.3V/2.5V IO Power Supply
- JEDEC Standard 100 pin TQFP Package
- Available in **Industrial** (-40°C to +85°C), **Enhanced** (-40°C to +105°C), and **Mil-Temperature** (-55°C to +125°C) Operating Ranges
- RoHS compliant options



FAST ACCESS TIMES

Parameter	Symbol	200Mhz	166Mhz	133Mhz	Units
Cycle Time	tCYC	5.0	6.0	7.5	ns
Clock Access Time	tCD	3.0	3.5	4.0	ns
Output Enable Access	tOE	3.0	3.5	4.0	ns

BLOCK DIAGRAM



GENERAL DESCRIPTION

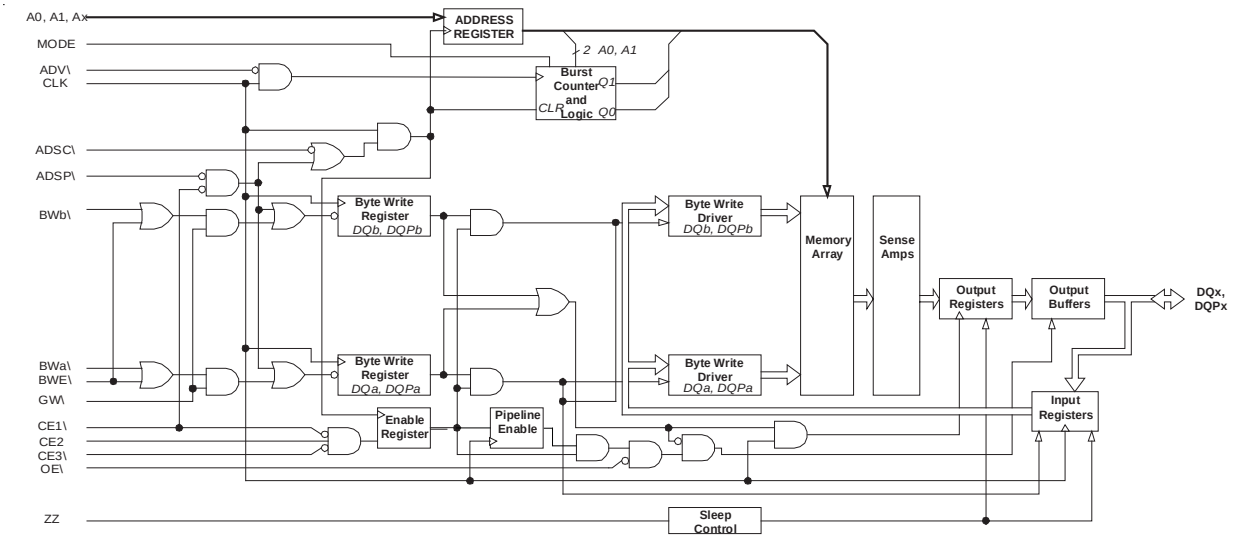
Micross Components AS5SP512K18 is a 9.0Mb High Performance Synchronous Pipeline Burst SRAM, available in multiple temperature screening levels, fabricated using High Performance CMOS technology and is organized as a 512K x 18. It integrates address and control registers, a two (2) bit burst address counter supporting four (4) double-word transfers. Writes are internally self-timed and synchronous to the rising edge of clock.

The AS5SP512K18 includes advanced control options including Global Write, Byte Write as well as an Asynchronous Output enable. Burst Cycle controls are handled by three (3) input pins, ADV\, ADSP\ and ADSC\. Burst operation can be initiated with either the Address Status Processor (ADSP\) or Address Status Cache controller (ADSC\) inputs. Subsequent burst addresses are generated internally in the system's burst sequence control block and are controlled by Address Advance (ADV\) control input.

PIN DESCRIPTION/ASSIGNMENT TABLE

Signal Name	Symbol	Type	Pin	Description
Clock	**CLK**	Input	**89**	This input registers the address, data, enables, Global and Byte writes as well as the burst control functions
Address	**A0, A1**	Input	**37, 36**	Low order, Synchronous Address Inputs and Burst counter address inputs
Address	**A**	Input(s)	**35, 34, 33, 32, 31, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43,83**	Synchronous Address Inputs
Chip Enable	**CE1\, CE3**	Input	**98, 92**	Active Low True Chip Enables
Chip Enable	**CE2**	Input	**97**	Active High True Chip Enable
Global Write Enable	**GW**	Input	**88**	Active Low True Global Write enable. Write to all bits
Byte Enables	**BWa\, BWb**	Input	**93, 94**	Active Low True Byte Write enables. Write to byte segments
Byte Write Enable	**BWE**	Input	**87**	Active Low True Byte Write Function enable
Output Enable	**OE**	Input	**86**	Active Low True Asynchronous Output enable
Address Strobe Controller	**ADSC**	Input	**85**	Address Strobe from Controller. When asserted LOW, Address is captured in the address registers and A0-A1 are loaded into the Burst When ADSP\ and ADSC are both asserted, only ADSP is recognized
Address Strobe from Processor	**ADSP**	Input	**84**	Synchronous Address Strobe from Processor. When asserted LOW, Address is captured in the Address registers, A0-A1 is registered in the burst counter. When both ADSP\ and ADSC\ or both asserted, only ADSP\ is recognized. ADSP\ is ignored when CE1\ is HIGH
Address Advance	**ADV**	Input	**83**	Advance input Address. When asserted HIGH, address in burst counter is incremented.
Power-Down	**ZZ**	Input	**64**	Asynchronous, non-time critical Power-down Input control. Places the chip into an ultra low power mode, with data preserved.
Data Parity Input/Outputs	**DQPa, DQPb**	Input/ Output	**74,24**	Bidirectional I/O Parity lines. As inputs they reach the memory array via an input register, the address stored in the register on the rising edge of clock. As outputs, the line delivers the valid data stored in the array via an output register and output driver. The data delieverd is from the previous clock period of the READ cycle.
Data Input/Outputs	**DQa, DQb**	Input/ Output	**58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23**	Bidirectional I/O Data lines. As inputs they reach the memory array via an input register, the address stored in the register on the rising edge of clock. As outputs, the line delivers the valid data stored in the array via an output register and output driver. The data delieverd is from the previous clock period of the READ cycle.
Burst Mode	**MODE**	Input	**31**	Interleaved or Linear Burst mode control
Power Supply [Core]	**VDD**	Supply	**91, 15, 41, 65**	Core Power Supply
Ground [Core]	**VSS**	Supply	**90, 17, 40, 67**	Core Power Supply Ground
Power Supply I/O	**VDDQ**	Supply	**4, 11, 20, 27, 54, 61, 70, 77**	Isolated Input/Output Buffer Supply
I/O Ground	**VSSQ**	Supply	**5, 10, 21, 26, 55, 60, 71, 76**	Isolated Input/Output Buffer Ground
No Connection(s)	**NC**	NA	**1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96**	No connections to internal silicon

LOGIC BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Micross Components's AS5SP512K18 Synchronous SRAM is manufactured to support today's High Performance platforms utilizing the Industries leading Processor elements including those of Intel and Motorola. The AS5SP512K18 supports Synchronous SRAM READ and WRITE operations as well as Synchronous Burst READ/WRITE operations. All inputs with the exception of OE\, MODE and ZZ are synchronous in nature and sampled and registered on the rising edge of the devices input clock (CLK). The type, start and the duration of Burst Mode operations is controlled by MODE, ADSC\, ADSP\ and ADV\ as well as the Chip Enable pins CE1\, CE2, and CE3\. All synchronous accesses including the Burst accesses are enabled via the use of the multiple enable pins and wait state insertion is supported and controlled via the use of the Advance control (ADV\).

The AS5SP512K18 supports both Interleaved as well as Linear Burst modes therefore making it an architectural fit for either the Intel or Motorola CISC processor elements available on the Market today.

The AS5SP512K18 supports Byte WRITE operations and enters this functional mode with the Byte Write Enable (BWE\) and the Byte Write Select pin(s) (BWa\ and BWb\). Global Writes are supported via the Global Write Enable (GW\) and Global Write Enable will override the Byte Write inputs and will perform a Write to all Data I/Os.

The AS5SP512K18 provides ease of producing very dense arrays via the multiple Chip Enable input pins and Tri-state outputs.

Single Cycle Access Operations

A Single READ operation is initiated when all of the following conditions are satisfied at the time of Clock (CLK) HIGH: [1] ADSP\ pr ADSC\ is asserted LOW, [2] Chip Enables are all asserted active, and [3] the WRITE signals (GW\, BWE\) are in their FALSE state (HIGH). ADSP\ is ignored if CE1\ is HIGH. The address presented to the Address inputs is stored within the Address Registers and Address Counter/Advancement Logic and then passed or presented to the array core. The corresponding data of the addressed location is propagated to the Output Registers and passed to the data bus on the next rising clock via the Output Buffers. The time at which the data is presented to the Data bus is as specified by either the Clock to Data valid specification or the Output Enable to Data Valid spec for the device speed grade chosen.

The only exception occurs when the device is recovering from a deselected to select state where its outputs are tristated in the first machine cycle and controlled by its Output Enable (OE\) on following cycle. Consecutive single cycle READS are supported. Once the READ operation has been completed and deselected by use of the Chip Enable(s) and either ADSP\ or ADSC\, its outputs will tri-state immediately.

A Single ADSP\ controlled WRITE operation is initiated when both of the following conditions are satisfied at the time of Clock (CLK) HIGH: [1] ADSP\ is asserted LOW, and [2] Chip Enable(s) are asserted ACTIVE. The address presented to the address bus is registered and loaded on CLK HIGH, then presented to the core array. The WRITE controls Global Write, and Byte Write Enable (GW\, BWE\) as well as the individual Byte Writes (BWa\ and BWb\) and ADV\ are ignored on the first machine cycle. ADSP\ triggered WRITE accesses require two (2) machine cycles to complete. If Global Write is asserted LOW on the second Clock (CLK) rise, the data presented to the array via the Data bus will be written into the array at the corresponding address location specified by the Address bus. If GW\ is HIGH (inactive) then BWE\ and one or more of the Byte Write controls (BWa\ and BWb\) controls the write operation. All WRITES that are initiated in this device are internally self timed.

A Single ADSC\ controlled WRITE operation is initiated when the following conditions are satisfied: [1] ADSC\ is asserted LOW, [2] ADSP\ is de-asserted (HIGH), [3] Chip Enable(s) are asserted (TRUE or Active), and [4] the appropriate combination of the WRITE inputs (GW\, BWE\, BWx\) are asserted (ACTIVE). Thus completing the WRITE to the desired Byte(s) or the complete data-path. ADSC\ triggered WRITE accesses require a single clock (CLK) machine cycle to complete. The address presented to the input Address bus pins at time of clock HIGH will be the location that the WRITE occurs. The ADV\ pin is ignored during this cycle, and the data WRITTEN to the array will either be a BYTE WRITE or a GLOBAL WRITE depending on the use of the WRITE control functions GW\ and BWE\ as well as the individual BYTE CONTOLS (BWx\).

DEEP POWER-DOWN MODE (SLEEP)

The AS5SP512K18 has a Deep Power-Down mode and is controlled by the ZZ pin. The ZZ pin is an Asynchronous input and asserting this pin places the SSRAM in a deep power-down mode (SLEEP). While in this mode, Data integrity is guaranteed. For the device to be placed successfully into this operational mode the device must be deselected and the Chip Enables, ADSP\ and ADSC\ remain inactive for the duration of tZZREC after the ZZ input returns LOW. Use of this deep power-down mode conserves power and is very useful in multiple memory page designs where the mode recovery time can be hidden. Accesses pending when entering sleep mode are not considered valid and completion of the operation is not guaranteed.

SYNCHRONOUS TRUTH TABLES

CE1\	CE2	CE3\	ADSP\	ADSC\	ADV\	WT / RD	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	NA	Not Selected
L	L	X	L	X	X	X	↑	NA	Not Selected
L	X	H	L	X	X	X	↑	NA	Not Selected
L	L	X	H	L	X	X	↑	NA	Not Selected
L	X	H	H	L	X	X	↑	NA	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst, READ
L	H	L	H	L	X	WT	↑	External Address	Begin Burst, WRITE
L	H	L	H	L	X	RD	↑	External Address	Begin Burst, READ
X	X	X	H	H	L	RD	↑	Next Address	Continue Burst, READ
H	X	X	X	H	L	RD	↑	Next Address	Continue Burst, READ
X	X	X	H	H	L	WT	↑	Next Address	Continue Burst, WRITE
H	X	X	X	H	L	WT	↑	Next Address	Continue Burst, WRITE
X	X	X	H	H	H	RD	↑	Current Address	Suspend Burst, READ
H	X	X	X	H	H	RD	↑	Current Address	Suspend Burst, READ
X	X	X	H	H	H	WT	↑	Current Address	Suspend Burst, WRITE
H	X	X	X	H	H	WT	↑	Current Address	Suspend Burst, WRITE

Notes:
1. X = Don't Care
2. WT= WRITE operation in WRITE TABLE, RD= READ operation in WRITE TABLE

BURST SEQUENCE TABLES

Interleaved Burst									
Burst Control Pin [MODE]	State	Case 1		Case 2		Case 3		Case 4	
	HIGH	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

Linear Burst									
Burst Control Pin [MODE]	State	Case 1		Case 2		Case 3		Case 4	
	LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

CAPACITANCE

Parameter	Symbol	Max.	Units
Input Capacitance	**CI**	6	pF
Input/Output Capacitance	**CIO**	8	pF
Clock Input Capacitance	**CCLK**	6	pF

WRITE TABLE

GW\	BW\	BWa\	BWb\	Operation
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE Byte [A]
H	L	H	L	WRITE Byte [B]
H	L	L	L	WRITE ALL Bytes
L	X	X	X	WRITE ALL Bytes

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	OE\	I/O Status
Power-Down (SLEEP)	H	X	High-Z
READ	L	L	DQ
	L	H	High-Z
WRITE	L	X	Din, High-Z
De-Selected	L	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min.	Max.	Units
Voltage on VDD Pin	**VDD**	-0.3	4.6	V
Voltage on VDDQ Pins	**VDDQ**	VDD		V
Voltage on Input Pins	**VIN**	-0.3	VDD+0.3	V
Voltage on I/O Pins	**VIO**	-0.3	VDDQ+0.3	V
Power Dissipation	**PD**		1.6	W
Storage Temperature	**tSTG**	-65	150	°C
Operating Temperatures [Screening Levels]	**/IT**	-40	85	°C
	/ET	-40	105	°C
	/XT	-55	125	°C

**Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for any duration or segment of time may affect device reliability.*

AC TEST LOADS

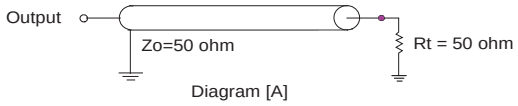


Diagram [A]

Vt= Termination Voltage
Rt= Termination Resistor

Vt= 1.50v for 3.3v VDDQ
Vt= 1.25v for 2.5v VDDQ

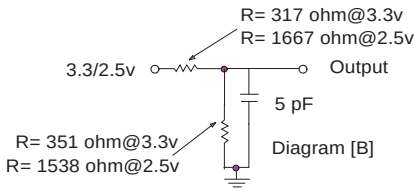


Diagram [B]

DC ELECTRICAL CHARACTERISTICS

(VDD=3.3v +10%/-5%, TA= Min. and Max temperatures of Screening level chosen)

Symbol	Parameter	Test Conditions		Min	Max	Units	Notes
VDD	Power Supply Voltage			3.135	3.63	V	1
VDDQ	I/O Supply Voltage			2.375	VDD	V	1,5
VoH	Output High Voltage	VDD=Min., IOH=-4mA	3.3v	2.4		V	1,4
		VDD=Min., IOH=-1mA	2.5v	2		V	1,4
VoL	Output Low Voltage	VDD=Min., IOL=8mA	3.3v		0.4	V	1,4
		VDD=Min., IOL=1mA	2.5v		0.4	V	1,4
VIH	Input High Voltage		3.3v	2	VDD+0.3	V	1,2
			2.5v	1.7	VDD+0.3	V	1,2
VIL	Input Low Voltage		3.3v	-0.3	0.8	V	1,2
			2.5v	-0.3	0.7	V	1,2
IIL	Input Leakage (except ZZ) & Mode	VDD=Max., VIN=VSS to VDD		-5	5	uA	3
IZZL	Input Leakage, ZZ pin & Mode			-30	30	uA	3
IOL	Output Leakage	Output Disabled, VOUT=VSSQ to VDDQ		-5	5	uA	
IDD	Operating Current	VDD=Max., f=Max., IOH=0mA	5.0ns Cycle, 200 Mhz		290	mA	
			6.0ns Cycle, 166 Mhz		270	mA	
			7.5ns Cycle, 133 Mhz		240	mA	
ISB1	Automatic CE. Power-down Current -TTL inputs	Max. VDD, Device De-Selected, VIN>/=VIH or VIN</=VIL f=fMAX=1/tCYC					
			5.0ns Cycle, 200 Mhz		200	mA	
			6.0ns Cycle, 166 Mhz		180	mA	
			7.5ns Cycle, 133 Mhz		160	mA	
ISB2	Automatic CE. Power-down Current - CMOS Inputs	Max. VDD, Device De-Selected, VIN</=0.3v or VIN>/=VDDQ-0.3v f=0			130	mA	

THERMAL RESISTANCE

Parameter	Description	Test Conditions	DQ Package	DQC Package	Unit
Θ JA	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	29.41	30.2	°C/W
Θ JC	Thermal Resistance (Junction to Case)		6.13	6.5	°C/W

Notes:

[1] All Voltages referenced to VSS (Logic Ground)

[2] Overshoot: VIH < +4.6V for t<tKC/2 for I<20mA
Undershoot: VIL >-0.7V for t<tKC/2 for I<20mA
Power-up: VIH <+3.6V and VDD<3.135V for t<200ms

[3] MODE and ZZ pins have internal pull-up resistors, and input leakage +/> +10uA

[4] The load used for VOH, VOL testing is shown in Figure-2 for 3.3v and 2.5V supplies.
AC load current is higher than stated values, AC I/O curves can be made available upon request

[5] VDDQ should never exceed VDD, VDD and VDDQ can be connected together

[6] This parameter is measured for initial design only

AC SWITCHING CHARACTERISTICS

(VDD=3.3v -5%/+10%, TA= Min. and Max temperatures of Screening level chosen)

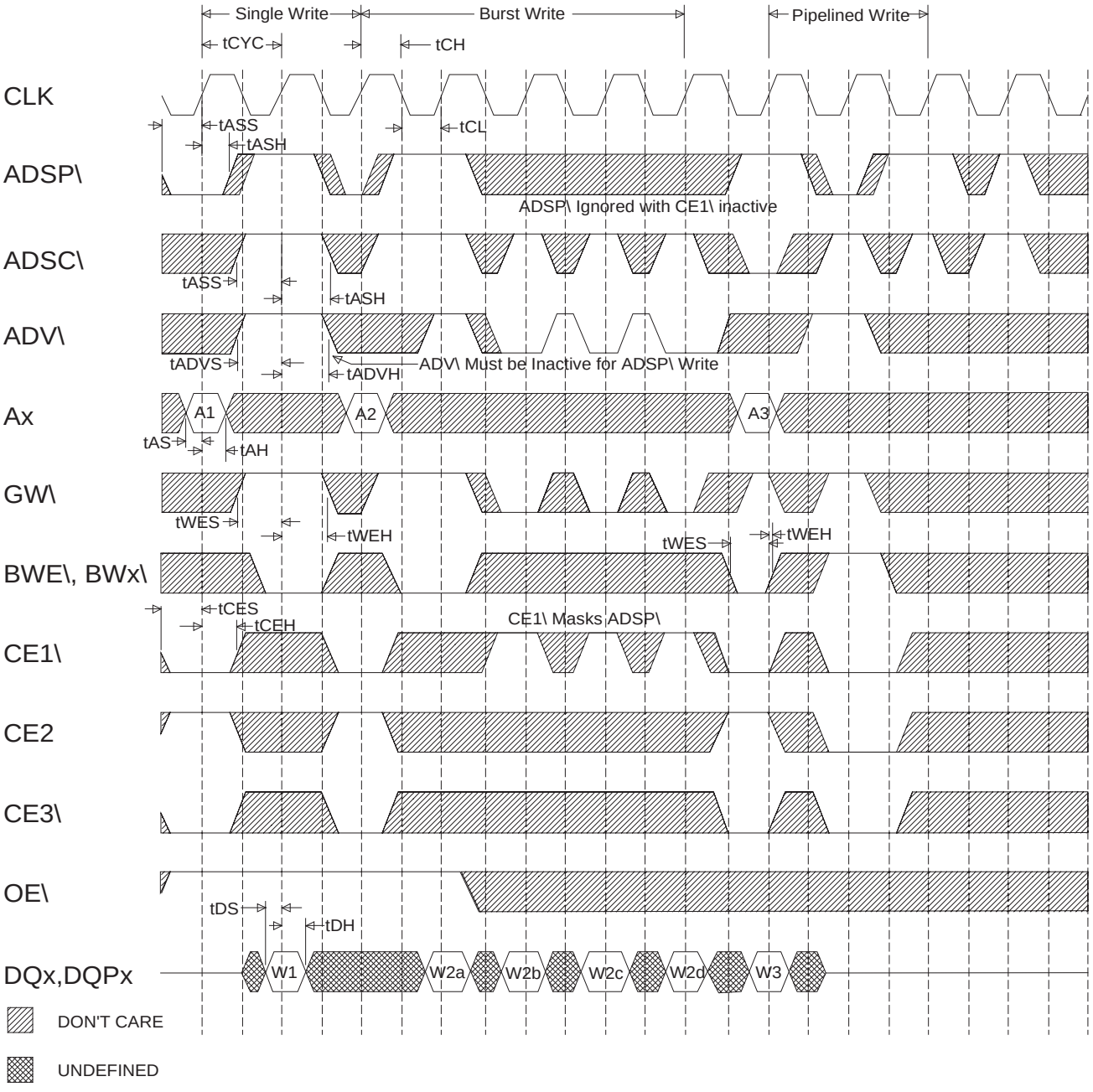
Parameter	Symbol	-30 [200Mhz]		-35 [166Mhz]		-40 [133Mhz]		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Clock (CLK) Cycle Time	**tCYC**	5.00	-	6.00	-	7.50	-	ns	
Clock (CLK) High Time	**tCH**	2.00	-	2.40	-	2.50	-	ns	1
Clock (CLK) Low Time	**tCL**	2.00	-	2.40	-	2.50	-	ns	1
Clock Access Time	**tCD**		3.00		3.50		4.00	ns	2
Clock (CLK) High to Output Low-Z	**tCLZ**	1.25	-	1.25	-	1.25	-	ns	2,3,4,5
Clock High to Output High-Z	**tCHZ**	1.25	3.00	1.25	3.50	1.25	3.50	ns	2,3,4,5
Output Enable to Data Valid	**tOE**	-	3.00	-	3.50	-	4.00	ns	6
Output Hold from Clock High	**tOH**	1.25	-	1.25	-	1.25	-	ns	
Output Enable Low to Output Low-Z	**tOELZ**	0.00	-	0.00	-	0.00	-	ns	2,3,4,5
Output Enable High to Output High-Z	**tOEHZ**	-	3.00	-	3.50	-	3.50	ns	2,3,4,5
Address Set-up to CLK High	**tAS**	1.50		1.50		1.50		ns	7,8
Address Hold from CLK High	**tAH**	0.50		0.50		0.50		ns	7,8
Address Status Set-up to CLK High	**tASS**	1.50		1.50		1.50		ns	7,8
Address Status Hold from CLK High	**tASH**	0.50		0.50		0.50		ns	7,8
Address Advance Set-up to CLK High	**tADVS**	1.50		1.50		1.50		ns	7,8
Address Advance Hold from CLK High	**tADVH**	0.50		0.50		0.50		ns	7,8
Chip Enable Set-up to CLK High (CEx\, CE2)	**tCES**	1.50		1.50		1.50		ns	7,8
Chip Enable Hold from CLK High (CEx\, CE2)	**tCEH**	0.50		0.50		0.50		ns	7,8
Data Set-up to CLK High	**tDS**	1.50		1.50		1.50		ns	7,8
Data Hold from CLK High	**tDH**	0.50		0.50		0.50		ns	7,8
Write Set-up to CLK High (GW\, BWE\, BWx\)	**tWES**	1.50		1.50		1.50		ns	7,8
Write Hold from CLK High (GW\, BWE\, BWX\)	**tWEH**	0.50		0.50		0.50		ns	7,8
ZZ High to Power Down	**tPD**		2		2		2	cycles	
ZZ Low to Power Up	**tPU**	2		2		2		cycles	

Notes to Switching Specifications:

1. Measured as HIGH when above VIH and Low when below VIL
2. This parameter is measured with the output loading shown in AC Test Loads
3. This parameter is sampled
4. Transition is measured +500mV from steady state voltage
5. Critical specification(s) when Design Considerations are being reviewed/analyized for Bus Contentention
6. OE\ is a Don't Care when a Byte or Global Write is sampled LOW
7. A READ cycle is defined by Byte or Global Writes sampled LOW and ADSP\ is sampled HIGH for the required SET-UP and HOLD times
8. This is a Synchronous device. All addresses must meet the specified SET-UP and HOLD times for all rising edges of CLK when either ADSP\ or ADSC\ is sampled LOW while the device is enabled. All other synchronous inputs must meet the SET-UP and HOLD times with stable logic levels for all rising edges of clock (CLK) during device operation (enabled). Chip Enable (Cex\, CE2) must be valid at each rising edge of clock (CLK) when either ADSP\ or ADSC\ is LOW to remain enabled.

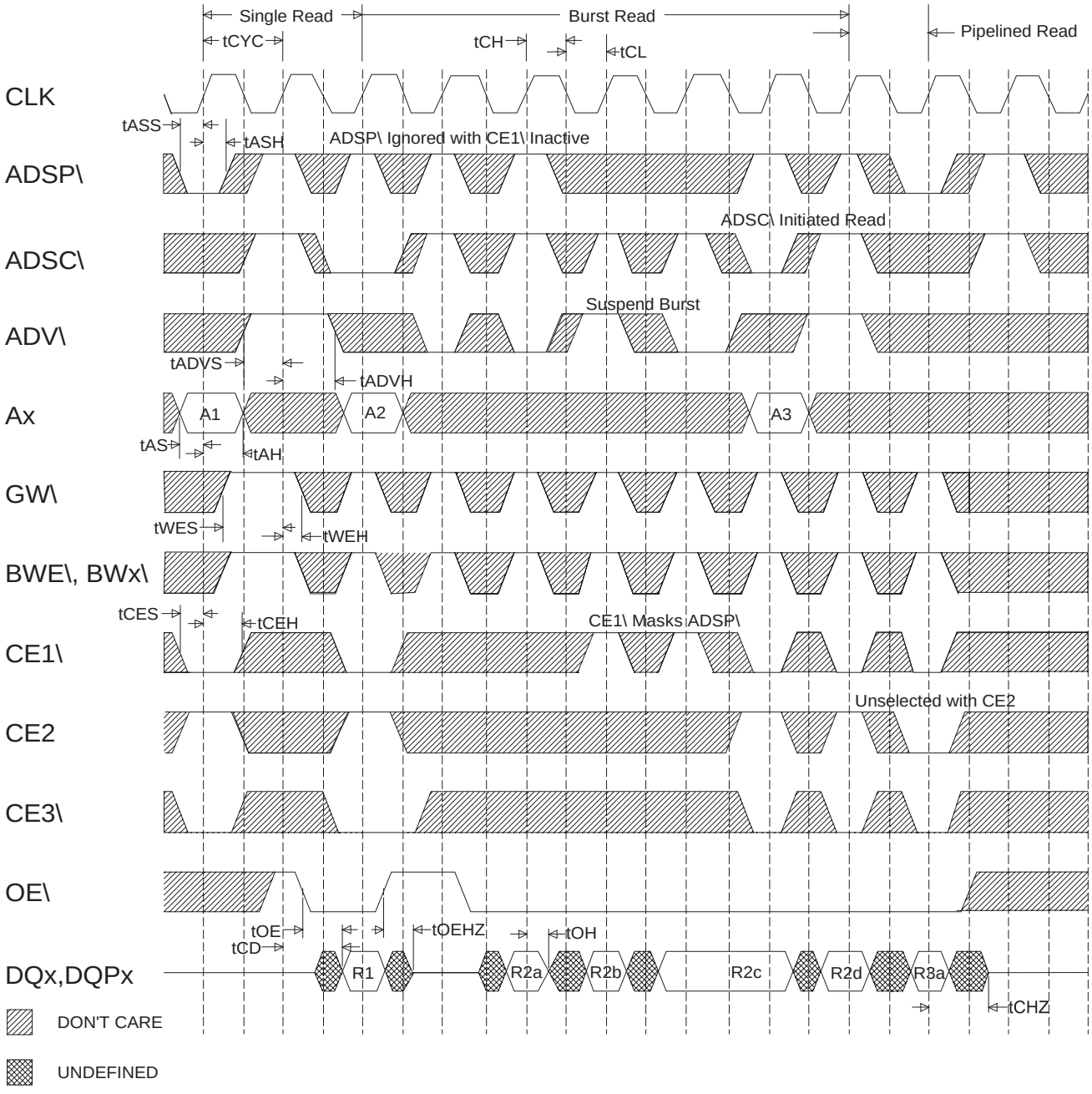
AC SWITCHING WAVEFORMS

Write Cycle Timing



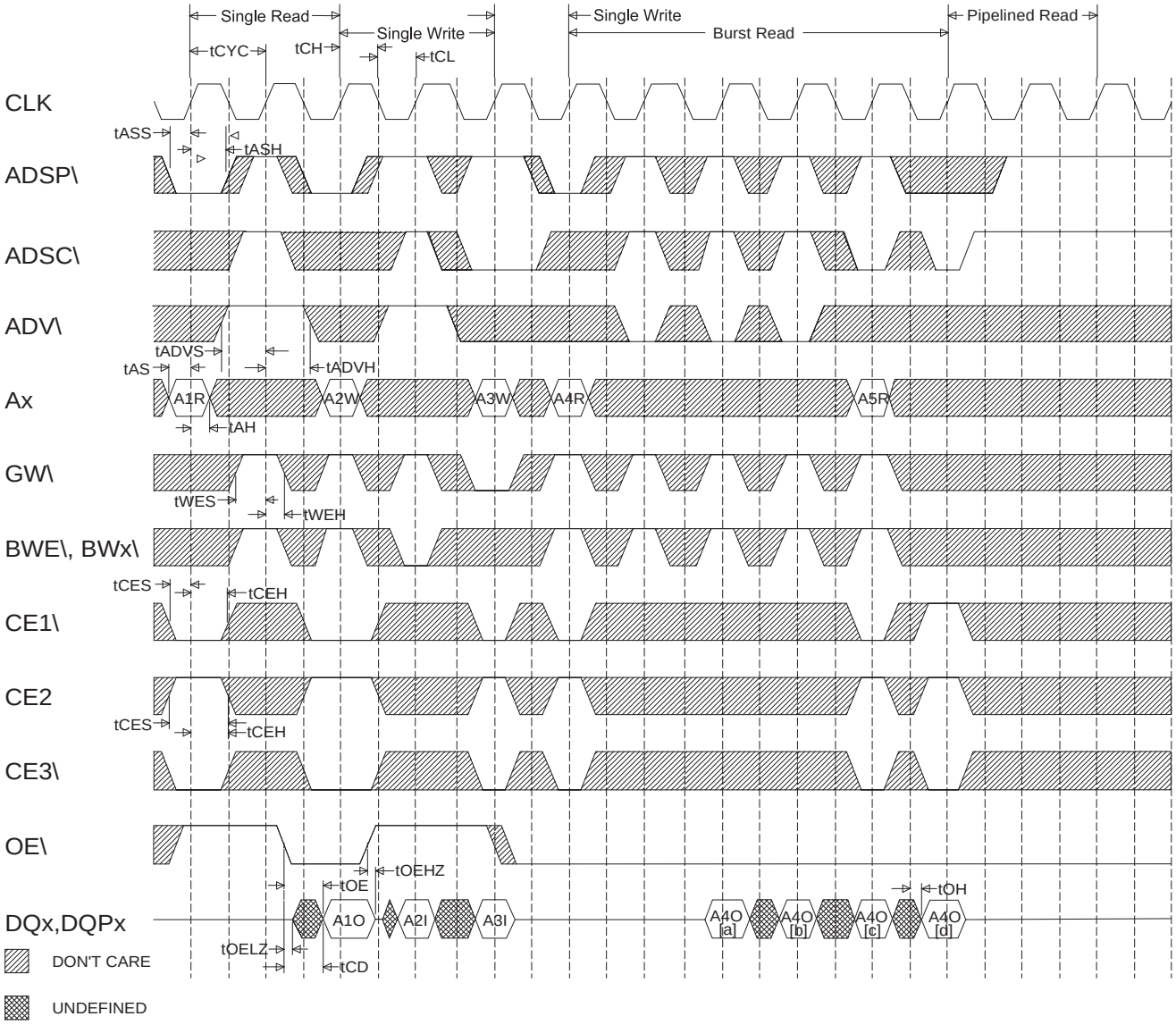
AC SWITCHING WAVEFORMS

Read Cycle Timing



AC SWITCHING WAVEFORMS

Read/Write Cycle Timing



POWER DOWN (SNOOZE MODE)

Power Down or Snooze is a Power conservation mode which when building large/very dense arrays, using multiple devices in a multi-banked or paged array, can greatly reduce the Operating current requirements of your total memory array solution.

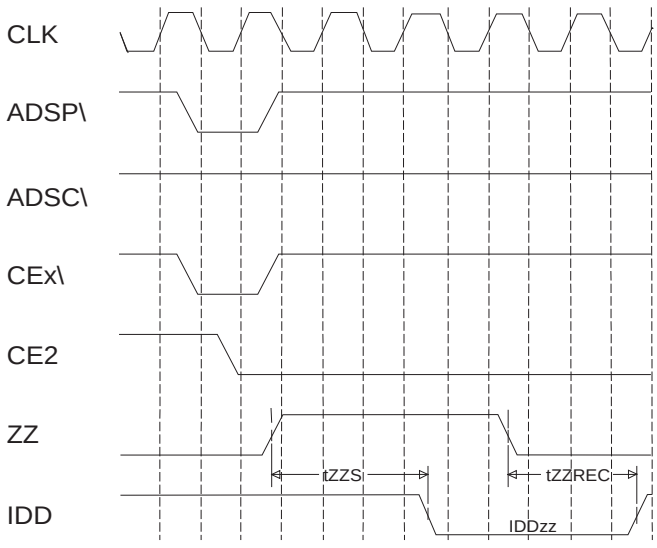
The device is placed in this mode via the use of the ZZ pin, an asynchronous control pin which when asserted, places the array into the lower power or Power Down mode. Awakening the array or leaving the Power Down (SNOOZE) mode is done so by de-asserting the ZZ pin .

While in the Power Down or Snooze mode, Data integrity is guaranteed. Accesses pending when the device entered the mode are not considered valid nor is the completion of the operation guaranteed. The device must be de-selected prior to entering the Power Down mode, all Chip Enables, ADSP\ and ADSC\ must remain inactive for the duration of ZZ recovery time (tZZREC).

ZZ MODE ELECTRICAL CHARACTERISTICS

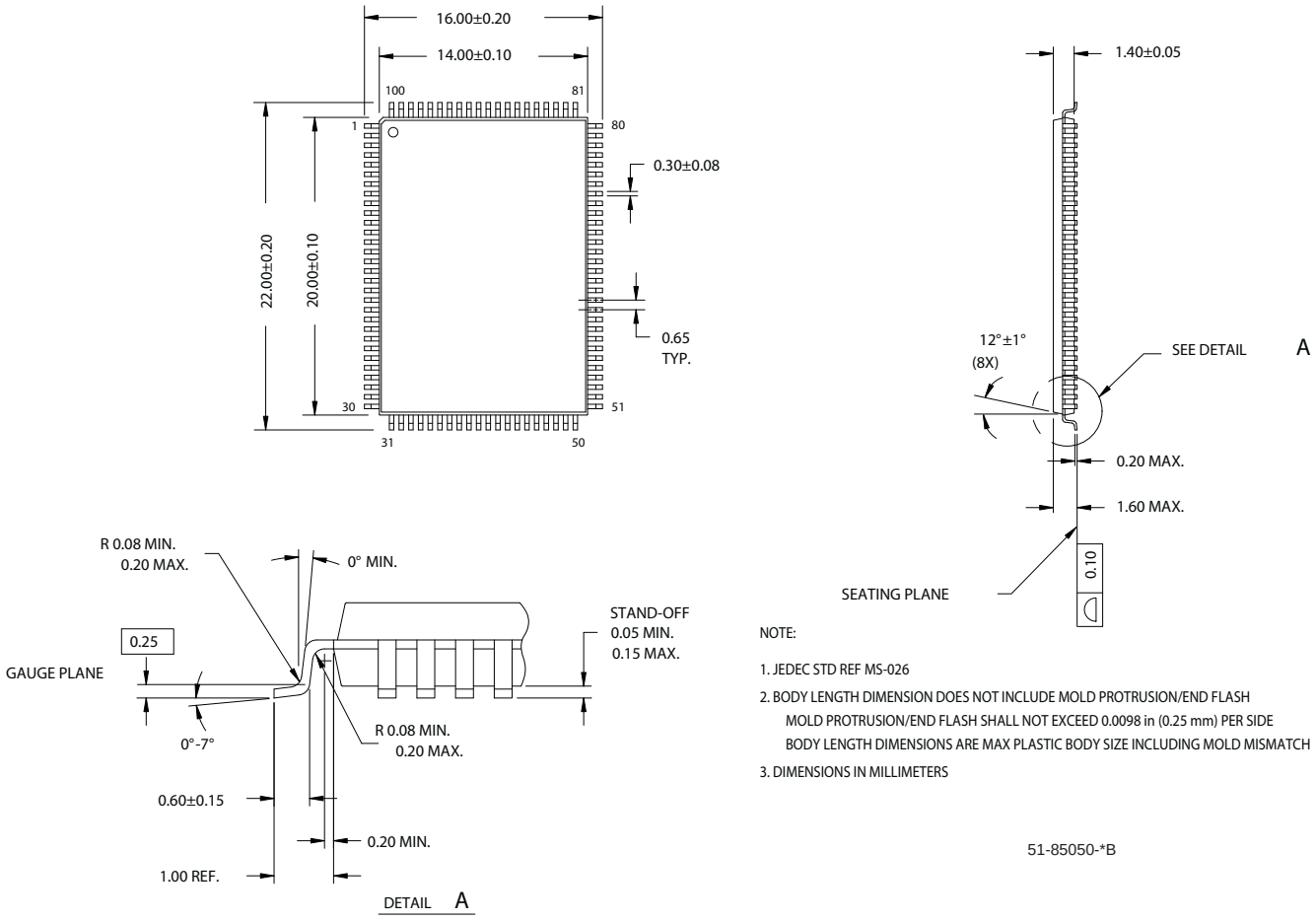
Parameter	Symbol	Test Conditon	Min.	Max.	Units
Power Down (SNOOZE) Mode	**IDDzz**	ZZ >/- VDD - 0.2V		75	mA
ZZ Active (Signal HIGH) to Power Down	**tZZS**	ZZ >/- VDD - 0.2V		2 tCYC	ns
ZZ Inactive (Signal Low) to Power Up	**tZZR**	ZZ </- 0.2V	2 tCYC		ns

ZZ MODE TIMING DIAGRAM



MECHANICAL DIAGRAM

100-Pin TQFP (Package Designator DQ)



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

ORDERING INFORMATION

Part Number	Configuration	tCD (ns)	Clock (Mhz)
TQFP			
AS5SP512K18DQ-30IT	512Kx18, 3.3vCore/3.3,2.5v IO	3.0	**200**
AS5SP512K18DQ-35IT	512Kx18, 3.3vCore/3.3,2.5v IO	3.5	**166**
AS5SP512K18DQ-40IT	512Kx18, 3.3vCore/3.3,2.5v IO	4.0	**133**
AS5SP512K18DQ-30ET	512Kx18, 3.3vCore/3.3,2.5v IO	3.0	**200**
AS5SP512K18DQ-35ET	512Kx18, 3.3vCore/3.3,2.5v IO	3.5	**166**
AS5SP512K18DQ-40ET	512Kx18, 3.3vCore/3.3,2.5v IO	4.0	**133**
AS5SP512K18DQ-35XT	512Kx18, 3.3vCore/3.3,2.5v IO	3.5	**166**
AS5SP512K18DQ-40XT	512Kx18, 3.3vCore/3.3,2.5v IO	4.0	**133**

AVAILABLE PROCESSES

IT = Industrial Temperature Range -40°C to +85°C
ET = Enhanced Temperature Range -40°C to +105°C
XT = Military Temperature Range -55°C to +125°C

DOCUMENT TITLE

9Mb, 512K x 18, Synchronous SRAM

REVISION HISTORY

Rev #	History	Release Date	Status
2.1	Updated Micross information	October 2010	Release
2.2	Added copper lead frame & RoHS options. Deleted I_{SB3} and I_{SB4}.	June 2011	Release
2.3	Added Thermal Resistance for DQC package, page 6.	September 2011	Release
2.4	Removed Cu-lead frame option	October 2013	Release

Changed:	From	To
CCLK &CI	5pF	6pF
CIO	5pF	8pF
IDDzz	35mA	75mA
IDD (200 MHz)	250mA	290mA
IDD (166 MHz)	220mA	270mA
IDD (133 MHz)	185mA	240mA
ISB1 (200 MHz)	120mA	200mA
ISB1 (166 MHz)	110mA	180mA
ISB1 (133 MHz)	100mA	160mA
ISB2	30mA	130mA