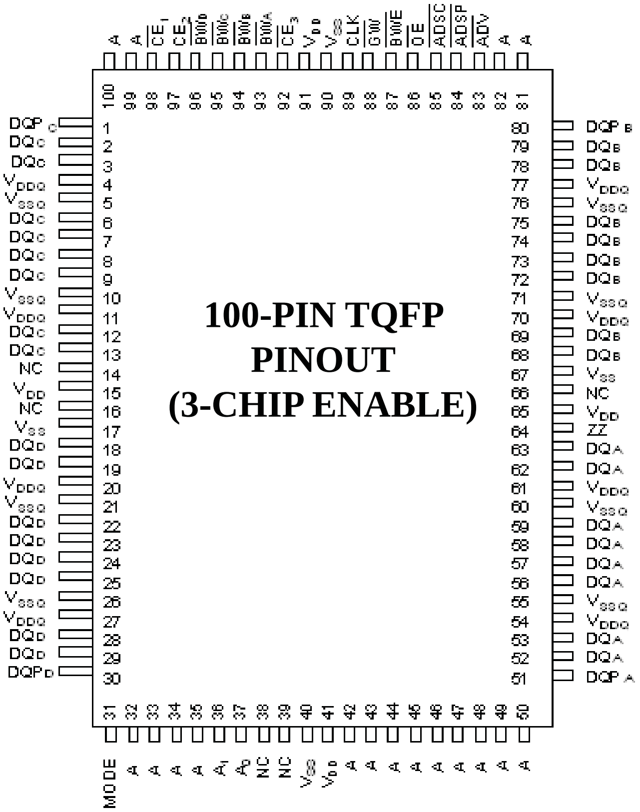
Plastic Encapsulated Microcircuit

18Mb, 512K x 36, Synchronous SRAM

Pipeline Burst, Single Cycle Deselect

FEATURES

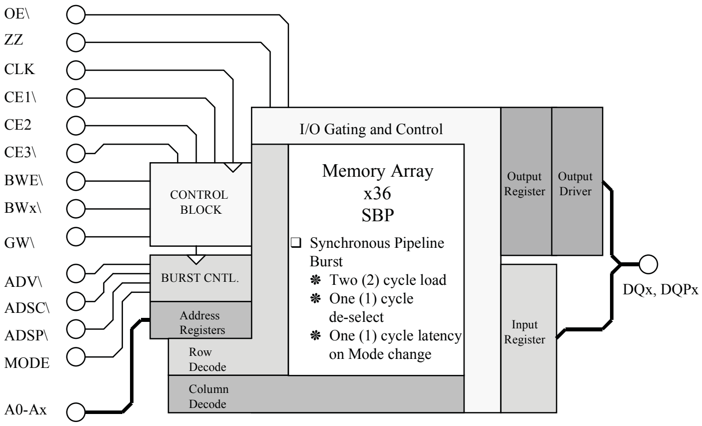
- Synchronous Operation in relation to the input Clock
- 2 Stage Registers resulting in Pipeline operation
- On chip address counter (base +3) for Burst operations
- Self-Timed Write Cycles
- On-Chip Address and Control Registers
- Byte Write support
- Global Write support
- On-Chip low power mode [powerdown] via ZZ pin
- Interleaved or Linear Burst support via Mode pin
- Three Chip Enables for ease of depth expansion without Data Contention.
- Two Cycle load, Single Cycle Deselect
- Asynchronous Output Enable (OE\)
- Three Pin Burst Control (ADSP\, ADSC\, ADV\)
- 3.3V Core Power Supply
- 3.3V/2.5V IO Power Supply
- JEDEC Standard 100 pin TQFP Package
- Available in **Industrial**, **Enhanced**, and **Mil-Temperature** Operating Ranges
- RoHs compliant options available


100-PIN TQFP PINOUT (3-CHIP ENABLE)

Fast Access Times

Parameter	Symbol	200Mhz	166Mhz	133Mhz	Units
Cycle Time	tCYC	5.0	6.0	7.5	ns
Clock Access Time	tCD	3.1	3.5	4.0	ns
Output Enable Access Time	tOE	3.1	3.5	4.0	ns

Block Diagram



GENERAL DESCRIPTION

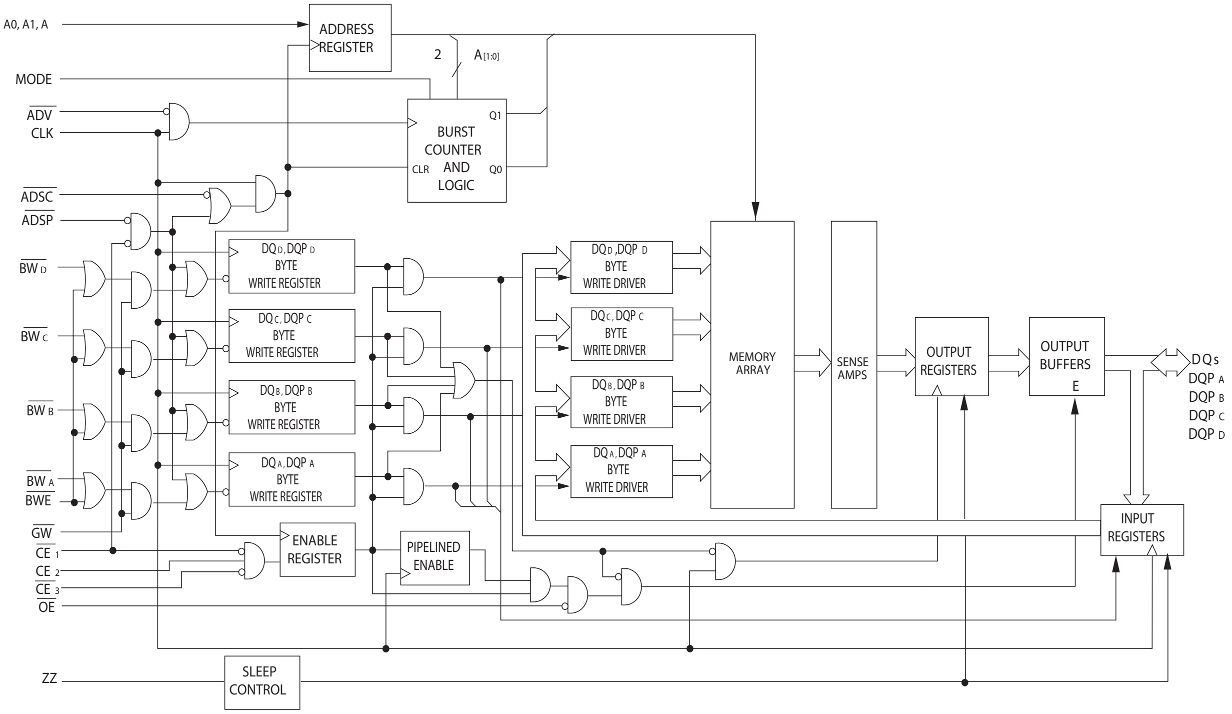
The AS5SP512K36 is a 18Mb High Performance Synchronous Pipeline Burst SRAM, available in multiple temperature screening levels, fabricated using High Performance CMOS technology and is organized as a 512K x 36 array. It integrates address and control registers, a two (2) bit burst address counter supporting four (4) double-word transfers. Writes are internally self-timed and synchronous to the rising edge of clock.

The AS5SP512K36 includes advanced control options including Global Write, Byte Write as well as an asynchronous output enable. Burst Cycle controls are handled by three (3) input pins, ADV\, ADSP\ and ADSC\. Burst operation can be initiated with either the Address Status Processor (ADSP\) or Address Status controller (ADSC\) inputs. Subsequent burst addresses are generated internally in the system's burst sequence control block and are controlled by the Address Advance (ADV\) control input.

Pin Descriptions

Clock	**CLK**	Input	**89**	Synchronous clock.
Address	**A0, A1**	Sync Input	**37, 36**	Low order, synchronous address inputs and burst counter address inputs.
Address	**A**	Sync Input(s)	**35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43, 42**	Synchronous address inputs
Chip Enable	**CE1\, CE3**	Sync Input	**98, 92**	Active low chip enables.
Chip Enable	**CE2**	Sync Input	**97**	Active high chip enable.
Global Write Enable	**GW**	Sync Input	**88**	Active low global write enable. Write to all bits.
Byte Enables	**BWa\, BWb\, BWc\, BWd**	Sync Input	**93, 94, 95, 96**	Active low byte write enables. Write to byte segments.
Byte Write Enable	**BWE**	Sync Input	**87**	Active low byte write function enable.
Output Enable	**OE**	Input	**86**	Active low asynchronous output enable.
Address Status Controller	**ADSC**	Sync Input	**85**	When asserted LOW, address is captured in the address registers and A0-A1 are loaded into the burst counter when ADSP\ and ADSC\ are both asserted, only ADSP\ is recognized.
Address Status Processor	**ADSP**	Sync Input	**84**	When asserted LOW, address is captured in the address registers, A0-A1 is registered in the burst counter. When both ADSP\ and ADSC\ or both asserted, only ADSP\ is recognized. ADSP\ is ignored when CE1\ is HIGH.
Address Advance	**ADV**	Sync Input	**83**	When asserted LOW, address in burst counter is incremented on rising edge of clock.
Power-Down	**ZZ**	Input	**64**	Asynchronous, non-time critical Power-down Input control. Places the chip into an ultra low power mode, with data preserved.
Data Parity Input/Outputs	**DQPa, DQPb, DQPc, DQPd**	Sync Input/ Output	**51, 80, 1, 30**	Synchronous parity on input/output.
Data Input/Outputs	**DQa, DQb, DQc, DQd**	Sync Input/ Output	**52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29**	Synchronous data input/output.
Burst Mode	**MODE**	Input	**31**	Interleaved or linear burst mode control.
Power Supply [Core]	**VDD**	Supply	**91, 15, 41, 65**	Core power supply.
Ground [Core]	**VSS**	Supply	**90, 17, 40, 67**	Core power supply ground.
Power Supply I/O	**VDDQ**	Supply	**4, 11, 20, 27, 54, 61, 70, 77**	Isolated input/output buffer supply.
I/O Ground	**VSSQ**	Supply	**5, 10, 21, 26, 55, 60, 71, 76**	Isolated input/output buffer ground.
No Connection(s)	**NC**	NA	**14, 16, 38, 39, 66**	No connections to internal silicon.

Logic Block Diagram



Functional Description

Micross Components AS5SP512K36 Synchronous SRAM is manufactured to support today's High Performance platforms utilizing the industry's leading processor elements including those of Intel and Motorola. The AS5SP512K36 supports Synchronous SRAM READ and WRITE operations as well as Synchronous Burst READ/WRITE operations. All inputs with the exception of OE\, MODE and ZZ are synchronous in nature and registered on the rising edge of input clock (CLK). The type, start and duration of Burst Mode operations is controlled by MODE, ADSC\, ADSP\ and ADV\. All synchronous accesses, including the Burst accesses, are enabled via the use of the multiple enable pins, and wait state insertion is supported and controlled via the use of the Address Advance (ADV\).

The AS5SP512K36 supports both Interleaved and Linear Burst modes.

The AS5SP512K36 supports Byte WRITE operations via the Byte Write Enable (BWE\) and the Byte Write Select pin(s) (BWa\, BWb\, BWc\, BWd\). Global Writes are supported via the Global Write Enable (GW\). Global Write Enable will override the Byte Write inputs and will perform a Write to all 36 Data Bits.

The AS5SP512K36 provides ease of producing very dense arrays via the multiple Chip Enable input pins and Asynchronous Output Enable.

Single Cycle Access Operations

A Single READ operation is initiated at the rising edge of Clock when all of the following conditions are satisfied: [1] ADSP\ or ADSC\ is asserted LOW, [2] Chip Enables are all asserted active, and [3] the WRITE signals (GW\, BWE\) are HIGH. ADSP\ is ignored if CE1\ is HIGH. The address presented to the Address inputs is stored within the Address Registers and Address Counter/Advancement Logic and presented to the array core. The corresponding data of the addressed location is propagated to the Output Registers and passed to the data bus on the next rising clock via the Output Buffers. The time at which the data is presented to the Data bus is as specified by either the Clock to Data valid specification or the Output Enable to Data Valid spec for the device speed grade chosen. The only exception occurs when the device is emerging from a deselected to selected state where its outputs are tristated in the first machine cycle and controlled by its Output Enable (OE\) on following cycle. Consecutive single cycle READS are supported. Once the SRAM is deselected by use of the Chip Enable(s) and either ADSP\ or ADSC\, its outputs will tri-state immediately.

A Single ADSP\ controlled WRITE operation is initiated when both of the following conditions are satisfied at the rising edge of Clock: [1] ADSP\ is asserted LOW, and [2] Chip Enable(s) are asserted ACTIVE. The WRITE controls: Global Write, Byte Write Enable (GW\, BWE\) the individual Byte Writes (BWa\, BWb\, BWc\, BWd\), and ADV\ are ignored on the first machine cycle. ADSP\ triggered WRITE accesses require two (2) machine cycles to complete. If Global Write is asserted LOW on the second Clock (CLK) rise, data will be written into the selected address location. If GW\ is HIGH (inactive) then the WRITE operation is controlled by BWE\ and one or more of the Byte Write controls (BWa\, BWb\, BWc\ and BWd\). All WRITES that are initiated in this device are internally self timed.

A Single ADSC\ controlled WRITE operation is initiated at the rising edge of Clock when the following conditions are satisfied: [1] ADSC\ is asserted LOW, [2] ADSP\ is de-asserted (HIGH), [3] Chip Enable(s) are asserted (TRUE or Active), and [4] the appropriate combination of the WRITE inputs (GW\, BWE\, BWx\) are asserted (ACTIVE). ADSC\ triggered WRITE accesses require a single clock (CLK) machine cycle to complete. The ADV\ pin is ignored during this cycle.

Deep Power-Down Mode (SLEEP)

The AS5SP512K36 has a Deep Power-Down mode and is controlled by the Asynchronous ZZ pin. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, Data integrity is guaranteed. For the device to be placed successfully into this operational mode the device must be deselected and the Chip Enables, ADSP\ and ADSC\ remain inactive for the duration of tZZREC after the ZZ input returns LOW. Accesses pending when entering "sleep" mode are not considered valid.

Synchronous Truth Table (1, 2)

CE1\	CE2	CE3\	ADSP\	ADSC\	ADV\	WT / RD	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	NA	Not Selected
L	L	X	L	X	X	X	↑	NA	Not Selected
L	X	H	L	X	X	X	↑	NA	Not Selected
L	L	X	H	L	X	X	↑	NA	Not Selected
L	X	H	H	L	X	X	↑	NA	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst, READ
L	H	L	H	L	X	WT	↑	External Address	Begin Burst, WRITE
L	H	L	H	L	X	RD	↑	External Address	Begin Burst, READ
X	X	X	H	H	L	RD	↑	Next Address	Continue Burst, READ
H	X	X	X	H	L	RD	↑	Next Address	Continue Burst, READ
X	X	X	H	H	L	WT	↑	Next Address	Continue Burst, WRITE
H	X	X	X	H	L	WT	↑	Next Address	Continue Burst, WRITE
X	X	X	H	H	H	RD	↑	Current Address	Suspend Burst, READ
H	X	X	X	H	H	RD	↑	Current Address	Suspend Burst, READ
X	X	X	H	H	H	WT	↑	Current Address	Suspend Burst, WRITE
H	X	X	X	H	H	WT	↑	Current Address	Suspend Burst, WRITE

Notes:

1. X = Don’t Care
2. WT= WRITE operation in WRITE TABLE, RD= READ operation in WRITE TABLE

Burst Sequence Tables

Interleaved Burst

Burst Control Pin [MODE]	State	Case 1		Case 2		Case 3		Case 4	
	HIGH	A1	A0	A1	A0	A1	A0	A1	A0
First Address	▨	0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

Linear Burst

Burst Control Pin [MODE]	State	Case 1		Case 2		Case 3		Case 4	
	LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	▨	0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Capacitance

Parameter	Symbol	Max.	Units
Input Capacitance	**CI**	6	pF
Input/Output Capacitance	**CIO**	8	pF

Write Table

GW\	BW\	BWa\	BWb\	BWc\	BWd\	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE Byte [A]
H	L	H	L	H	H	WRITE Byte [B]
H	L	H	H	L	L	WRITE Byte [C], [D]
H	L	L	L	L	L	WRITE ALL Bytes
L	X	X	X	X	X	WRITE ALL Bytes

Asynchronous Truth Table

Operation	ZZ	OE\	I/O Status
Power-Down (SLEEP)	H	X	High-Z
READ	L	L	DQ
	L	H	High-Z
WRITE	L	X	Din, High-Z
De-Selected	L	X	High-Z

Absolute Maximum Ratings*

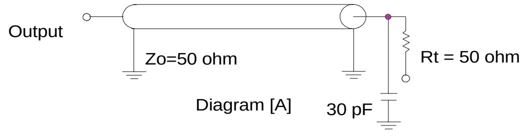
Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Voltage on VDD Pin	**VDD**	-0.3	4.6	V
Voltage on VDDQ Pins	**VDDQ**		VDD	V
Voltage on Input Pins	**VIN**	-0.3	VDD+0.3	V
Voltage on I/O Pins	**VIO**	-0.3	VDDQ+0.3	V
Power Dissipation	**PD**		1.6	W
Storage Temperature	**tSTG**	-65	150	°C
Operating Temperatures [Screening Levels]	**/IT**	-40	85	°C
	/ET	-40	105	°C
	/XT	-55	125	°C

**Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for any duration or segment of time may affect device reliability.*

AC Test Loads

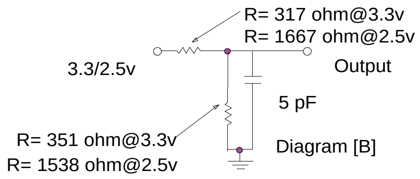
Figure 1



Vt= Termination Voltage
Rt= Termination Resistor

Vt= 1.50v for 3.3v VDDQ
Vt= 1.25v for 2.5v VDDQ

Figure 2



DC Electrical Characteristics (VDD = 3.3v ± 5%, VDDQ = 3.3V/2.5V ± 5%, VDDQ ≤ VDD) [1, 2] TA=Min. and Max temperatures of Screening level chosen

Symbol	Parameter	Test Conditions		Min	Max	Units	Notes
VDD	Power Supply Voltage			3.465	3.630	V	
VDDQ	I/O Supply Voltage			2.375	VDD	V	4
VoH	Output High Voltage	VDD=Min., IOH=-4mA	3.3v	2.4		V	
		VDD=Min., IOH=-1mA	2.5v	2		V	
VoL	Output Low Voltage	VDD=Min., IOL=8mA	3.3v		0.4	V	
		VDD=Min., IOL=1mA	2.5v		0.4	V	
VIH	Input High Voltage		3.3v	2		V	
			2.5v	1.7		V	
VIL	Input Low Voltage		3.3v		0.8	V	
			2.5v		0.7	V	
IIL	Input Leakage (except ZZ) Mode Pin	VDD=Max., VIN=VSS to VDD		-5	5	uA	3
IZ	Input Leakage, ZZ pin			-30	30	uA	3
IOL	Output Leakage	Output Disabled, VOUT=VSSQ to VDDQ		-5	5	uA	
IDD	Operating Current	VDD=Max., f=Max., IOH=0mA	5.0ns Cycle, 200 Mhz		475	mA	
			6.0ns Cycle, 166 Mhz		425	mA	
			7.5ns Cycle, 133 Mhz		375	mA	
ISB1	Automatic CE, Power Down Current - TTL inputs	Max VDD, De-Selected, VIN>=VIH or VIN</=VIL f=1/tCYC					
			5.0ns Cycle, 200 Mhz		250	mA	
			6.0ns Cycle, 166 Mhz		225	mA	
			7.5ns Cycle, 133 Mhz		200	mA	
ISB2	CMOS Standby	Max. VDD, Device deselected, VIN </=0.3V or VIN>/=VDDQ-0.3V f=1/tCYC			200	mA	

Thermal Resistance

Parameter	Description	Test Conditions	DQ Package	DQC Package	Unit
Θ JA	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	28.66	30.2	°C/W
Θ JC	Thermal Resistance (Junction to Case)		4.08	6.5	°C/W

Notes:

[1] All Voltages referenced to VSS (Logic Ground)
[2] Overshoot: VIH(AC) < VDD +1.5V (Pulsewidth less than tCYC/2)
Undershoot: VIL(AC) > -2V (Pulsewidth less than tCYCLZ)
tPower-up: Assumes a linear amp from OV to VDD(MIN) within zooms.
During this time VIH ≤ VDD and VDDQ ≤ VDD
[3] MODE and ZZ pins have internal pull-up resistors
[4] VDDQ should never exceed VDD, VDD and VDDQ can be connected together

AC Switching Characteristics (VDD = 3.3v ± 5%, VDDQ = 3.3V/2.5V ± 5%, VDDQ ≤ VDD) [1]

TA=Min. and Max temperatures of Screening level chosen

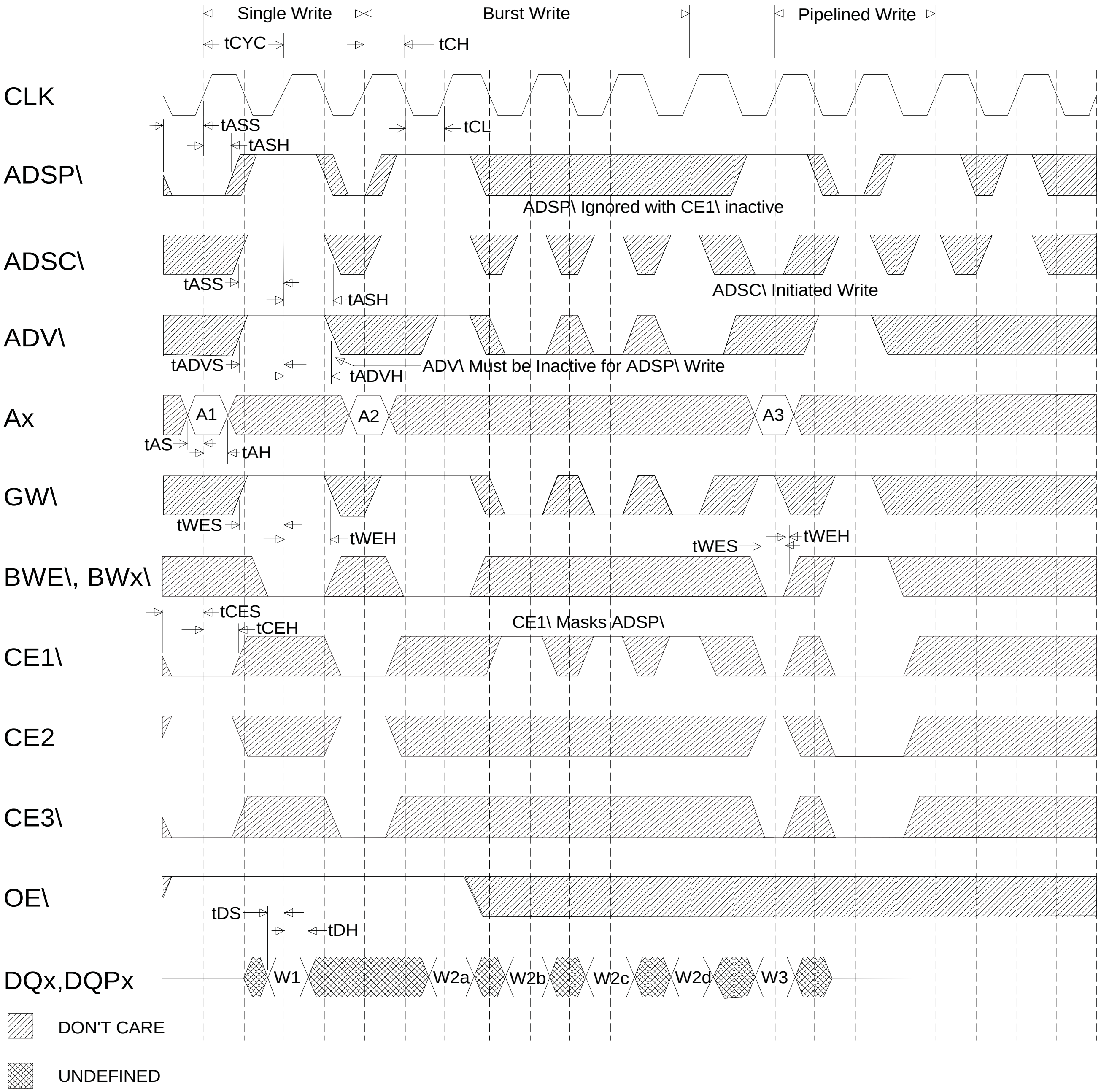
Parameter	Symbol	-30 [200Mhz]		-35 [166Mhz]		-40 [133Mhz]		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Clock (CLK) Cycle Time	**tCYC**	5.00	-	6.00	-	7.50	-	ns	
Clock (CLK) High Time	**tCH**	2.00	-	2.20	-	2.50	-	ns	
Clock (CLK) Low Time	**tCL**	2.00	-	2.20	-	2.50	-	ns	
Clock Access Time	**tCD**		3.10		3.50		4.00	ns	
Clock (CLK) High to Output Low-Z	**tCLZ**	1.00	-	1.00	-	1.00	-	ns	2,3
Clock High to Output High-Z	**tCHZ**	1.25	3.00	1.25	3.50	1.25	3.50	ns	2,3
Output Enable to Data Valid	**tOE**	-	3.10	-	3.50	-	4.00	ns	
Output Hold from Clock High	**tOH**	1.25	-	1.25	-	1.25	-	ns	
Output Enable Low to Output Low-Z	**tOELZ**	0.00	-	0.00	-	0.00	-	ns	2,3
Output Enable High to Output High-Z	**tOEHZ**	-	3.00	-	3.50	-	3.50	ns	2,3
Address Set-up to CLK High	**tAS**	1.40		1.50		1.50		ns	
Address Hold from CLK High	**tAH**	0.40		0.50		0.50		ns	
Address Status Set-up to CLK High	**tASS**	1.40		1.50		1.50		ns	
Address Status Hold from CLK High	**tASH**	0.40		0.50		0.50		ns	
Address Advance Set-up to CLK High	**tADVS**	1.40		1.50		1.50		ns	
Address Advance Hold from CLK High	**tADVH**	0.40		0.50		0.50		ns	
Chip Enable Set-up to CLK High (CEx\, CE2)	**tCES**	1.40		1.50		1.50		ns	
Chip Enable Hold from CLK High (CEx\, CE2)	**tCEH**	0.40		0.50		0.50		ns	
Data Set-up to CLK High	**tDS**	1.40		1.50		1.50		ns	
Data Hold from CLK High	**tDH**	0.40		0.50		0.50		ns	
Write Set-up to CLK High (GW\, BWE\, BWx\)	**tWES**	1.40		1.50		1.50		ns	
Write Hold from CLK High (GW\, BWE\, BWX\)	**tWEH**	0.40		0.50		0.50		ns	
ZZ High to Power Down	**tPD**		2		2		2	cycles	
ZZ Low to Power Up	**tPU**		2		2		2	cycles	

Notes to Switching Specifications:

1. Configuration signal mode is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

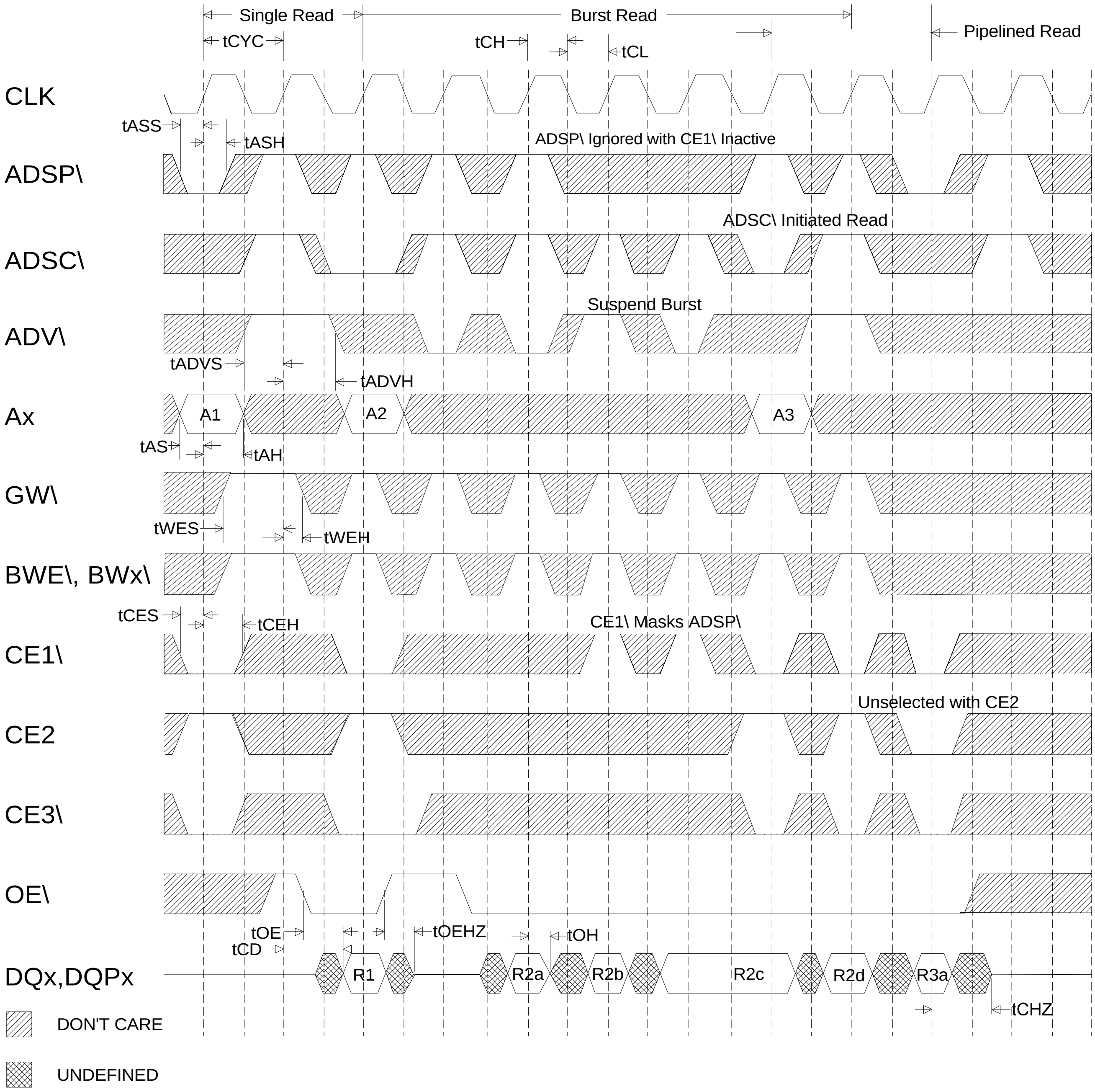
AC SWITCHING WAVEFORMS

Write Cycle Timing



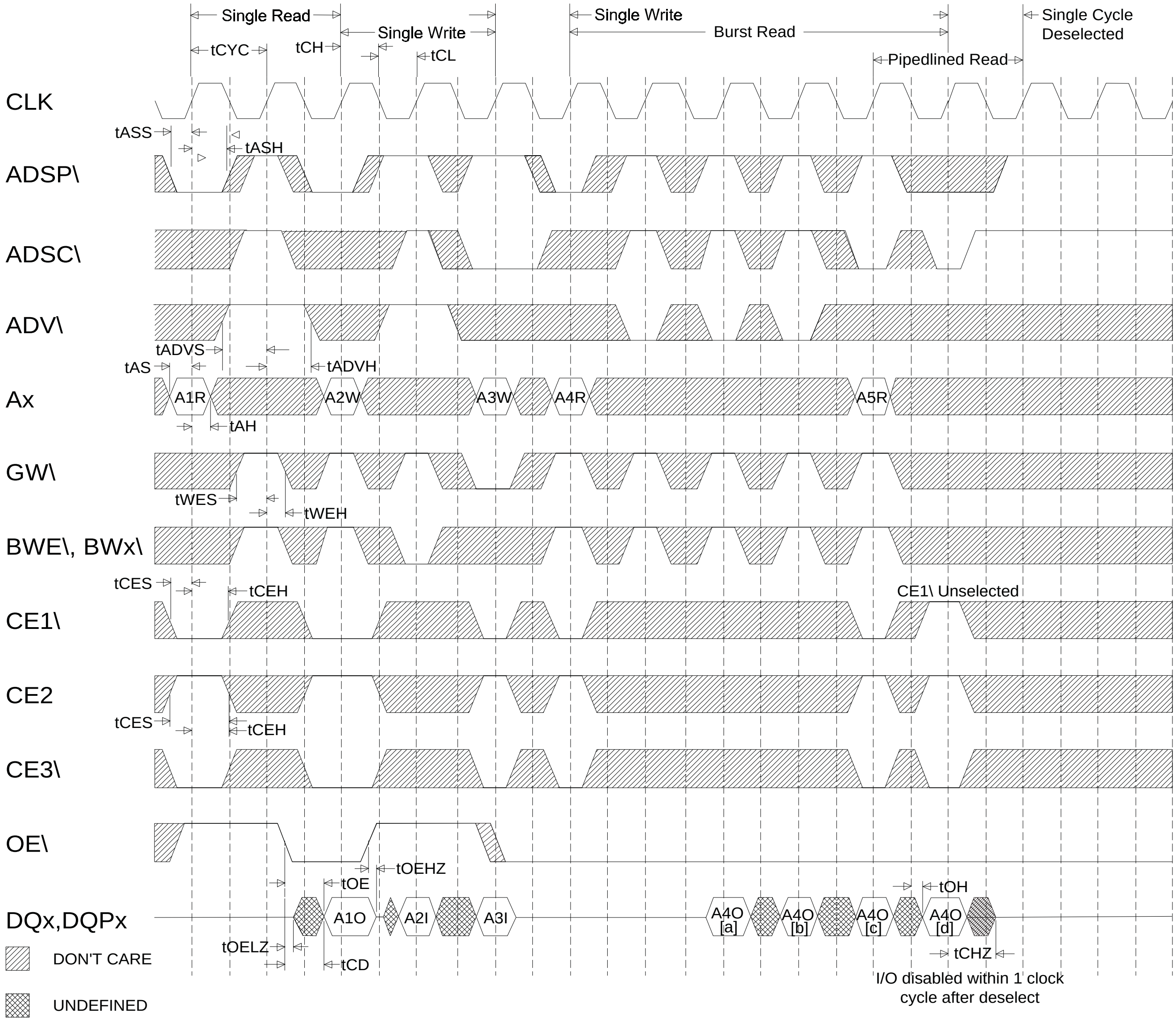
AC SWITCHING WAVEFORMS

Read Cycle Timing



AC SWITCHING WAVEFORMS

Read/Write Cycle Timing



POWER DOWN (SLEEP MODE)

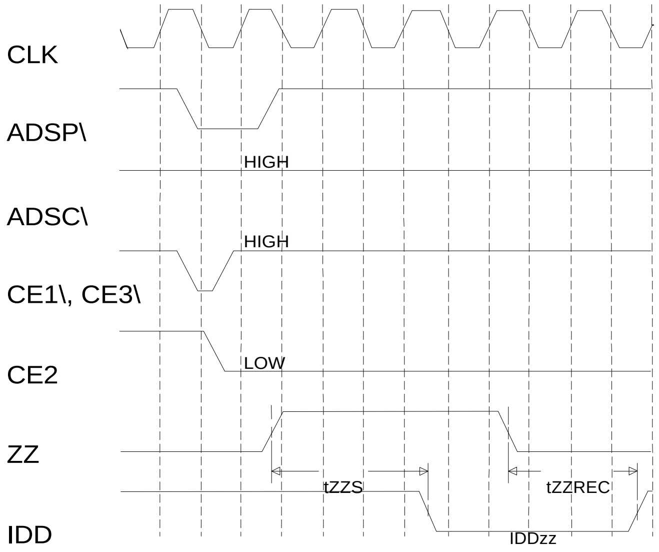
The device is placed in this SLEEP mode via the use of the ZZ pin, an asynchronous control pin which when asserted, places the array into the lower power or Power Down mode. Awakening the array or leaving the Power Down (SLEEP) mode is done so by de-asserting the ZZ pin .

While in the Power Down or Snooze mode, Data integrity is guaranteed. Accesses pending when the device entered the mode are not considered valid nor is the completion of the operation guaranteed. The device must be de-selected prior to entering the Power Down mode, all Chip Enables, ADSP\ and ADSC\ must remain inactive for the duration of ZZ recovery time (tZZREC).

ZZ MODE ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditon	Min.	Max.	Units
Power Down (SNOOZE) Mode	**IDDzz**	ZZ >/- VDD - 0.2V		165	mA
ZZ Active (Signal HIGH) to Power Down	**tZZS**	ZZ >/- VDD - 0.2V		2 tCYC	ns
ZZ Inactive (Signal Low) to Power Up	**tZZR**	ZZ </- 0.2V	2 tCYC		ns

ZZ MODE TIMING DIAGRAM [1, 2]



1. Device must be deselected when entering ZZ mode. See Synchronous Truth table for all signal conditions to deselect device.
2. I/O's are in three-state when exiting ZZ sleep mode.

ORDERING INFORMATION

TQFP

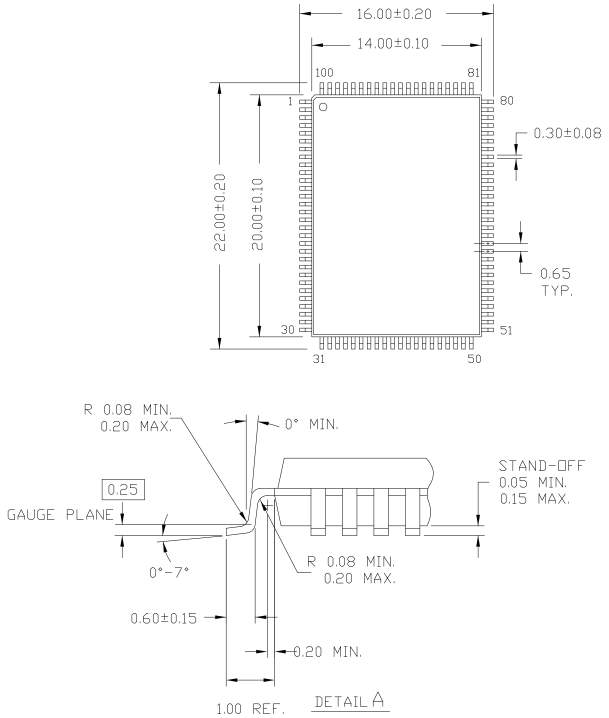
Device Number	Configuration	tCD (ns)	Clock (Mhz)
AS5SP512K36DQ-30/IT	512Kx36, 3.3vCore/3.3,2.5vIO	3.1	**200**
AS5SP512K36DQ-35/IT	512Kx36, 3.3vCore/3.3,2.5vIO	3.5	**166**
AS5SP512K36DQ-40/IT	512Kx36, 3.3vCore/3.3,2.5vIO	4.0	**133**
AS5SP512K36DQ-30/ET	512Kx36, 3.3vCore/3.3,2.5vIO	3.1	**200**
AS5SP512K36DQ-35/ET	512Kx36, 3.3vCore/3.3,2.5vIO	3.5	**166**
AS5SP512K36DQ-40/ET	512Kx36, 3.3vCore/3.3,2.5vIO	4.0	**133**
AS5SP512K36DQ-35/XT	512Kx36, 3.3vCore/3.3,2.5vIO	3.5	**166**
AS5SP512K36DQ-40/XT	512Kx36, 3.3vCore/3.3,2.5vIO	4.0	**133**

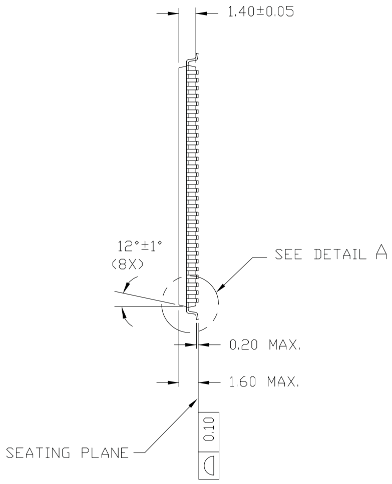
AVAILABLE PROCESSES

IT = Industrial Temperature Range	-40°C to +85°C
ET = Enhanced Temperature Range	-40°C to +105°C
XT = Military Temperature Range	-55°C to +125°C

MECHANICAL DEFINITION

100-Pin TQFP (Package Designator DQ)





NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

DOCUMENT TITLE

Plastic Encapsulated Microcircuit , 18Mb, 512K x 36, Synchronous SRAM
Pipeline Burst, Single Cycle Deselect

REVISION HISTORY

<table>
<tr><th>Rev #</th><th>History</th><th>Release Date</th><th>Status</th></tr>
<tr><td>2.5</td><td>updated max ratings & DC Electrical Characteristics</td><td>September 2008</td><td>Release</td></tr>
<tr><td>2.6</td><td>Updated Micross Information</td><td>October 2010</td><td>Release</td></tr>
<tr><td>2.7</td><td>Changed ADV\ description text from HIGH to LOW on page 2, Edited ADV\ Write Cycle Timing drawing on page 7</td><td>November 2010</td><td>Release</td></tr>
<tr><td>2.8</td><td>Added copper lead frame and RoHS compliant options, Updated IDDzz, pg 10 from 35mA to 165mA, Updated logic block diagram on page 2. Changed t_{CLZ}min from 1.25ns to 1.0ns. Corrected -30 t_{OH} from 1.65ns to 1.25ns.
Changed:
<table>
<tr><th>Spec</th><th>Device</th><th>From</th><th>To</th><th></th></tr>
<tr><td>I_{DD}</td><td>5ns Cycle</td><td>350</td><td>475</td><td>mA</td></tr>
<tr><td></td><td>6ns Cycle</td><td>300</td><td>425</td><td>mA</td></tr>
<tr><td></td><td>7.5ns Cycle</td><td>275</td><td>375</td><td>mA</td></tr>
<tr><td>I_{SB1}</td><td>5ns Cycle</td><td>160</td><td>250</td><td>mA</td></tr>
<tr><td></td><td>6ns Cycle</td><td>150</td><td>225</td><td>mA</td></tr>
<tr><td></td><td>7.5ns Cycle</td><td>140</td><td>200</td><td>mA</td></tr>
<tr><td>I_{SB2}</td><td>All</td><td>70</td><td>200</td><td>mA</td></tr>
<tr><td>I_{SB3}</td><td>All</td><td>80</td><td>250</td><td>mA</td></tr>
<tr><td>Deleted I_{SB4}</td><td>Specification</td><td></td><td></td><td></td></tr>
</table></td><td>May 2011</td><td>Release</td></tr>
<tr><td>2.9</td><td>Added Thermal Resistance for DQC package, page 5.</td><td>September 2011</td><td>Release</td></tr>
<tr><td>3.0</td><td>Removed Cu-lead frame option</td><td>October 2013</td><td>Release</td></tr>
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