512K x 36 SSRAM

Flow-Through SRAM
No Bus Latency

AVAILABLE AS MILITARY SPECIFICATIONS

•MIL-STD-883

FEATURES

- Pin compatible and functionally equivalent to ZBT devices.
- Supports 133MHz bus operations with zero wait states
  -Data is transferred on every clock
- Internally self-timed output buffer control to eliminate the need to use asynchronous OE\
- Registered inputs for Flow-Through operation
- Byte Write capability
- Common I/O architecture
- Fast clock-to-output times
  -6.5ns (for 133 MHz device)*
  -8.5ns (for 100 MHz device)
- Single 3.3V -5% and +1-% power supply V_{DD}
- Separate V_{DD} for 3.3V or 2.5V I/O
- Clock Enable (CEN\) pin to suspend operation
- Synchronous self-timed writes
- Available in 100-pin TSOP package.**
- Burst Capability - linear or interleaved burst order
- No bus latency architecture eliminated dead cycles between write and read cyccles

OPTIONS — MARKING

- Timing
  6.5ns access — -6.5*
  8.5ns access — -8.5

- Operating Temperature Ranges
  Military (-55°C to +125°C) XT
  Industrial (-40°C to +85°C) IT

- Package(s)**
  100-pin TQFP — DQ

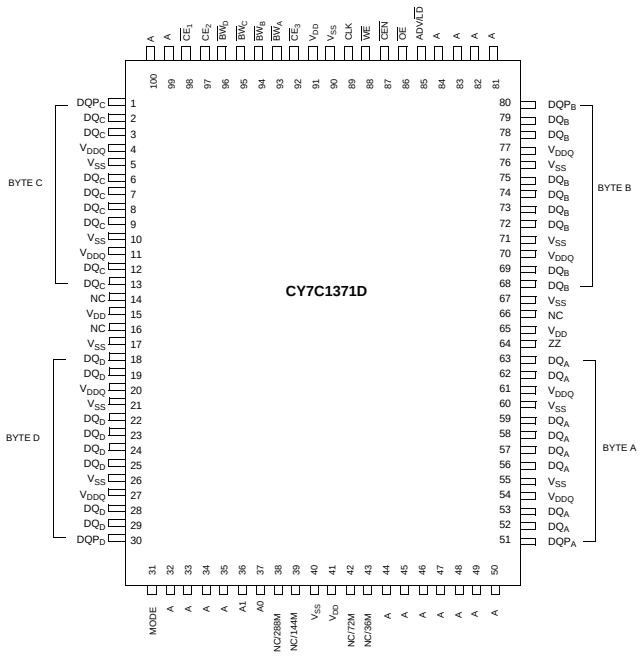
NOTES:
* 6.5ns speed available with IT option only.
**Contact factory for BGA package interests.

GENERAL DESCRIPTION

The AS5SS512K36D is is a 3.3V, 512K x 36 Synchronous flow through Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations with no wait state insertion. The AS5SS512K36D is equipped with the advanced No Bus Latency logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write-Read transitions.

PIN ASSIGNMENT
(Top View)

100-Pin TQFP (DQ)



All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (CEN) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device). Write operations are controlled by the two or four Byte Write Select (BWX) and a Write Enable (WE) input. All writes are conducted with on-chip synchronous self-timed write circuitry. Three synchronous Chip Enables (CE1, CE2, CE3) and an asynchronous Output Enable (OE) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (CEN\) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the Byte Write Selects (BWS\ a,b,c,d) and a Write Enable (WE\) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Synchronous Chip Enable (CE1\, CE2, CE3\) and an asynchronous Output Enable (OE\) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

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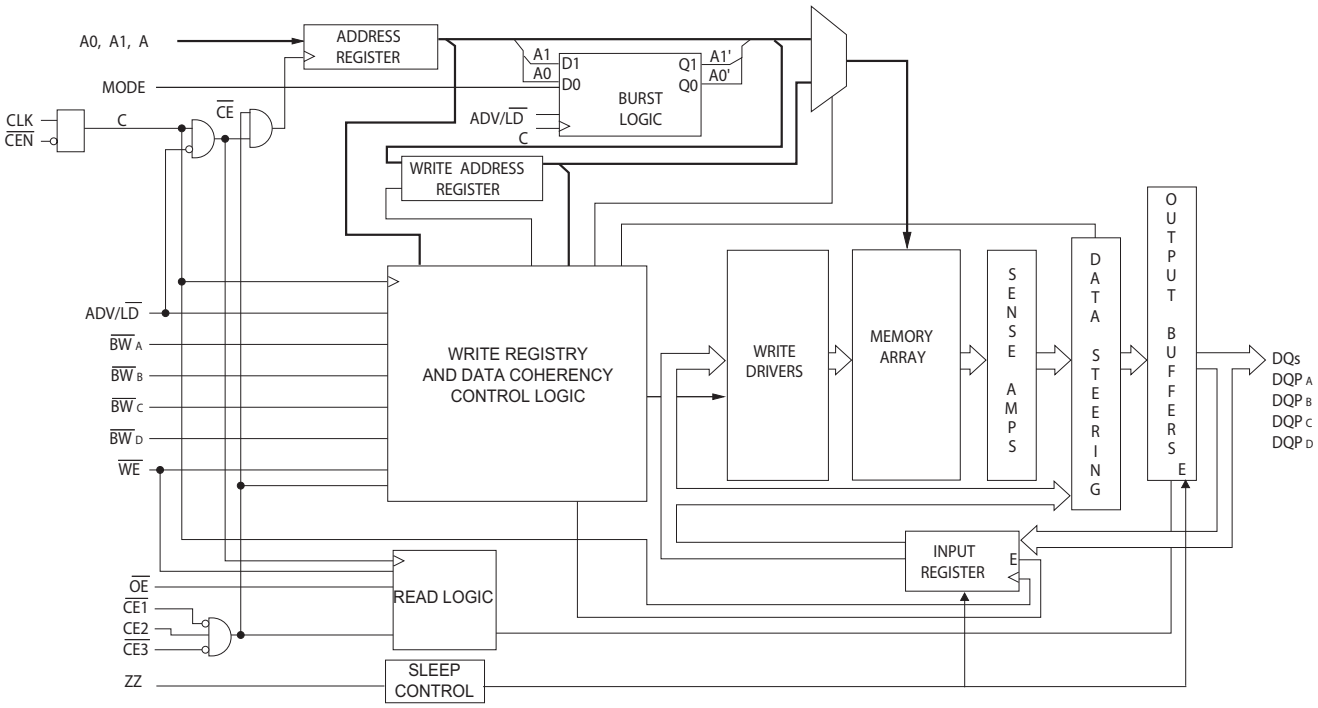
FUNCTIONAL BLOCK DIAGRAM



SELECTION GUIDE

	133 MHz	100 MHz	UNITS
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	210	175	mA
Maximum CMOS Standby Current	70	70	mA

PIN DEFINITIONS

PIN	I/O TYPE	DESCRIPTION
AO A1 A	Input-Synchronous	Address Inputs used to select one of the address locations. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
BWa\ BWb\ BWc\ BWd\	Input-Synchronous	Byte Write Inputs, Active LOW. Qualified with WE to conduct writes to the SRAM. Sampled on the rising edge of CLK.
WE\	Input-Synchronous	Write Enable Input, active LOW. Sampled on the rising edge of CLK if CEN\ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/LD\	Input-Synchronous	Advanced/Lowed Input used to advance the on-chip address counter or load a new address. When HIGH (and CEN\ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/LD\ should be driven LOW in order to load a new address.
CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. CLK is qualified with CEN\. CLK is only recognized if CEN\ is active LOW.
CE1\	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE2 and CE3\ to select/deselect the device.
CE2\	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with CE1\ and CE3\ to select/deselect the device.
CE3\	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE1\ and CE2 to select/deselect the device.
OE\	Input-Asynchronous	Output Enable, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. OE\ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
CEN\	Input-Synchronous	Clock Enable Input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting CEN\ does not deselect the device, CEN\ can be used to extend the previous cycle when required.
ZZ	Input-Synchronous	ZZ “Sleep” Input. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQa DQb DQc DQd	I/O- Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by OE\ and the internal control logic. When OE\ is asserted LOW, the pins can behave as outputs. When HIGH, DQa - DQd are placed in a three-state condition. The outputs are automatically three-stated during the data portion of the write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of OE\.
DPa DPb DPc DPd	I/O- Synchronous	Bidirectional Data Parity I/O lines. Functionally, these signals are identical to DQs.
MODE	Input Strap Pin	Mode Input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
V_{DD}	Power Supply	Power supply inputs to the core of the device.
$V_{DD}Q$	I/O Power Supply	Power supply for the I/O circuitry.
V_{SS}	Ground	Ground for the device. Should be connected to the ground of the system.
NC	---	No connects. Pins are not internally connected.

FUNCTIONAL OVERVIEW

The AS5SS512K36 is a Synchronous Flow-Through Burst NoBL SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN\). If CEN\ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN\.

Accesses can be initiated by asserting chip enables (CE1\, CE2, CE3\) active at the rising edge of the clock. If clock enable (CEN\) is active LOW and ADV/LD\ is asserted LOW, the address presented to the device will be latched. The access can either be a Read or Write operation, depending on the status of the write enable (WE\). Byte Write selects can be used to conduct byte write operations. Write operations are qualified by the write enable (WE\). All writes are simplified with on-chip synchronous self-timed write circuitry

Synchronous chip enable (CE1\, CE2, and CE3\) and an asynchronous output enable (OE\) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/LD\ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CEN\ is asserted LOW, (2) CE1\, CE2, and CE3\ are ALL asserted active, (3) the write enable input signal WE is deasserted HIGH, and 4) ADV/LD\ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 7.5 ns (117-MHz device) provided OE\ is active LOW. After the first clock of the read access the output buffers are controlled by OE\ and the internal control logic. OE\ must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output will be three-stated immediately.

Burst Read Accesses

The AS5SS512K36 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/LD\ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/LD\ will increment the internal burst counter regardless of the state of chip enables inputs or WE\. WE\ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN\ is asserted LOW, (2) chip enables asserted active, and (3) the write signal WE\ is asserted LOW. The address presented is loaded into the address register. The write signals are latched into the Control Logic block. The data lines are automatically three-stated regardless of the state of the OE\ input signal. This allows the external logic to present the data on DQ and DP.

On the next clock rise the data presented to DQ and DP (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete. Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by Byte Write select signals. The AS5SS512K36 provide byte write capability that is described in the Write Cycle Description table. Asserting the write enable input (WE\) with the selected Byte Write select input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the AS5SS512K36 are common I/O devices, data should not be driven into the device while the outputs are active. The output enable (OE\) can be deasserted HIGH before presenting data to the DQ and DP inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DP are automatically three-stated during the data portion of a write cycle, regardless of the state of OE\.

Burst Write Accesses

The AS5SS512K36 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/LD\ must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/LD\ is driven HIGH on the subsequent clock rise, the chip enables (CE1\, CE2, and CE3\) and WE\ inputs are ignored and the burst counter is incremented. The correct BWSa,b,c,d\ / BWSa,b\ inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE\s, ADSP\, and ADSC\ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

CYCLE DESCRIPTION TRUTH TABLE[2,3,4,5,6,7,8]

OPERATION	ADDRESS	CE1\	CE2	CE3\	ZZ	ADV/LD\	WE\	BW\x	OE\	CEN\	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/ Dummy Read (Continue Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (Q)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (Q)
NOP/Write Abort (Continue Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

INTERLEAVED BURST SEQUENCE[2,3,9]

FIRST ADDRESS A[1:0]	SECOND ADDRESS A[1:0]	THIRD ADDRESS A[1:0]	FOURTH ADDRESS A[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST SEQUENCE[2,3,9]

FIRST ADDRESS A[1:0]	SECOND ADDRESS A[1:0]	THIRD ADDRESS A[1:0]	FOURTH ADDRESS A[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

NOTES:

2. X = "Don't Care." H = Logic HIGH, L = Logic LOW. BWX = 0 signifies at least one Byte Write Select is active, BWX = Valid signifies that the desired byte write selects are asserted, see truth table for details.
3. Write is defined by BWX, and WE. See truth table for Read/Write.
4. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
5. The DQs and DQPX pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
6. CEN = H, inserts wait states.
7. Device powers up deselected and the IOs in a tri-state condition, regardless of OE.
8. OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQPX = Tri-state when OE is inactive or when the device is deselected, and DQs and DQPX = data when OE is active.
9. Table only lists a partial listing of the byte write combinations. Any Combination of BWX is valid Appropriate write is based on which byte write is active.

ZZ MODE ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
I_{DDZZ}	Sleep mode stand-by current	ZZ $\geq V_{DD}$ - 0.2V		80	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD}$ - 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2V	$2t_{CYC}$		ns

WRITE CYCLE DESCRIPTION[1]

FUNCTION	WE\	BWSd\	BWSc\	BWSb\	BWSa\
Read	1	X	X	X	X
Write - No Bytes Written	0	1	1	1	1
Write Byte 0 - (DQa and DPa)	0	1	1	1	0
Write Byte 1 - (DQb and DPb)	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 - (DQc and DPc)	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 - (DQb and DPd)	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

NOTES:
1. X = “Don’t Care,” 1 = Logic HIGH, 0 = Logic LOW.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage on V_{DD} Relative to GND .....-0.5V to +3.6V
Storage Temperature.....-65°C to +150°C
Ambient Temperature with Power Applied...-55°C to +125°C
DC Voltage Applied to Outputs
in High Z State[1].....-0.5V to V_{DDQ} +0.5V
DC Input Voltage[1].....-0.5V to V_{DDQ} +0.5V
Current into Outputs (LOW).....20mA
Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)
Latch-Up Current.....>200mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE[2]	V_{DD}	V_{DDQ}
Military (XT)	-55°C to +125°C	3.3V +10%/-5%	2.5 - 5% to V_{DD}
Industrial (IT)	-40°C to +85°C		

ELECTRICAL CHARACTERISTICS (Over the operating range)

PARAMETER	SYM	CONDITIONS		-7.5 MIN	-7.5 MAX	-8.5 MIN	-8.5 MAX	UNIT
Power Supply Voltage	V_{DD}			3.135	3.63	3.135	3.63	V
I/O Supply Voltage	V_{DDQ}			2.375	V_{DD}	2.375	V_{DD}	V
Output HIGH Voltage	V_{OH}	V_{DD} = MIN, I_{OH} = -1.0mA	V_{DDQ} = 2.5V	2.0		2.0		V
		V_{DD} = MIN, I_{OH} = -4.0mA	V_{DDQ} = 2.3V	2.4		2.4		V
Output LOW Voltage	V_{OL}	V_{DD} = MIN, I_{OL} = 1.0mA	V_{DDQ} = 2.5V		0.4		0.4	V
		V_{DD} = MIN, I_{OL} = 8.0mA	V_{DDQ} = 2.3V		0.4		0.4	V
Input HIGH Voltage	V_{IH}		V_{DDQ} = 2.5V	2	V_{DD} + 0.3	2	V_{DD} + 0.3	V
			V_{DDQ} = 2.3V	1.7	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
Input LOW Voltage[1]	V_{IL}		V_{DDQ} = 2.5V	-0.3	0.8	-0.3	0.8	V
			V_{DDQ} = 2.3V	-0.3	0.7	-0.3	0.7	V
Input Load Current	I_X	GND ≤ V_I ≤ V_{DDQ}		-5	5	-5	5	µA
Input Current of MODE				-30	30	-30	30	µA
Output Leakage Current	I_{OZ}	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		-5	5	-5	5	µA
V_{DD} Operating Supply	I_{DD}	V_{DD} = MAX, I_{OUT} = 0mA, f = f_{MAX} = 1/t_{CYC}			210		190	mA
Automatic CE Power-Down Current - TTL Inputs	I_{SB1}	MAX V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}			120		110	mA
Automatic CE Power-Down Current - CMOS Inputs	I_{SB2}	MAX V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} - 0.3V, f = 0			70		70	mA
Automatic CE Power-Down Current - CMOS Inputs	I_{SB3}	MAX V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} - 0.3V, f = f_{MAX} = 1/t_{CYC}			105		90	mA
Automatic CE Power-Down Current - TTL Inputs	I_{SB4}	MAX V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = 0			80		80	mA

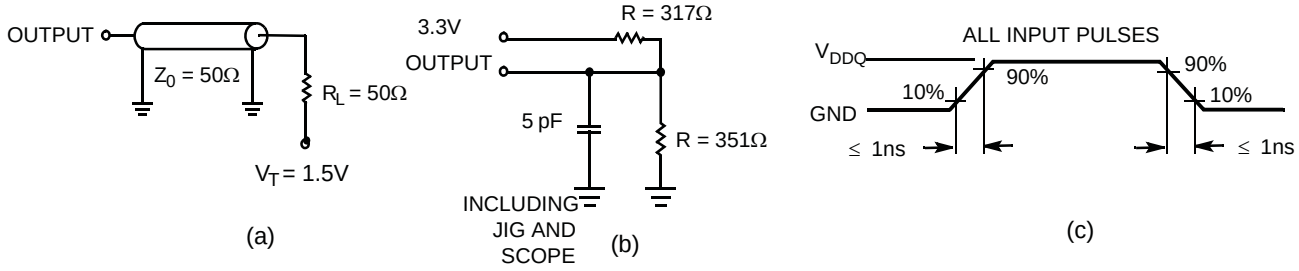
NOTES:
1. Minimum voltage equals .2.0V for pulse durations of less than 20 ns.
2. T_A is the case temperature.
3. The load used for V_{OH} and V_{OL} testing is shown in figure (b) of the AC Test Loads.

CAPACITANCE[1]

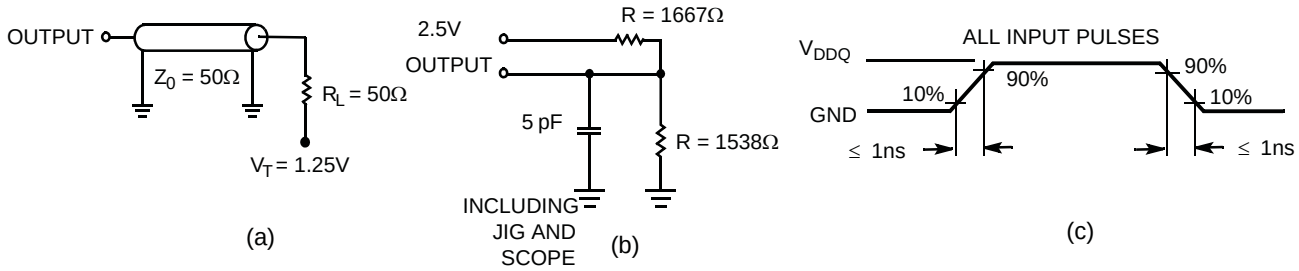
PARAMETER	SYM	TEST CONDITION	MAX	UNIT
Input Capacitance	C_{IN}	T_A = 25°C, f = 1MHz	5	pF
Clock Input Capacitance	C_{CLK}		5	pF
Input/Output Capacitance	$C_{I/O}$		5	pF

AC TEST LOADS & WAVEFORMS

3.3V IO Test Load



2.5V IO Test Load



THERMAL RESISTANCE[1]

PARAMETER	CONDITIONS	SYM	MAX	UNIT
Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 x 4.5 inch sq., 2 layer printed circuit board.	θ_{JA}	28.66	°C/W
Thermal Resistance (Junction to Case)		θ_{JC}	4.08	°C/W

NOTES:

1. Tested initially and after any design or process change that may affect these parameters.
2. Input waveform should have a slew rate of < 1 V/ns.

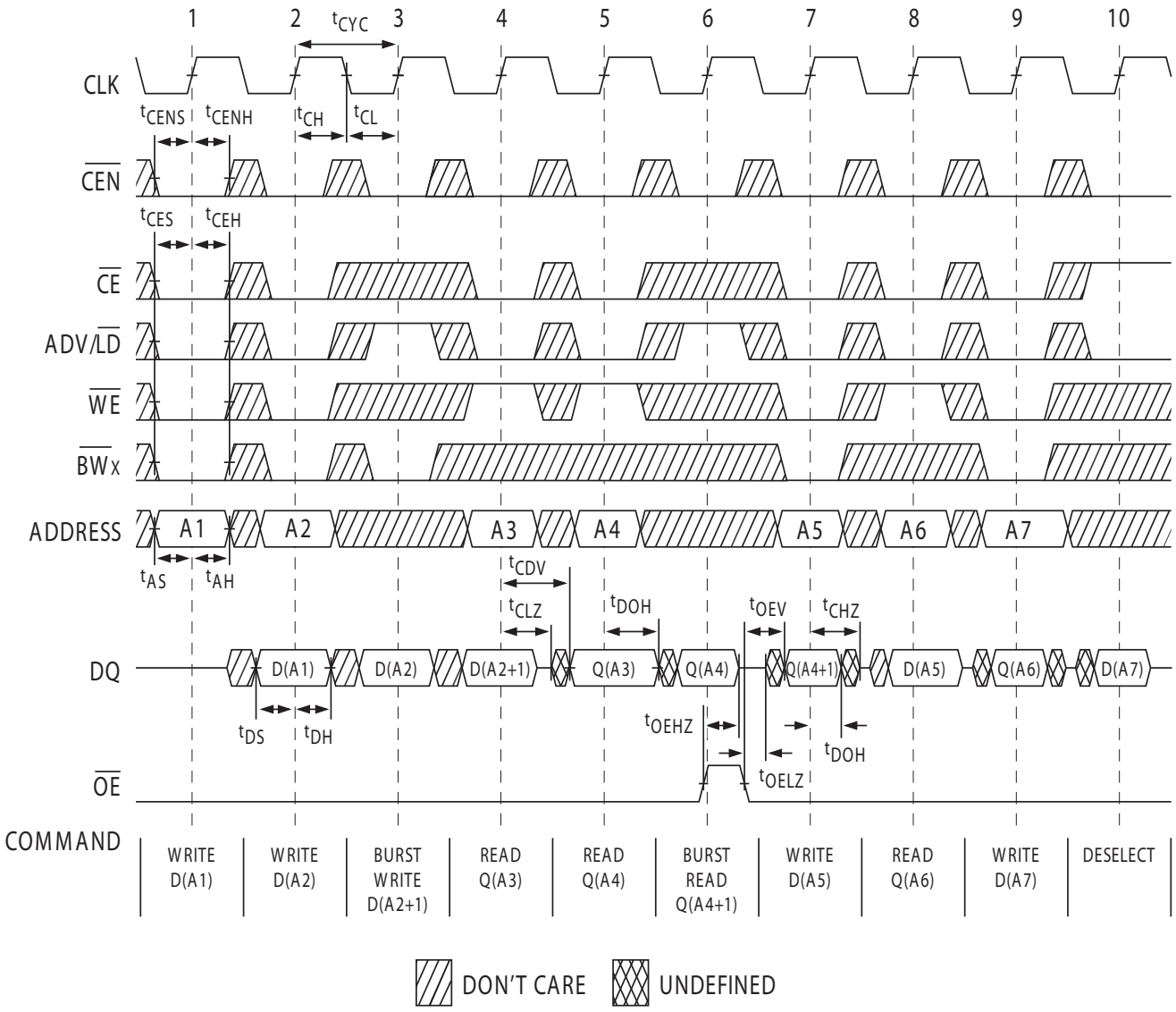
SWITCHING CHARACTERISTICS (Over the Operating Range)[2]

		-7.5		-8.5		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS
CLOCK						
Clock Cycle Time	t_{CYC}	7.5		10		ns
Clock HIGH	t_{CH}	2.1		2.5		ns
Clock LOW	t_{CL}	2.1		2.5		ns
OUTPUT TIMES						
Data Output Valid After CLK Rise	t_{CDV}		6.5		8.5	ns
OE\ LOW to Output Valid[1, 3, 5]	t_{OEV}		3.2		3.8	ns
Data Output Hold After CLK Rise	t_{DOH}	2.0		2.0		ns
Clock to High-Z[1-5]	t_{CHZ}		4.0		5.0	ns
Clock to Low-Z[1-5]	t_{CLZ}	2.0		2.0		ns
OE\ HIGH to Output High-Z[2, 3, 5]	t_{EOHZ}		4.0		5.0	ns
OE\ LOW to Output Low-Z[2, 3, 5]	t_{EOLZ}	0		0		ns
SET-UP TIMES						
Address Set-up Before CLK Rise	t_{AS}	1.5		1.5		ns
Data Input Set-up Before CLK Rise	t_{DS}	1.5		1.5		ns
CEN\ Set-up Before CLK Rise	t_{CENS}	1.5		1.5		ns
WE\, BWSx\ Set-up Before CLK Rise	t_{WES}	1.5		1.5		ns
ADV/LD\ Set-up Before CLK Rise	t_{ALS}	1.5		1.5		ns
Chip Select Set-up	t_{CES}	1.5		1.5		ns
HOLD TIMES						
Address Hold After CLK Rise	t_{AH}	0.5		0.5		ns
Data Input Hold After CLK Rise	t_{DH}	0.5		0.5		ns
CEN\ Hold After CLK Rise	t_{CENH}	0.5		0.5		ns
WE\, BWSx\ Hold After CLK Rise	t_{WEH}	0.5		0.5		ns
ADV/LD\ Hold After CLK Rise	t_{ALH}	0.5		0.5		ns
Chip Select Hold After CLK Rise	t_{CEH}	0.5		0.5		ns

NOTES:

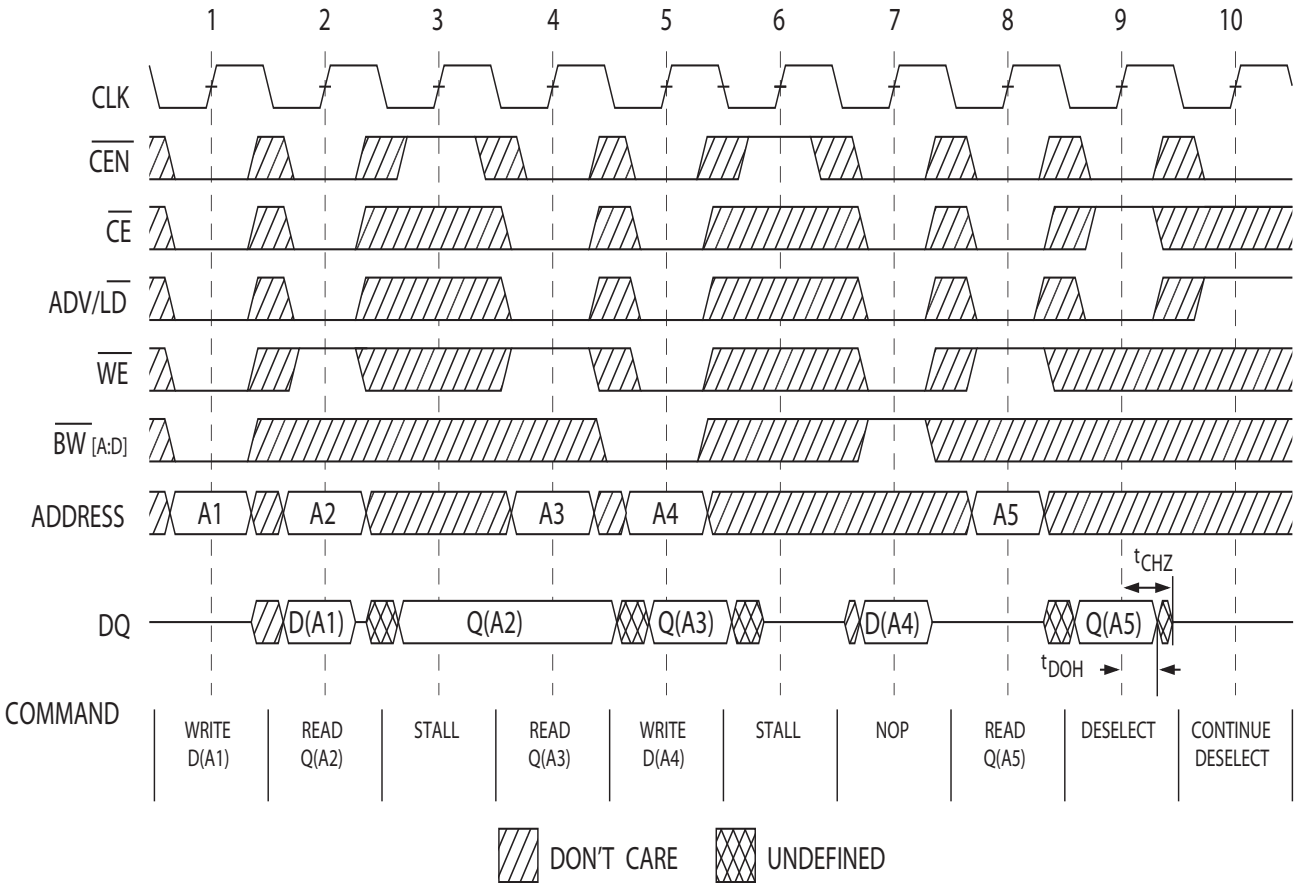
1. Tested initially and after any design or process change that may affect these parameters.
2. Unless otherwise noted, test conditions assume signal transition time of 1ns or less, timing reference levels of 1.5/1.25V, input pulse levels of 0 to 3.0/2.5V for 3.3/2.5V VDDQ respectively, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a), (b) and (c) of AC Test Loads.
3. t_{CHZ}, t_{CLZ}, t_{EOV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
4. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
5. This parameter is sampled and not 100% tested.

SWITCHING WAVEFORMS: READ/WRITE WAVEFORMS [25, 26, 27]



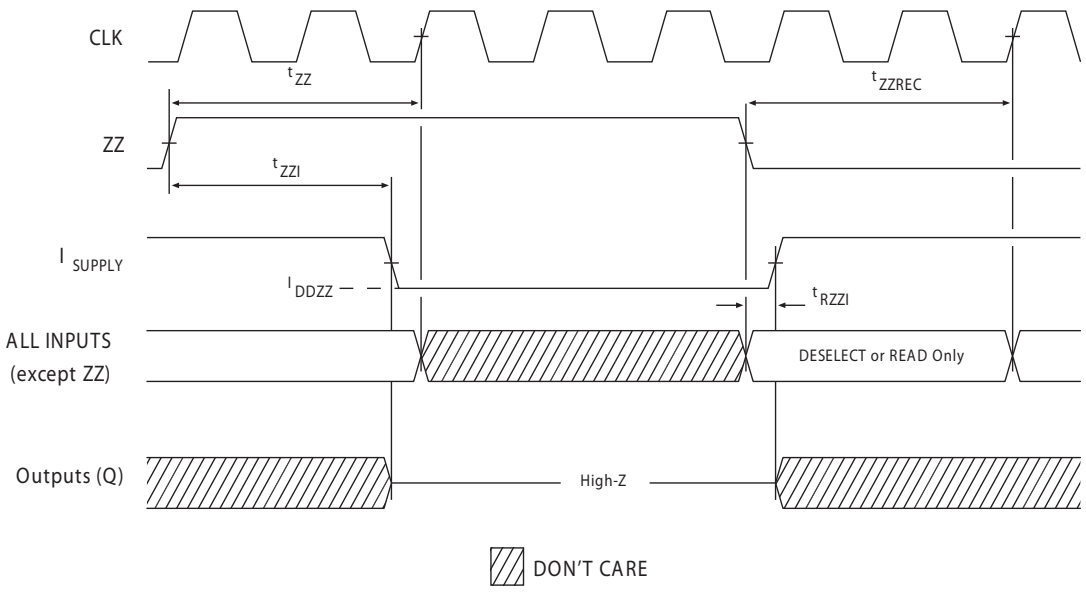
Notes:
25. For this waveform ZZ is tied LOW.
26. When CE is LOW, CE_1 is LOW, CE_2 is HIGH and CE_3 is LOW. When CE is HIGH, CE_1 is HIGH or CE_2 is LOW or CE_3 is HIGH.
27. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

SWITCHING WAVEFORMS: NOP, STALL & DESELECT CYCLES[25, 26, 28]



Note:
28. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates CEN being used to create a pause. A write is not performed during this cycle.

SWITCHING WAVEFORMS: ZZ MODE TIMING [29, 30]

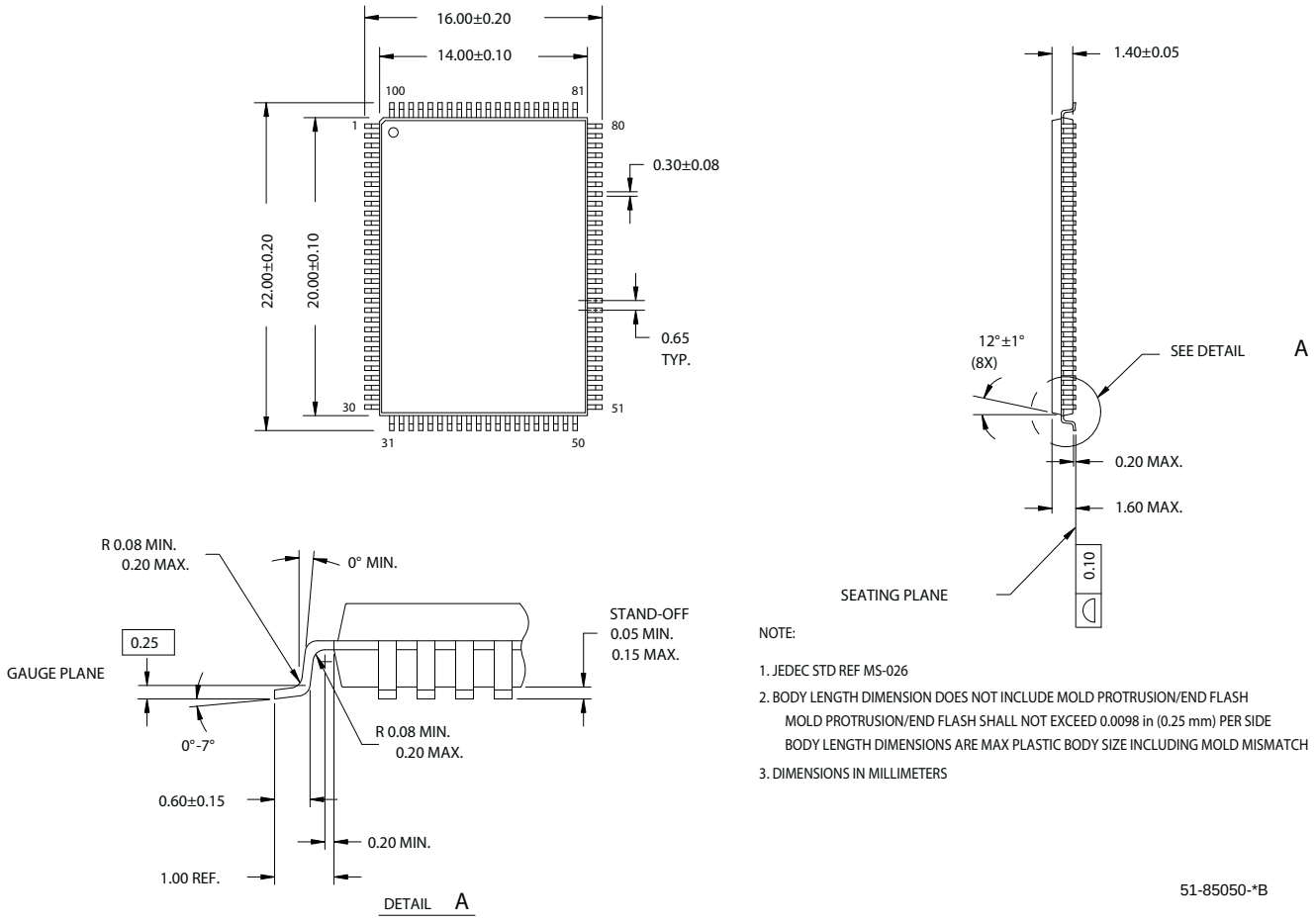


Notes:
29.Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
30.DQs are in high-Z when exiting ZZ sleep mode.

All measurements are in inches.

MECHANICAL DEFINITIONS*

Micross 100-PIN TQFP (Package Designator DQ)



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

NOTES: * Dimensions are in millimeters.

ORDERING INFORMATION

EXAMPLE: AS5SS512K36DDQ-7.5/IT

Device Number	Package Type	Speed ns	Process
AS5SS512K36D	DQ	-7.5	/IT[1]
AS5SS512K36D	DQ	-8.5	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C

NOTES: 1. The -7.5 option is available with IT processing only.

DOCUMENT TITLE

512K x 36 SSRAM

REVISION HISTORY

Rev #	History	Release Date	Status
0.2	Updated Speeds, pg 1&2	April 2009	Release
0.5	Updated to Rev D	June 2009	Release
0.5	Updated Micross Information	January 2010	Release