



## Datasheet

DS000667

# AS7421

## 64-Channel Hyperspectral NIR Sensor

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# Content Guide

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# 1 General Description

AS7421 is a 64-channel near infrared digital spectrometer for spectral identification and spectral footprint analysis used in consumer devices. The spectral response of the sensor is defined in the wavelengths from approximately 750 nm to 1050 nm and the channels are equally distributed over the mentioned range. Once a spectral measurement is started, all 64 channels are processed automatically by 16 parallel sampling ADCs with four consecutive integration cycles.

AS7421 integrates Fabry-Perot filters into standard CMOS silicon via nano-optic deposited interference filter technology and its package provides a built in aperture and micro optics to control the light entering the sensor array. In addition, the module provides a near infrared (NIR) light source and an integrated LED driver to control it.

Control and spectral data access is implemented through a serial I<sup>2</sup>C interface. A GPIO and an interrupt signal are available to start/synchronize the spectral measurement as well as minimize I<sup>2</sup>C traffic.

## 1.1 Key Benefits & Features

The benefits and features of AS7421, 64-Channel Hyperspectral NIR Sensor, are listed below:

**Figure 1:**  
**Added Value of Using AS7421**

Benefits	Features
Miniaturized reflectance/absorbance spectral analysis and material identification in NIR range	61 individual and 4 special purpose spectral channels with a FWHM of typical 10 nm 16-bit full scale resolution per spectral channel
Fast measurement time	16 parallel sampling ADCs with individual gain settings 256 ms to obtain measurement data for all 64 channels
High module integration and low BOM	Integrated 64-channel sensor with on-chip Fabry-Perot filters Integrated NIR light source (LED) to cover 750 - 1050 nm range Integrated programmable LED driver Integrated optics to limit AOI on sensor
Low power consumption and minimum I <sup>2</sup> C traffic	3.3 V VDD operation Configurable sleep mode Interrupt-driven device
Synchronization of spectral measurement	Configurable GPIO to trigger/sync spectral measurements

Benefits	Features
Full calibration support package available for sensor integration	Calibration library support which includes data post-processing of spectral raw data Data output options: raw data, absorbance spectra, 1 <sup>st</sup> derivative of absorbance spectra, 2 <sup>nd</sup> derivative of absorbance spectra

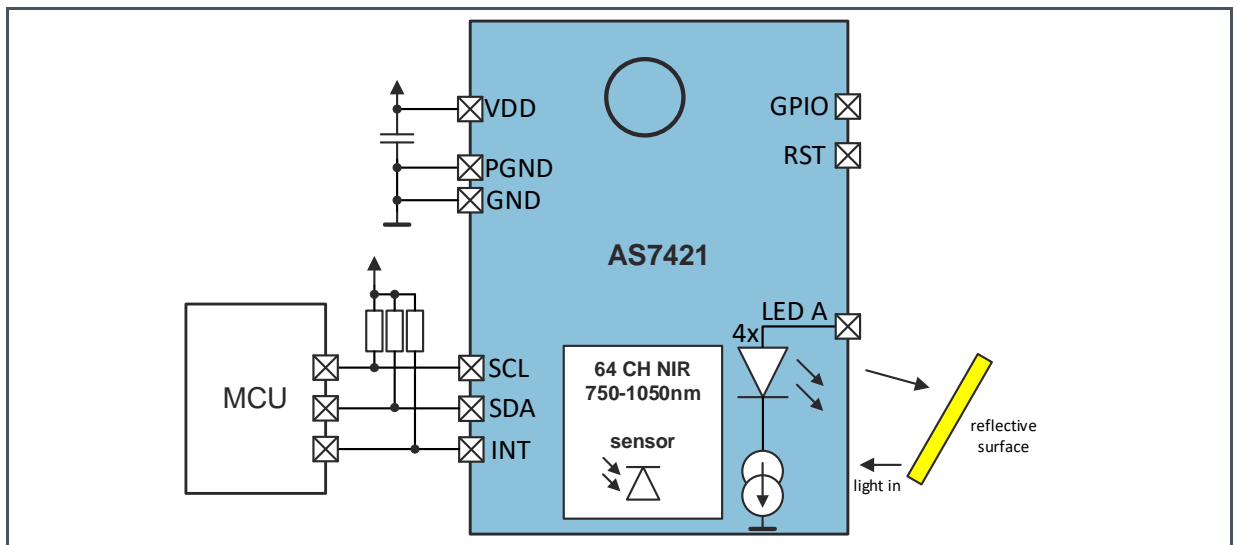
## 1.2 Applications

- Spectral material identification of goods and fabrics
- Moisture measurements in industrial or agricultural environments
- Brix and dry matter measurements of fruits (fruit ripeness)

## 1.3 Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**  
Functional Blocks of AS7421



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## 2 Ordering Information

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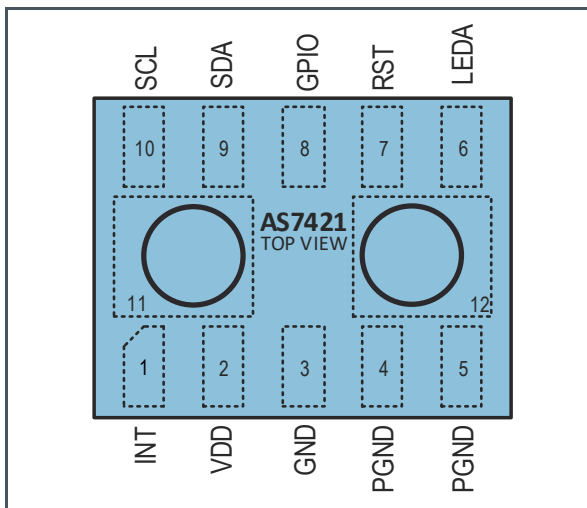
Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS7421-ZLGT	OLGA-10	AS7421	Tape & Reel	2000 pcs/reel

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## 3 Pin Assignment

### 3.1 Pin Diagram

Figure 3:  
Pin Assignment of AS7421 (TOP VIEW)



### 3.2 Pin Description

Figure 4:  
Pin Description of AS7421

Pin Number	Pin Name	Pin Type <sup>(1)</sup>	Description
1	INT	DO_OD	Interrupt. Open drain output. Connect pull up resistor to 1.8 V or 3.3 V. Active low.
2	VDD	P	Positive supply terminal.
3	GND	P	Ground. All voltages referenced to GND.
4	PGND	P	Ground. All voltages referenced to GND.
5	PGND	A_I	Ground. All voltages referenced to GND.
6	LED A	A_I	Supply voltage for NIR LEDs anode.
7	RST	DI	Reset input with internal pull down resistor. Active high.
8	GPIO	D_I/O	General purpose input/output.

Pin Number	Pin Name	Pin Type <sup>(1)</sup>	Description
9	SDA	D_I/O	Serial Interface data signal line for I <sup>2</sup> C interface. Connect pull up resistor to 1.8 V or 3.3 V.
10	SCL	DI	Serial Interface clock signal line for I <sup>2</sup> C interface. Connect pull up resistor to 1.8 V or 3.3 V.
11	GND	P	Exposed pad, connect to GND with thermal vias.
12	LED A	A_I	Exposed pad, connect to LED A.

- (1) Explanation of abbreviations:
- DI Digital Input
  - D\_I/O Digital Input/Output
  - DO\_OD Digital Output, open drain
  - P Power pin
  - A\_I Analog input

## 4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Electrical Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5**  
**Absolute Maximum Ratings of AS7421**

Symbol	Parameter	Min	Max	Unit	Comments
<b>Electrical Parameters</b>					
$V_{DD} / V_{GND}$	Supply voltage to ground	-0.3	3.6	V	Applicable for pin VDD
$V_{LEDA}$	LEDA voltage to ground	-0.3	3.6	V	Applicable for pin LEDA
$V_{DIG\_MAX}$	Digital pins	-0.3	VDD+0.3	V	Applicable for pins SCL, SDA and INT
$I_{SCR}$	Input current (latch-up immunity)	± 100		mA	JESD78E
<b>Continuous Power Dissipation (<math>T_A = 70\text{ °C}</math>)</b>					
$P_T$	Continuous power dissipation	1.4		W	Including LEDs and sensor
<b>Electrostatic Discharge</b>					
$ESD_{HBM}$	Electrostatic discharge HBM	± 2000		V	JS-001-2017
$ESD_{CDM}$	Electrostatic discharge CDM	± 500		V	JS-002-2014
<b>Temperature Ranges and Storage Conditions</b>					
$T_A$	Ambient temperature	-30	+85	°C	
$R_{THJA}$	Junction to ambient thermal resistance	85		K/W	Depending on actual PCB layout. <sup>(2)</sup>
$T_{STRG}$	Storage temperature range	-40	+85	°C	
$T_{BODY}$	Package body temperature	260		°C	IPC/JEDEC J-STD-020 <sup>(1)</sup>
$R_{HNC}$	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Maximum floor life time of 168h

- (1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).
- (2) Value defined for PCB using 5x5mm copper area on bottom side of PCB. Thermal vias used to connect exposed pad from TOP layer with bottom layer. Contact ams OSRAM for guidelines on thermal management.



## 5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at  $V_{DD}=3.3\text{ V}$  and  $T_A=25\text{ °C}$  unless otherwise noted.

**Figure 6:**  
Electrical Characteristics of AS7421

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply voltage		3	3.3	3.6	V
$V_{LEDA}$	LED supply voltage	$I_{LED} = 75\text{ mA}$		2.8	3.0 <sup>(1)</sup>	V
$f_{OSC}$	Oscillator frequency			8		MHz
$T_A$	Operating free-air temperature		-30	25	60	°C
$T_J$	Operating junction temperature		-30	25	65	°C
$T_{OVTEMP}$	Overtemperature shutdown			150	165	°C
<b>Power Consumption</b>						
$I_{DD}$	Supply current	$V_{DD} = 3.3\text{ V}; T_A = 25\text{ °C}$ Active mode <sup>(2)</sup>		2.5	5	mA
		$V_{DD} = 3.3\text{ V}; T_A = 25\text{ °C}$ Idle mode <sup>(3)</sup>		400		µA
		$V_{DD} = 3.3\text{ V}; T_A = 25\text{ °C}$ Sleep mode <sup>(4)</sup>		2	4	µA
<b>Digital Pins</b>						
$V_{IH}$	SCL, SDA input high voltage		1.26			V
$V_{IL}$	SCL, SDA input low voltage				0.54	V
$V_{OL}$	INT, SDA output low voltage	6 mA sink current			0.4	V
$C_i$	Input pin capacitance				10	pF
$I_{leak}$	Leakage current into SCL, SDA, INT, GPIO pins				1.5	µA
<b>LED Driver</b>						
$I_{LED\_ACCURACY}$	Absolute ILED accuracy	$I_{LED} = 50\text{ mA}$ $T_A = 25\text{ °C}$	-30		+30	%
$V_{COMP}$	Compliance voltage of current sink	$I_{LED} = 75\text{ mA}$			500	mV
<b>LED</b>						
$V_{f\_LED1}$	Forward voltage	$I_F = 25\text{ mA}$		2.0		V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{f\_LED2}$	Forward voltage	$I_F = 25 \text{ mA}$		1.6		V
$V_{f\_LED3}$	Forward voltage	$I_F = 25 \text{ mA}$		1.25		V
$V_{f\_LED4}$	Forward voltage	$I_F = 25 \text{ mA}$		1.25		V
$\lambda_{p\_LED1}$	Peak wavelength	$I_F = 25 \text{ mA}$		760		nm
$\lambda_{p\_LED2}$	Peak wavelength	$I_F = 25 \text{ mA}$		830		nm
$\lambda_{p\_LED3}$	Peak wavelength	$I_F = 25 \text{ mA}$		950		nm
$\lambda_{p\_LED4}$	Peak wavelength	$I_F = 25 \text{ mA}$		1040		nm

- (1) VDD must be applied before VLEDA during power on. VLEDA must always be smaller or equal than  $VDD+0.3 \text{ V}$ .
- (2) Active state occurs during ongoing spectral measurement  $AEN = "1"$  and power consumption defined without LED current.
- (3) Idle state occurs when  $PON = "1"$  and all functions are disabled.
- (4) Sleep state occurs when  $PON = "0"$  and no active I<sup>2</sup>C communication.

**Figure 7:**  
**Optical Characteristics of AS7421, Integration Time = 65.5 ms (unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FWHM	Full width half maximum of filter <sup>(8)</sup>			10		nm
$\lambda_s$	Peak Wavelength Separation			5		nm
dark	Dark ADC count value	Ee = 0 $\mu\text{W}/\text{cm}^2$ AGAIN: 128x Integration time: 65.5 ms			5	counts
Gain ratio	Optical gain ratios, relative to 1x gain setting	AGAIN: 1x		1		
		AGAIN: 2x		2		
		AGAIN: 4x		4		
		AGAIN: 8x		8		
		AGAIN: 16x		16		
		AGAIN: 32x		32		
		AGAIN: 64x		64		
		AGAIN: 128x		128		
AGAIN: 256x		256				
SNR <sub>SYSTEM</sub>	Signal to noise ratio of optical system <sup>(1)(2)</sup>	Range: 750 nm – 1050 nm	500			
ImSR	Intra-module spectral repeatability <sup>(1)(3)</sup>	Range: 750 nm – 1050 nm			0.5	%
IMSR	Inter-module spectral repeatability <sup>(1)(4)</sup>	Range: 750 nm – 1050 nm			5	%
W <sub>acc</sub>	Wavelength accuracy <sup>(1)(7)</sup>				5	nm
t <sub>int</sub>	Integration time <sup>(5)</sup>		0.5	65.5	256	ms
t <sub>64CH</sub>	Measurement time for all 64 channel <sup>(6)</sup>			4 x t <sub>int</sub>		ms
f	Field of view of single photo diode		-10		10	deg

- (1) Parameter not tested in final test but guaranteed by design and validation.
- (2) Verified with raw spectral data collected with reflectance standard sample (RSS) with reflectance of 99% (white diffusive target). Average and standard deviation is calculated for each channel ( $\lambda_{CH}$ ) for 10 measurements.  $\text{SNR}_{\text{SYSTEM}} = \mu(\lambda_{CH}) / \sigma(\lambda_{CH})$ .
- (3) Verified with raw spectral data collected with reflectance standard sample (RSS, 10 measurements per channel) with reflectance of 99% (white diffusive target) and wavelength calibration standard zenith polymer (WCS, 100 measurements per channel).
- (4) Verified with raw spectral data collected with reflectance standard sample (RSS, 10 measurements per channel for 10 devices) with reflectance of 99% (white diffusive target) and wavelength calibration standard zenith polymer (WCS, 100 measurements per channel for 10 devices).
- (5) 65.5 ms integration time to achieve 16-bit count value (depending on amount of light reflected to sensor)
- (6) 4 integration cycles are done automatically to process all 64 channels.
- (7) Verified after full sensor calibration. Raw spectral data recorded for each channel with wavelength calibration standard zenith polymer (WCS, 10 measurements per channel).
- (8) Parameter verified with collimated light at 0° AOI (angle of incidence).

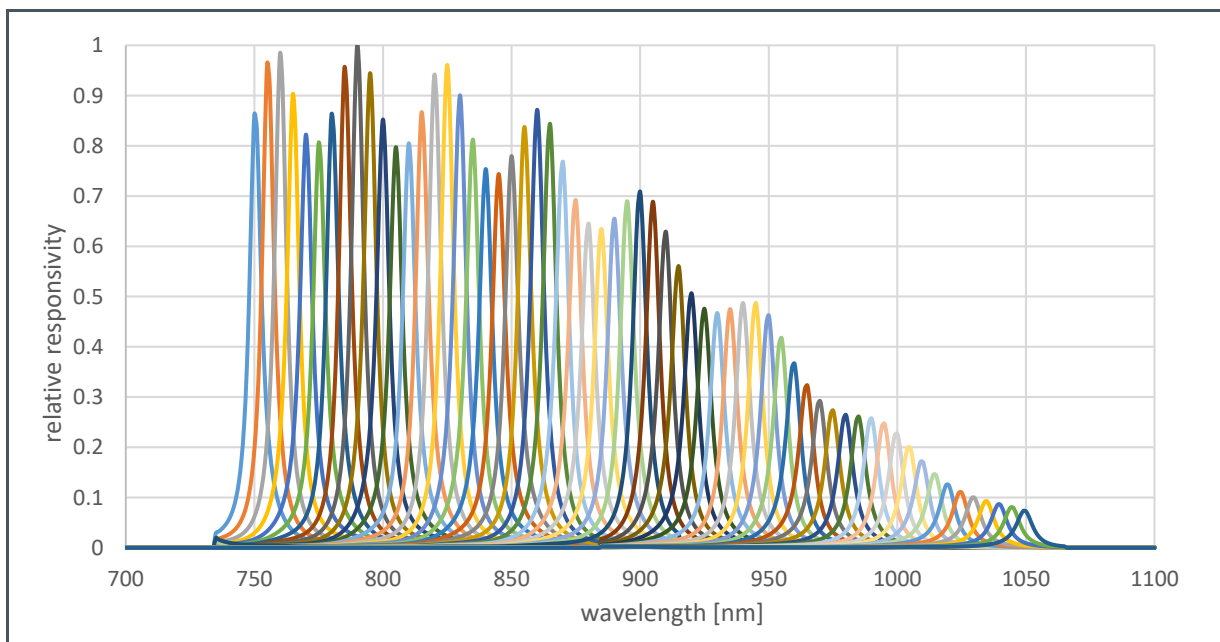
**Figure 8:**  
**Typical Irradiance Responsivity of AS7421, Integration Time = 65.5 ms (unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>e_PD0</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 830 nm		406		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD1</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 750 nm		431		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD2</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 790 nm		409		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD3</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 870 nm		296		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD4</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 940 nm		190		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD5</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 980 nm		112		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD6</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1020 nm		105		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD7</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 830 nm		385		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD8</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 760 nm		394		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD9</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 800 nm		422		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD10</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 840 nm		385		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD11</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 880 nm		344		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD12</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 930 nm		235		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD13</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 970 nm		151		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD14</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1010 nm		148		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD15</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1050 nm		61		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD16</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 770 nm		398		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD17</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 810 nm		416		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD18</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 850 nm		390		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD19</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 890 nm		367		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD20</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 920 nm		253		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD21</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 960 nm		166		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD22</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1000 nm		180		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD23</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1040 nm		74		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD24</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 780 nm		398		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD25</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 820 nm		411		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD26</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 860 nm		405		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD27</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 900 nm		363		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD28</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 910 nm		286		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD29</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 950 nm		189		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD30</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 990 nm		206		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD31</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1030 nm		92		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD32</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 775 nm		401		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD33</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 815 nm		430		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD34</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 855 nm		401		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD35</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 895 nm		370		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD36</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 905 nm		304		counts / (μW/cm <sup>2</sup> )
R <sub>e_PD37</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 945 nm		209		counts / (μW/cm <sup>2</sup> )

R <sub>e_PD38</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 985 nm	225	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD39</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1025 nm	104	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD40</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 765 nm	397	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD41</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 805 nm	418	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD42</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 845 nm	371	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD43</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 885 nm	354	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD44</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 915 nm	269	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD45</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 955 nm	177	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD46</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 995 nm	203	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD47</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1035 nm	90	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD48</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 755 nm	375	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD49</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 795 nm	401	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD50</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 835 nm	387	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD51</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 875 nm	320	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD52</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 926 nm	239	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD53</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 965 nm	163	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD54</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1005 nm	169	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD55</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1045 nm	74	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD56</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 830 nm	403	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD57</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 785 nm	413	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD58</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 825 nm	327	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD59</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 865 nm	214	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD60</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 935 nm	214	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD61</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 975 nm	143	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD62</sub>	Irradiance responsivity	AGAIN: 128x; λ <sub>p</sub> : 1015 nm	134	counts / (μW/cm <sup>2</sup> )
R <sub>e_PD63</sub>	Irradiance responsivity	AGAIN: 64x; λ <sub>p</sub> : 830 nm	426	counts / (μW/cm <sup>2</sup> )

## 6 Typical Operating Characteristics

**Figure 9:**  
Typical Spectral Responsivity of Sensor



**Figure 10:**  
Typical LED Spectral Emission at 50 mA LED Current

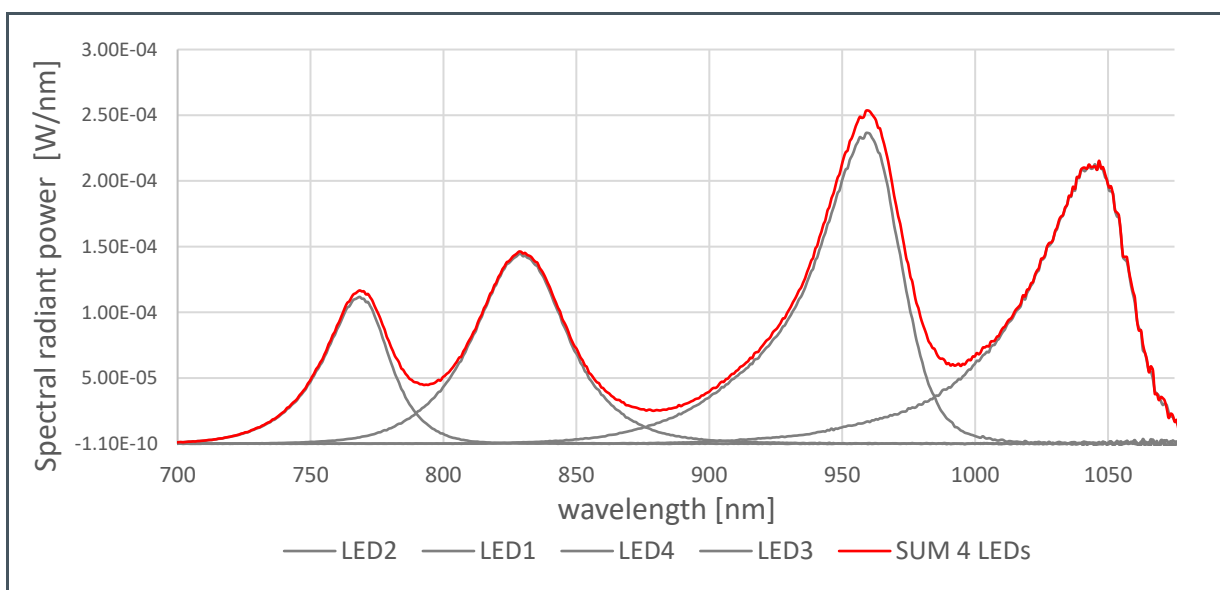
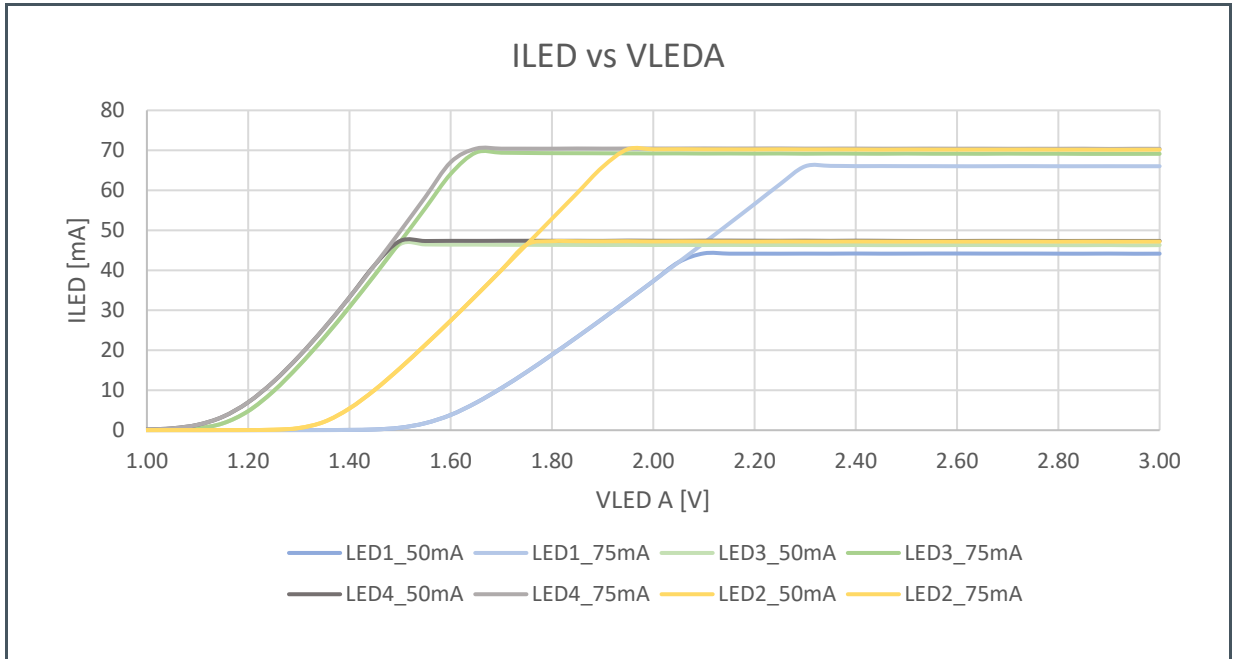


Figure 11:  
Typical LED Forward Voltage vs. LED Current

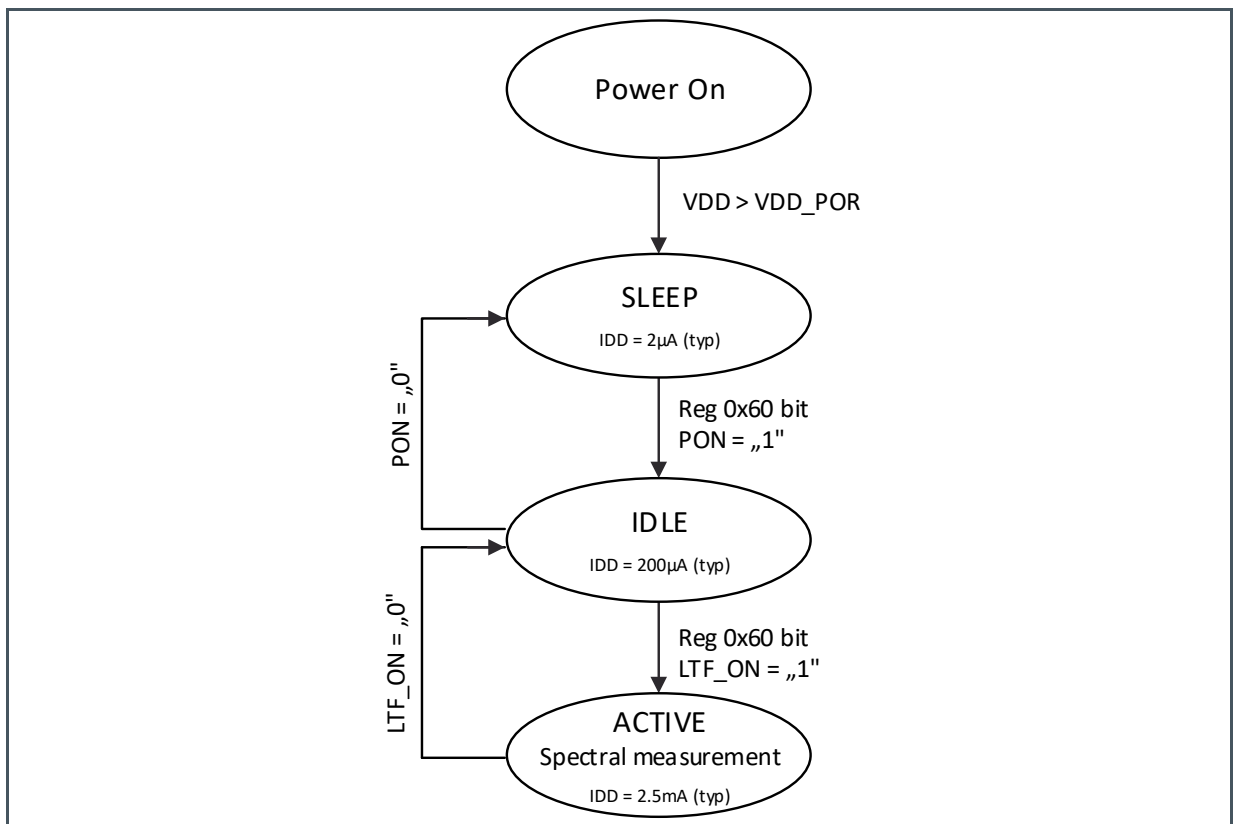


# 7 Functional Description

Upon power-up (POR), the device initializes. It is required that VDD is applied and settled 10 ms before the supply voltage of the NIR light source is applied (VLED\_A). During power down VLED\_A needs to be turned off 10 ms prior VDD.

During initialization, the device cannot accept I<sup>2</sup>C transactions. All communication with the device must be delayed and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state, the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I<sup>2</sup>C transaction occurs during this state, the I<sup>2</sup>C core wakes up temporarily to service the communication. Once the Power ON bit, "PON", is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever the spectral measurement is enabled (LTF\_ON = "1") the device enters the ACTIVE state. If the spectral measurement is disabled (LTF\_ON = "0") the device returns to the IDLE state. The figure below describes a simplified state diagram and the typical supply currents in each state. The power consumption in ACTIVE state does not include the power consumption to drive the NIR LEDs.

**Figure 12:**  
Start Up Flow-Chart



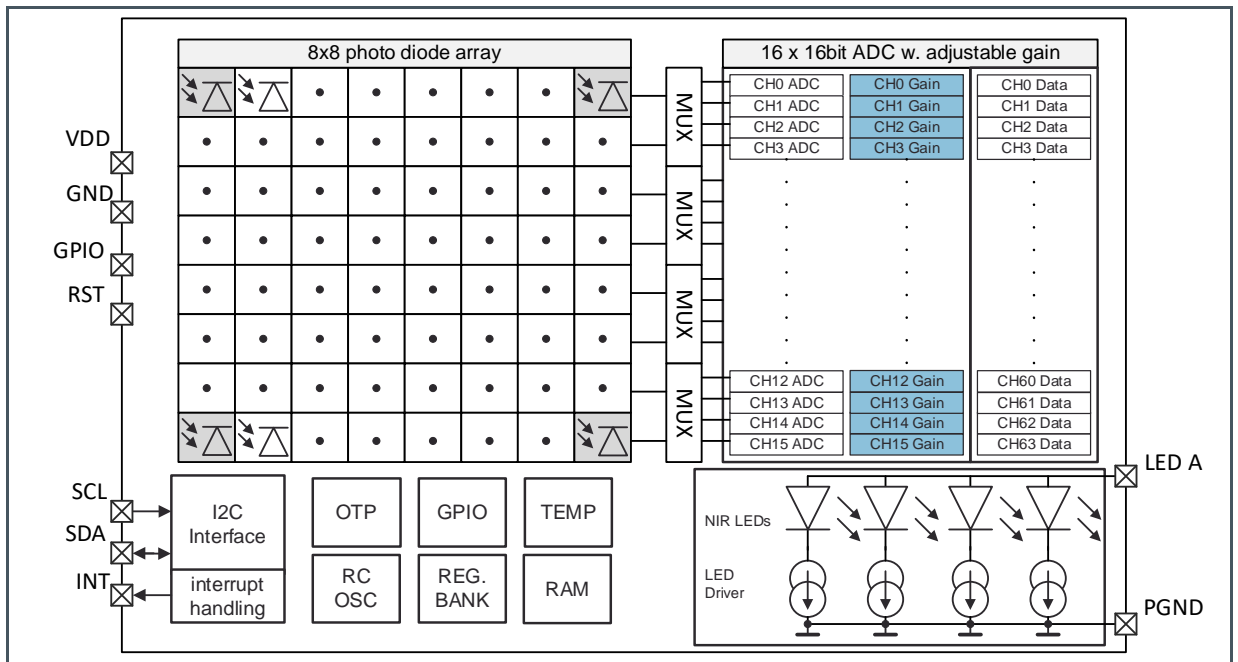


## 7.1 Device Architecture

The device features 64 photo diodes (8 x 8 array) with on-chip Fabry-Perot filters. 61 photodiodes have an individual spectral response in the wavelength range from 750 nm - 1050 nm. The four corner photodiodes (indicated in the block diagram below with grey shading) share the same filter response of 830 nm. Sixteen dedicated 16-bit ADCs with adjustable gain and integration time are available and can be configured with the serial interface. The gain of each ADC can be adjusted independently. Once a spectral measurement is started, the device automatically runs four full integration cycles to obtain spectral data of all 64 channels. The spectral data (128 bytes) is stored on chip and can be read out using the I<sup>2</sup>C interface burst mode after the four cycles have been finished.

The GPIO can be used to trigger and synchronize a spectral measurement with an external MCU or as additional interrupt output. The pin RST acts as reset input and is active high.

**Figure 13:**  
**Simplified Block Diagram of AS7421**



## 7.2 Sensor Array

The device features an 8 x 8-photodiode array – each photo diode has its own filter with a dedicated response. The pitch between each photo-diode is 200 μm. Four photodiodes (corner) share the same wavelength response.

**Figure 14:**  
**Photodiode Array**

	1600μm							
1600μm	830 nm	750	790	870	940	980	1020	830 nm
	760	800	840	880	930	970	1010	1050
	770	810	850	890	920	960	1000	1040
	780	820	860	900	910	950	990	1030
	775	815	855	895	905	945	985	1025
	765	805	845	885	915	955	995	1035
	755	795	835	875	925	965	1005	1045
	830 nm	785	825	865	935	975	1015	830 nm

## 7.3 SMUX Configuration

The device integrates a multiplexer (SMUX). With the SMUX, it is possible to map all available photo diodes to one of four pre-defined ADCs. In total sixteen ADCs are available for data processing. After power up of the device the SMUX needs to be configured and the configuration data is stored in the RAM. ams OSRAM provides reference codes and an application note on how to configure the SMUX.

## 7.4 ADC Gain Configuration

The gain of each modulator (ADC) can be adjusted individually. Eight configuration steps are available, from AGAIN “0” (gain factor 1x) to AGAIN “8” which equals a gain ration of 256x. ams OSRAM provides reference codes and an application note on how to configure the AGAIN values of AS7421.

## 7.5 Typical Measurement Cycle

Figure 15:  
Measurement Cycle with LED\_WAIT\_OFF = "1"

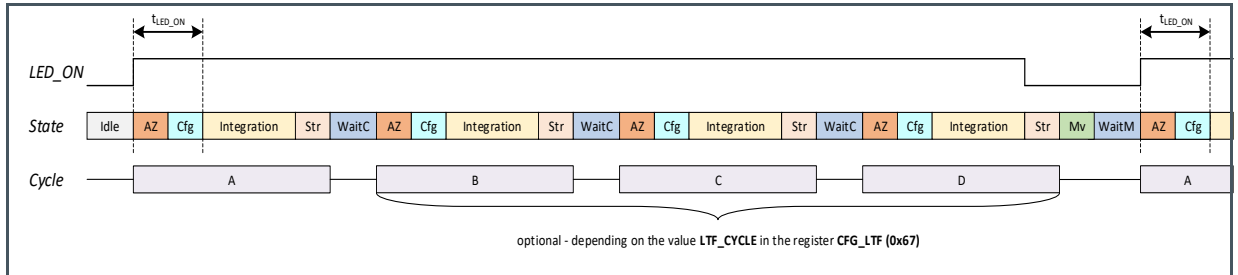


Figure 16:  
Measurement Cycle with LED\_WAIT\_OFF = "0"

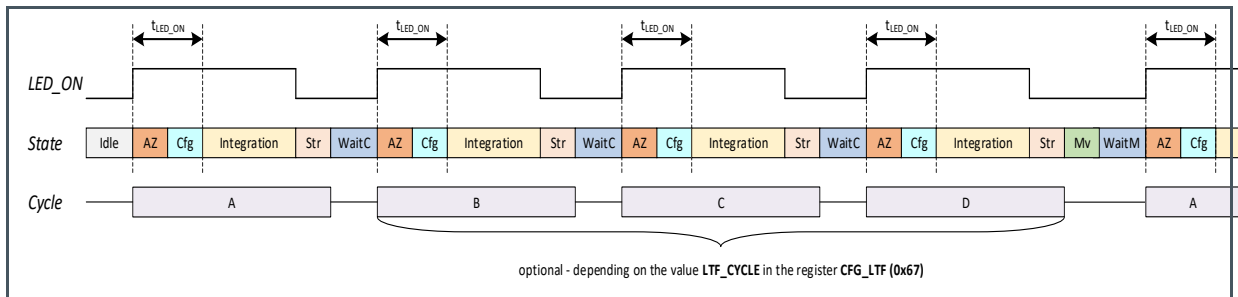


Figure 17:  
Measurement State Explanation

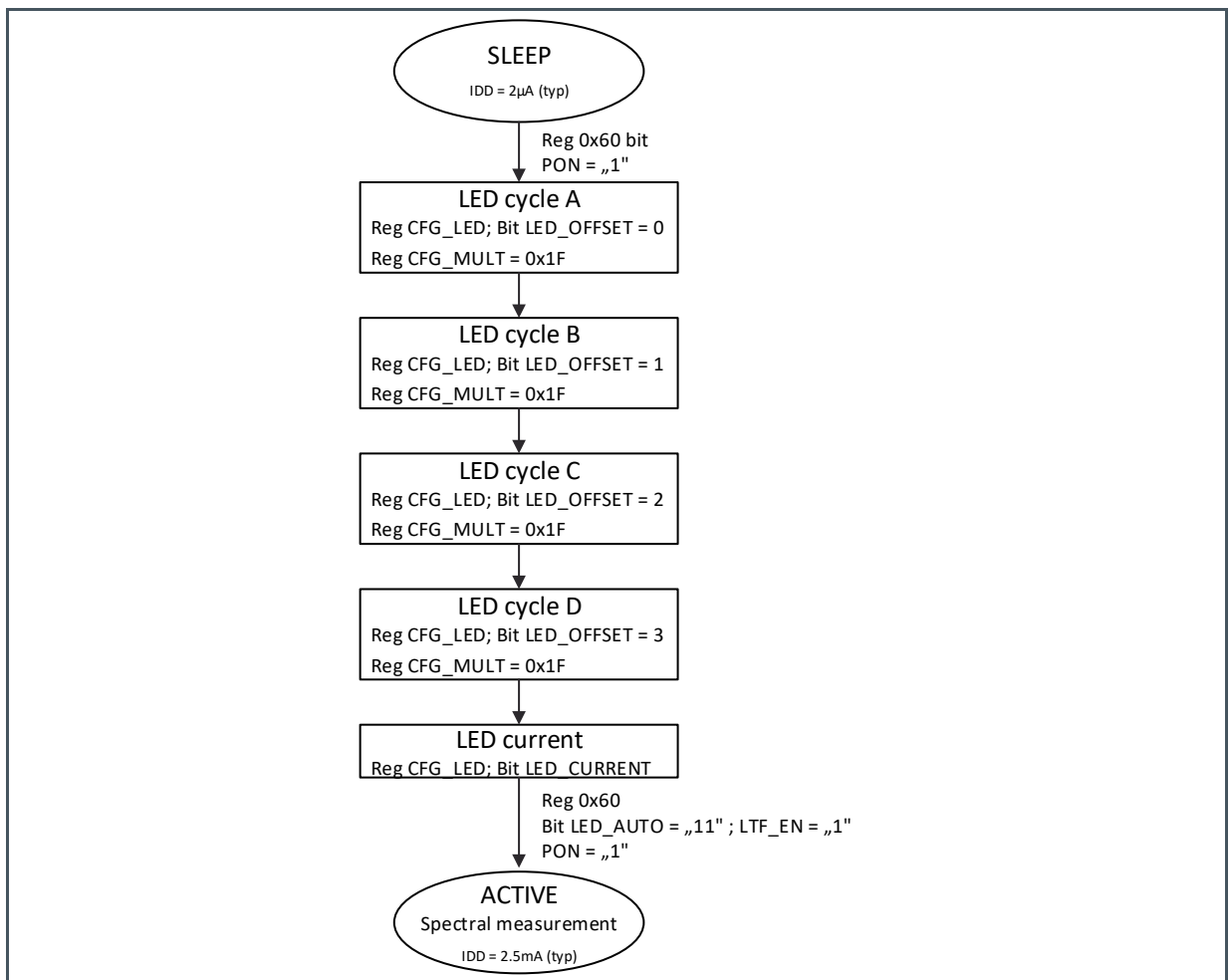
<b>AZ</b>	AutoZero ...	Offset compensation of ADCs
<b>Cfg</b>	Configuration ...	Set the ASETUP and SMUX values for the integration cycle
<b>Integration</b>	Integration cycle	Programmable with register <b>LTF_ITIME (0x61 – 0x63)</b>
<b>Str</b>	Store ...	Store the 16 x 16bit ADC data in the internal RAM
<b>Mv</b>	Move ...	Provision of a new memory area in the internal RAM for the next measurement
<b>WaitC</b>	Wait Cycle ...	Waiting time between integration cycles within a measurement (can optionally be switched on or off) Programmable with registers <b>LTF_WTIME (0x64 – 0x67)</b>
<b>WaitM</b>	Wait Measurement ...	Waiting time between the provision of a new memory area and the automatic start of the next measurement Programmable with registers <b>LTF_WTIME (0x64 – 0x67)</b>

## 7.6 LED Driver

Four current sinks are provided to drive the 4 integrated NIR LEDs with a programmable constant current of 50 mA or 75 mA per channel. If a measurement is done with 4 x 75 mA ILED the next measurement can be started after a timeout of 10 seconds.

The LED driver can be configured with the register CFG\_LED. With the bits “LED\_AUTO” in register 0x60 it is possible that the LED driver is configured in such a way that during two consecutive spectral measurements the LEDs are turned on in the first and turned off in the second measurement or vice versa. The example below shows how the device needs to be configured to turn on all LEDs for integration cycle A to D.

**Figure 18:**  
**LED Configuration Example – All LEDs On During Integration**



# 8 Device and System Calibration

AS7421 is a fully integrated spectrometer, including sensor array, light sources, optics, Fabry-Perot interference filter, cover glass, light guide, all integrated into a single package. Factors such as temperature drift of the LEDs, wavelength shift of the filters but also system related influences such as optical stack-up of the final application influence the measurement results and therefore need to be calibrated to provide accurate and repeatable spectral measurements.

Typically a calibration consist of 2 stages, stage 1 is Device Calibration. ams OSRAM is providing a device calibration file for each individual device which is linked to its unique device ID. This Device Calibration file is needed for final System Calibration and can be used by our provided “Calibration Library”.

System Calibration is done to compensate influences which are caused by final system optical stack up implementation, such as cross talk from cover glasses or influences from external diffusers within the optical stack-up. The System Calibration file (stage 2) is generated by use of our Calibration Library.

**Figure 19:**  
Calibration Stages

Calibration Stage	Addressed Items	Comment
Device Calibration (Stage 1 Calibration)	Sensor Array (responsivity)	Device Calibration file is provided by ams OSRAM for each individual AS7421 device.
	Light Sources (SPD)	
	Temperature Drift of PDs	
	Filter Performance (PWL)	
System Calibration (Stage 2 Calibration)	Optical stack of final application such as cover glasses, system optics...	In order to generate a system calibration file the Device Calibration file and the calibration library are needed.

ams OSRAM is providing the following supporting tools to enable system calibration at customer applications.

**Figure 20:**  
Supporting Tools (SW and Calibration)

Supporting Tools	Function	Version
AS7421 Calibration Library	Provides APIs for system calibration.	1.4.0
Calibration Library API Documentation	Documentation of available APIs.	1.4.0
AS7421 Chip Library	Provide low level access to AS7421 configuration.	4.0.0

Supporting Tools	Function	Version
Chip Library API Documentation	Documentation of Chip Library.	4.0.0
AS7421 Calibration Application Note	Provides details to calibration flow.	1.4

## 9 I<sup>2</sup>C Interface

The device uses I<sup>2</sup>C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I<sup>2</sup>C bus is released). During consecutive Read transactions, the future/repeated I<sup>2</sup>C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1. All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I<sup>2</sup>C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

### 9.1 I<sup>2</sup>C Address

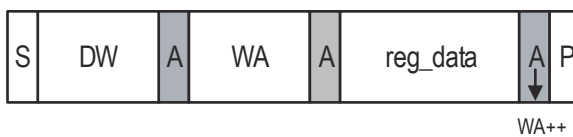
Figure 21:  
AS7421 I<sup>2</sup>C Slave Address

Device	I <sup>2</sup> C Address
AS7421	0x64

### 9.2 I<sup>2</sup>C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP (P). Following each byte (9<sup>th</sup> clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (A/N) on the bus. If the slave transmits N, the master may issue a STOP.

Figure 22:  
I<sup>2</sup>C Byte Write



## 9.3 I<sup>2</sup>C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9<sup>th</sup> clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

**Figure 23:**  
I<sup>2</sup>C Read



## 9.4 Timing Characteristics

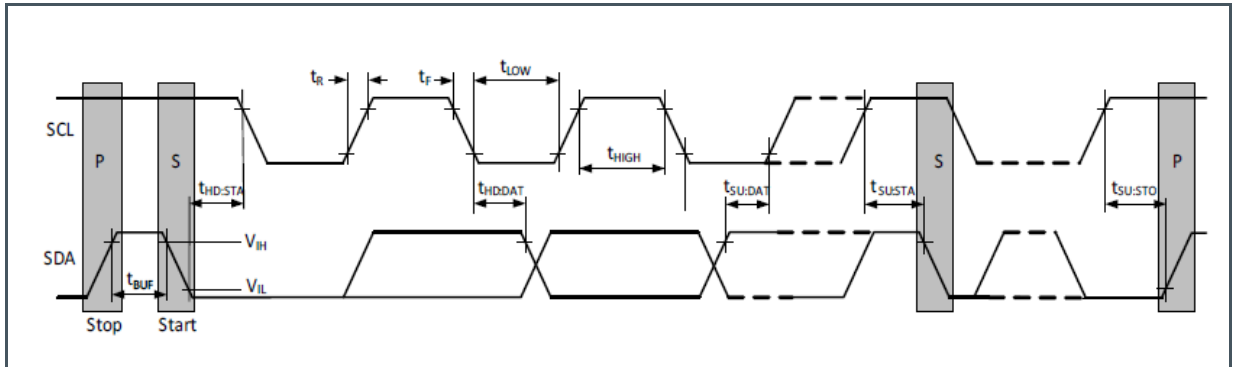
**Figure 24:**  
I<sup>2</sup>C Timing Characteristics

Symbol	Parameter	Min	Max	Unit
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency		400	kHz
t <sub>BUF</sub>	Bus free time between start and stop condition	1.3		μs
t <sub>HS,STA</sub>	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		μs
t <sub>SU,STA</sub>	Repeated start condition setup time	0.6		μs
t <sub>SU,STO</sub>	Stop condition setup time	0.6		μs
t <sub>LOW</sub>	SCL clock low period	1.3		μs
t <sub>HIGH</sub>	SCL clock high period	0.6		μs
t <sub>HD,DAT</sub>	Data hold time	60		ns
t <sub>SU,DAT</sub>	Data setup time	100		ns
t <sub>F</sub>	Clock/data fall time		300	ns
t <sub>R</sub>	Clock/data rise time		300	ns



## 9.5 Timing Diagrams

Figure 25:  
I<sup>2</sup>C Slave Timing Diagram



# 10 Register Description

The device is controlled and monitored by registers accessed through the I<sup>2</sup>C serial interface. These registers provide device control functions and can be read to determine device status and acquire device data.

The register set is summarized below. The values of all registers and fields that are listed as reserved (gray) or are not listed must not be changed at any time. Two-byte fields are always latched with the low byte followed by the high byte. The “Name” column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (D7) to LSB (D0).

Note: After power on reset the following commands have to be written prior accessing other registers:

Write 44h to register 6Fh

Write 20h to register 6Eh

Write 00h to register 6Fh

## 10.1 Register Overview

Figure 26:  
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
<b>Configuration Registers</b>										
0x38	CFG_MISC						LED_WAI T_OFF	WAIT_CYC LE_ON	SW_RST	
0x39	CFG_LED_MUL T				LED_MULT [4:0]					
0x3A	reserved	reserved								
0x3B	reserved	reserved								
0x3C	TEMP_COMPD AC	TEMP_COMPDAC [7:0]								
0x3D	LED_WAIT	LED_WAIT [7:0]								
0x3E	CFG_PINMAP		INT_PINMAP [2:0]			INT_INVE RT	GPIO_PINMAP [2:0]			
<b>RAM Configuration</b>										
0x40	CFG_RAM_0									
...	...	32 Byte for programming the configuration data into the internal RAM								
0x5F	CFG_RAM_31									
<b>Enable Register</b>										
0x60	ENABLE	LTF_MODE [1:0]		LED_AUTO [1:0]		SYNC_E N	TSD_EN	LTF_EN	PON	
<b>Configuration Registers</b>										
0x61	LTF_ITIME_L	LTF_ITIME [7:0]								

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
0x62	LTF_ITIME_M					LTF_ITIME [15:8]				
0x63	LTF_ITIME_H					LTF_ITIME [23:16]				
0x64	LTF_WTIME_L					LTF_WTIME [7:0]				
0x65	LTF_WTIME_M					LTF_WTIME [15:8]				
0x66	LTF_WTIME_H					LTF_WTIME [23:16]				
0x67	CFG_LTF		TEMP_DIODE_SEL [2:0]			LTF_CYCLE [1:0]		CLKMOD [2:0]		
0x68	CFG_LED	SET_LED_ON	LED_OFF_EN		LED_OFFSET [1:0]			LED_CURRENT [2:0]		
0x69	LTF_ICOUNT					LTF_ICOUNT [7:0]				
0x6A	CFG_RAM	REG_BANK				RAM_OFFSET [4:0]				
0x6B	CFG_GPIO					GPIO_IN_VERT	GPIO_OE_N	GPIO_OUT	GPIO_IN	
0x6C	INT_ENABLE				EN_DLOST	EN_DSAT	EN_ASAT	EN_TSD	EN_AZ	EN_ADATA
0x6D	CFG_AZ	AZ_ON	AZ_WTIME [1:0]		AZ_EN	AZ_CYCLE	AZ_ITERATION[2:0]			
<b>Status</b>										
0x70	STATUS_0					DEV_ID [5:0]				
0x71	STATUS_1						REV_ID [2:0]			
0x72	STATUS_2					LTF_ASAT [7:0]				
0x73	STATUS_3					LTF_ASAT [15:8]				
0x76	STATUS_6		TEMP_ASAT	LTF_READY	LTF_BUSY					
0x77	STATUS_7	I2C_DATA_PTR[1:0]		DLOST	DSAT	ASAT	TSD	AZ	ADATA	
<b>Temp</b>										
0x78	TEMP0_L					TEMP0 [7:0]				
0x79	TEMP0_H					TEMP0 [15:8]				
0x7A	TEMP1_L					TEMP1 [7:0]				
0x7B	TEMP1_H					TEMP1 [15:8]				
0x7C	TEMP2_L					TEMP2 [7:0]				
0x7D	TEMP2_H					TEMP2 [15:8]				
0x7E	TEMP3_L					TEMP3 [7:0]				
0x7F	TEMP3_H					TEMP3 [15:8]				
<b>Spectral Channel Output Register</b>										
0x80						CH0_DATA [7:0]				
0x81	CH0_DATA					CH0_DATA [15:8]				
0x82						CH1_DATA [7:0]				
0x83	CH1_DATA					CH1_DATA [15:8]				
0x84						CH2_DATA [7:0]				
0x85	CH2_DATA					CH2_DATA [15:8]				
0x86						CH3_DATA [7:0]				
0x87	CH3_DATA					CH3_DATA [15:8]				
0x88						CH4_DATA [7:0]				
0x89	CH4_DATA					CH4_DATA [15:8]				
0x8A	CH5_DATA					CH5_DATA [7:0]				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x8B					CH5_DATA [15:8]				
0x8C	CH6_DATA				CH6_DATA [7:0]				
0x8D					CH6_DATA [15:8]				
0x8E	CH7_DATA				CH7_DATA [7:0]				
0x8F					CH7_DATA [15:8]				
0x90	CH8_DATA				CH8_DATA [7:0]				
0x91					CH8_DATA [15:8]				
0x92	CH9_DATA				CH9_DATA [7:0]				
0x93					CH9_DATA [15:8]				
0x94	CH10_DATA				CH10_DATA [7:0]				
0x95					CH10_DATA [15:8]				
0x96	CH11_DATA				CH11_DATA [7:0]				
0x97					CH11_DATA [15:8]				
0x98	CH12_DATA				CH12_DATA [7:0]				
0x99					CH12_DATA [15:8]				
0x9A	CH13_DATA				CH13_DATA [7:0]				
0x9B					CH13_DATA [15:8]				
0x9C	CH14_DATA				CH14_DATA [7:0]				
0x9D					CH14_DATA [15:8]				
0x9E	CH15_DATA				CH15_DATA [7:0]				
0x9F					CH15_DATA [15:8]				
0xA0	CH16_DATA				CH16_DATA [7:0]				
0xA1					CH16_DATA [15:8]				
0xA2	CH17_DATA				CH17_DATA [7:0]				
0xA3					CH17_DATA [15:8]				
0xA4	CH18_DATA				CH18_DATA [7:0]				
0xA5					CH18_DATA [15:8]				
0xA6	CH19_DATA				CH19_DATA [7:0]				
0xA7					CH19_DATA [15:8]				
0xA8	CH20_DATA				CH20_DATA [7:0]				
0xA9					CH20_DATA [15:8]				
0xAA	CH21_DATA				CH21_DATA [7:0]				
0xAB					CH21_DATA [15:8]				
0xAC	CH22_DATA				CH22_DATA [7:0]				
0xAD					CH22_DATA [15:8]				
0xAE	CH23_DATA				CH23_DATA [7:0]				
0xAF					CH23_DATA [15:8]				
0xB0	CH24_DATA				CH24_DATA [7:0]				
0xB1					CH24_DATA [15:8]				
0xB2	CH25_DATA				CH25_DATA [7:0]				
0xB3					CH25_DATA [15:8]				
0xB4	CH26_DATA				CH26_DATA [7:0]				
0xB5					CH26_DATA [15:8]				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xB6	CH27_DATA				CH27_DATA [7:0]				
0xB7					CH27_DATA [15:8]				
0xB8	CH28_DATA				CH28_DATA [7:0]				
0xB9					CH28_DATA [15:8]				
0xBA	CH29_DATA				CH29_DATA [7:0]				
0xBB					CH29_DATA [15:8]				
0xBC	CH30_DATA				CH30_DATA [7:0]				
0xBD					CH30_DATA [15:8]				
0xBE	CH31_DATA				CH31_DATA [7:0]				
0xBF					CH31_DATA [15:8]				
0xC0	CH32_DATA				CH32_DATA [7:0]				
0xC1					CH32_DATA [15:8]				
0xC2	CH33_DATA				CH33_DATA [7:0]				
0xC3					CH33_DATA [15:8]				
0xC4	CH34_DATA				CH34_DATA [7:0]				
0xC5					CH34_DATA [15:8]				
0xC6	CH35_DATA				CH35_DATA [7:0]				
0xC7					CH35_DATA [15:8]				
0xC8	CH36_DATA				CH36_DATA [7:0]				
0xC9					CH36_DATA [15:8]				
0xCA	CH37_DATA				CH37_DATA [7:0]				
0xCB					CH37_DATA [15:8]				
0xCC	CH38_DATA				CH38_DATA [7:0]				
0xCD					CH38_DATA [15:8]				
0xCE	CH39_DATA				CH39_DATA [7:0]				
0xCF					CH39_DATA [15:8]				
0xD0	CH40_DATA				CH40_DATA [7:0]				
0xD1					CH40_DATA [15:8]				
0xD2	CH41_DATA				CH41_DATA [7:0]				
0xD3					CH41_DATA [15:8]				
0xD4	CH42_DATA				CH42_DATA [7:0]				
0xD5					CH42_DATA [15:8]				
0xD6	CH43_DATA				CH43_DATA [7:0]				
0xD7					CH43_DATA [15:8]				
0xD8	CH44_DATA				CH44_DATA [7:0]				
0xD9					CH44_DATA [15:8]				
0xDA	CH45_DATA				CH45_DATA [7:0]				
0xDB					CH45_DATA [15:8]				
0xDC	CH46_DATA				CH46_DATA [7:0]				
0xDD					CH46_DATA [15:8]				
0xDE	CH47_DATA				CH47_DATA [7:0]				
0xDF					CH47_DATA [15:8]				
0xE0	CH48_DATA				CH48_DATA [7:0]				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xE1					CH48_DATA [15:8]				
0xE2	CH49_DATA				CH49_DATA [7:0]				
0xE3					CH49_DATA [15:8]				
0xE4	CH50_DATA				CH50_DATA [7:0]				
0xE5					CH50_DATA [15:8]				
0xE6	CH51_DATA				CH51_DATA [7:0]				
0xE7					CH51_DATA [15:8]				
0xE8	CH52_DATA				CH52_DATA [7:0]				
0xE9					CH52_DATA [15:8]				
0xEA	CH53_DATA				CH53_DATA [7:0]				
0xEB					CH53_DATA [15:8]				
0xEC	CH54_DATA				CH54_DATA [7:0]				
0xED					CH54_DATA [15:8]				
0xEE	CH55_DATA				CH55_DATA [7:0]				
0xEF					CH55_DATA [15:8]				
0xF0	CH56_DATA				CH56_DATA [7:0]				
0xF1					CH56_DATA [15:8]				
0xF2	CH57_DATA				CH57_DATA [7:0]				
0xF3					CH57_DATA [15:8]				
0xF4	CH58_DATA				CH58_DATA [7:0]				
0xF5					CH58_DATA [15:8]				
0xF6	CH59_DATA				CH59_DATA [7:0]				
0xF7					CH59_DATA [15:8]				
0xF8	CH60_DATA				CH60_DATA [7:0]				
0xF9					CH60_DATA [15:8]				
0xFA	CH61_DATA				CH61_DATA [7:0]				
0xFB					CH61_DATA [15:8]				
0xFC	CH62_DATA				CH62_DATA [7:0]				
0xFD					CH62_DATA [15:8]				
0xFE	CH63_DATA				CH63_DATA [7:0]				
0xFF					CH63_DATA [15:8]				

## 10.2 Detailed Register Description

Explanation of abbreviation:

- RW = read or write
- RO = read only
- W = write only
- SC = self-clearing after access

### 10.2.1 ENABLE Register (Address 0x60)

Figure 27:  
ENABLE Register

Addr: 0x60		ENABLE		
Bit	Bit Name	Default	Access	Bit Description
7:6	LTF_MODE	00	RW	<b>LTF mode</b> 00: Normal operation 01: Reserved 10: Reserved 11: Reserved
5:4	LED_AUTO	00	RW	<b>Controls NIR light source during spectral measurement</b> 00: LEDs OFF 01: First measurement OFF / second measurement ON 10: First measurement ON / second measurement OFF 11: LEDs ON
3	SYNC_EN	0	RW	<b>Synchronization enable</b> 0: Spectral measurement started with bit LTF_EN 1: Spectral measurement synchronized with signal applied to pin GPIO. GPIO needs to be configured as input in register CFG_GPIO.
2	TSD_EN	0	RW	<b>Automatic power down by temperature measurement</b> 0: OFF 1: ON
1	LTF_EN	0	RW	<b>LTF enable</b> 0: Spectral measurement disabled 1: Spectral measurement enabled
0	PON	0	RW	<b>Power ON</b> 0: Internal oscillator disabled – device enter 1: Internal oscillator enabled – device enter idle state

### 10.2.2 LTF\_ITIME Register (Address 0x61, 0x62, 0x63)

Register 0x61, 0x62 and 0x63 program the integration time of the LTF converter. The integration time is set as follows:

$$t_{int} = (LTF\_ITIME + 1) \times \frac{1}{f_{CLKMOD}}$$

Figure 28:  
LTF\_ITIME\_L Register

Addr: 0x61		LTF_ITIME_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	LTF_ITIME	0	RW	<b>Integration time</b> Low byte of integration time. Do not change during LTF_EN = "1".

Figure 29:  
LTF\_ITIME\_M Register

Addr: 0x62		LTF_ITIME_M		
Bit	Bit Name	Default	Access	Bit Description
15:8	LTF_ITIME	0	RW	<b>Integration time</b> Middle byte of integration time. Do not change during LTF_EN = "1".

Figure 30:  
LTF\_ITIME\_H Register

Addr: 0x63		LTF_ITIME_H		
Bit	Bit Name	Default	Access	Bit Description
23:16	LTF_ITIME	0	RW	<b>Integration time</b> High byte of integration time. Do not change during LTF_EN = "1".



### 10.2.3 LTF\_WTIME Register (Address 0x64, 0x65, 0x66)

LTF\_WTIME register (0x64, 0x65 and 0x66) programs the wait time (WTIME) between two consecutive spectral measurements. The wait time is set as follows:

$$t_{wait} = (LTF\_WTIME + 1) \times \frac{1}{f\_CLKMOD}$$

Figure 31:  
LTF\_WTIME\_L Register

Addr: 0x64		LTF_WTIME_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	LTF_WTIME	0	RW	<b>Wait time</b> Low byte of wait time. Do not change during LTF_EN = "1".

Figure 32:  
LTF\_WTIME\_M Register

Addr: 0x65		LTF_WTIME_M		
Bit	Bit Name	Default	Access	Bit Description
15:8	LTF_WTIME	0	RW	<b>Wait time</b> Middle byte of wait time. Do not change during LTF_EN = "1".

Figure 33:  
LTF\_WTIME\_H Register

Addr: 0x66		LTF_WTIME_H		
Bit	Bit Name	Default	Access	Bit Description
23:16	LTF_WTIME	0	RW	<b>Wait time</b> High byte of wait time. Do not change during LTF_EN = "1".

### 10.2.4 CFG\_LTF Register (Address 0x67)

Figure 34:  
CFG\_LTF Register

Addr: 0x67		CFG_LTF		
Bit	Bit Name	Default	Access	Bit Description
7:5	TEMP_DIODE_SEL	000	RW	<b>Select temperature diode.</b>
4:3	LTF_CYCLE	00	RW	<b>Number of integration cycles during a spectral measurement</b> 00: One integration cycle, A (16 channels) 01: Two integration cycles, A+B (32 channels) 10: Three integration cycles, A+B+C (48 channels) 11: Four integration cycles, A+B+C+D (64 channels) Note: To get spectral data of all 64 channels LTF_CYCLE needs to be set to "11". Do not change this setting during LTF_EN = "1".
2:0	CLKMOD	100	RW	<b>Frequency of integration clock</b> 010: Reserved 100: 1 MHz 101: Reserved 110: Reserved Note: Do not change.

## 10.2.5 CFG\_LED Register (Address 0x68)

Figure 35:  
CFG\_LED Register

Addr: 0x68		CFG_LED		
Bit	Bit Name	Default	Access	Bit Description
7	SET_LED_ON	0	RW	<b>LED enable</b> 0: LED disabled 1: Enable LED permanently Note: Can only be enabled if PON = "1". Bit is automatically cleared with PON = "0".
6	LED_OFF_EN	0	RW	<b>LED off during modulation</b> 0: Normal mode 1: LED is turned OFF during modulation if LTF_MODE is set to "10" (one integration before modulation).
5:4	LED_OFFSET	00	RW	<b>Offset address for programming the values for LED_MULT. Access succeeded via the address CFG_LED_MULT.</b> 00: LED_MULT_0 for integration cycle A 01: LED_MULT_1 for integration cycle B 10: LED_MULT_2 for integration cycle C 11: LED_MULT_3 for integration cycle D
2:0	LED_CURRENT	000	RW	<b>LED current configuration per LED driver</b> 000: 50 mA 001: 75 mA Others: Reserved

## 10.2.6 LTF\_ICOUNT Register (Address 0x69)

Figure 36:  
LTF\_ICOUNT Register

Addr: 0x69		LTF_ICOUNT		
Bit	Bit Name	Default	Access	Bit Description
7:0	LTF_ICOUNT	0	RW	<b>Number of spectral measurements</b> 0x00: No measurement 0xFF: 255 measurements in continuous mode Others: Number of measurements. After every measurement, LTF_ON is set to "0" internally.

### 10.2.7 CFG\_MISC Register (Address 0x38)

Figure 37:  
CFG\_MISC Register

Addr: 0x38		CFG_MISC		
Bit	Bit Name	Default	Access	Bit Description
2	LED_WAIT_OFF	0	RW	<b>LED waiting time</b> 1: Disable the LED waiting time between integration cycle A to D.
1	WAIT_CYCLE_ON	0	RW	<b>LTF waiting time</b> 1: Enable the waiting time between integration cycle A to D (programmable with LTF_WTIME).
0	SW_RST	0	SC	<b>Software reset</b> 1: Reset to default status as after power-on reset or reset via pin RST.

### 10.2.8 CFG\_LED\_MULT Register (Address 0x39)

Figure 38:  
CFG\_LED\_MULT Register

Addr: 0x39		CFG_LED_MULT		
Bit	Bit Name	Default	Access	Bit Description
4:0	LED_MULT	0	RW	<b>Defines which LED is turned ON per integration cycle A to D.</b> 0x1F: All LEDs ON per integration cycle. Other: Reserved Note: LED_OFFSET needs to be set first, after that LED_MULT needs to be written.

### 10.2.9 LED\_WAIT Register (Address 0x3D)

Figure 39:  
LED\_WAIT Register

Addr: 0x3D		LED_WAIT		
Bit	Bit Name	Default	Access	Bit Description
7:0	LED_WAIT	0	RW	Wait time between switching on the LED and begin of integration/modulation.  $t_{LED\_wait} = (LED\_WAIT) \times 1024 \mu s$

### 10.2.10 CFG\_PINMAP Register (Address 0x3E)

Figure 40:  
CFG\_PINMAP Register

Addr: 0x3E		CFG_PINMAP		
Bit	Bit Name	Default	Access	Bit Description
6:4	INT_PINMAP	0	RW	<b>Select signal to output pin INTX.</b> 0: INTX 1: LTF_READY 2: LTF_BUSY 3: LED_ON Others: Reserved
3	INT_INVERT	0	RW	Invert output pin INTX
2:0	GPIO_PINMAP	0	RW	<b>Select signal to output pin GPIO.</b> 0: GPIO 1: LTF_READY 2: LTF_BUSY 3: LED_ON Others: Reserved

### 10.2.11 CFG\_RAM Register (Address 0x6A)

Figure 41:  
CFG\_RAM Register

Addr: 0x6A		CFG_RAM		
Bit	Bit Name	Default	Access	Bit Description
7	REG_BANK	0	RW	Select P2RAM
4:0	RAM_OFFSET	0	RW	<p><b>Offset address for programming the configuration into the RAM. Access succeeded via the addresses CFG_RAM_0 to CFG_RAM_31.</b></p> <p>0x0C: SMUX for integration cycle A                      0x0D: SMUX for integration cycle B                      0x0E: SMUX for integration cycle C                      0x0F: SMUX for integration cycle D                      0x10: ASETUP for integration cycle A/B                      0x11: ASETUP for integration cycle C/D                      0x12: COMPDAC for modulators and integrators                      Others: Reserved</p>

### 10.2.12 CFG\_GPIO Register (Address 0x6B)

Figure 42:  
CFG\_GPIO Register

Addr: 0x6B		CFG_GPIO		
Bit	Bit Name	Default	Access	Bit Description
3	GPIO_INVERT	0	RW	<p><b>GPIO invert</b></p> <p>0: Input/output not inverted;                      1: Input/output inverted.</p>
2	GPIO_OEN	0	RW	<p><b>GPIO output enable</b></p> <p>0: GPIO output disabled;                      1: GPIO output enabled.</p>
1	GPIO_OUT	0	RW	GPIO output
0	GPIO_IN	0	RO	GPIO input

### 10.2.13 INT\_EN Register (Address 0x6C)

Figure 43:  
INT\_EN Register

Addr: 0x6C		INT_EN		
Bit	Bit Name	Default	Access	Bit Description
5	EN_DLOST	0	RW	1: Enable data lost interrupt.
4	EN_DSAT	0	RW	1: Enable digital saturation interrupt.
3	EN_ASAT	0	RW	1: Enable analog saturation interrupt.
2	EN_TSD	0	RW	1: Enable temperature shutdown interrupt.
1	EN_AZ	0	RW	1: Enable auto zero interrupt.
0	EN_ADATA	0	RW	1: Enable ADATA interrupt.

### 10.2.14 CFG\_AZ Register (Address 0x6D)

Figure 44:  
CFG\_AZ Register

Addr: 0x6D		CFG_AZ		
Bit	Bit Name	Default	Access	Bit Description
7	AZ_ON	0	RW	Start single autozero for all modulators and integrators if PON=1.
6:5	AZ_WTIME	00	RW	<b>Wait time for autozero</b> 00: Wait time = 32 $\mu$ s 01: Wait time = 64 $\mu$ s 10: Wait time = 128 $\mu$ s 11: Wait time = 256 $\mu$ s Do not change during LTF_EN = "1"
4	AZ_EN	0	RW	1: Enable autozero during measurements. First autozero starts before the first measurement.
3	AZ_CYCLE	0	RW	1: Autozero is done before each integration cycle.
2:0	AZ_ITERATION	00	RW	Autozero is done every 2 x "AZ_ITERATION".

### 10.2.15 STATUS\_0 Register (Address 0x70)

Figure 45:  
STATUS\_0 Register

Addr: 0x70		STATUS_0		
Bit	Bit Name	Default	Access	Bit Description
5:0	DEV_ID	0B	RO	Device ID

### 10.2.16 STATUS\_1 Register (Address 0x71)

Figure 46:  
STATUS\_1 Register

Addr: 0x71		STATUS_1		
Bit	Bit Name	Default	Access	Bit Description
2:0	REV_ID	01	RO	Revision ID

### 10.2.17 STATUS\_2 Register (Address 0x72)

Figure 47:  
STATUS\_2 Register

Addr: 0x72		STATUS_2		
Bit	Bit Name	Default	Access	Bit Description
7:0	LTF_ASAT [7:0]	0	RO	<b>Analog saturation</b> If set to "1", analog saturation of modulators 0 to 7.



### 10.2.18 STATUS\_3 Register (Address 0x73)

Figure 48:  
STATUS\_3 Register

Addr: 0x73		STATUS_3		
Bit	Bit Name	Default	Access	Bit Description
7:0	LTF_ASAT [15:8]	0	RO	<b>Analog saturation</b> If set to "1", analog saturation of modulators 8 to 15.

### 10.2.19 STATUS\_6 Register (Address 0x76)

Figure 49:  
STATUS\_6 Register

Addr: 0x76		STATUS_6		
Bit	Bit Name	Default	Access	Bit Description
6	TEMP_ASAT	0	RO	Analog saturation of temperature.
5	LTF_READY	0	RO	Measurement is finished. New measurement can be started.
4	LTF_BUSY	0	RO	Measurement is active. New measurement cannot be started.

### 10.2.20 STATUS\_7 Register (Address 0x77)

The register STATUS\_7 contains the information to the interrupt status. The interrupt status is automatically reset after reading the corresponding bit.

Before reading the data of the last measurement register STATUS\_7 has to be read first.

Figure 50:  
STATUS\_7 Register

Addr: 0x77		STATUS_7		
Bit	Bit Name	Default	Access	Bit Description
7:6	I2C_DATA_PTR	10	RO	Information to read data pointer for the temperature and spectral measurement data.
5	DLOST	0	RO	Measurement data has been lost. Time for reading is larger than the time of a measurement.
4	DSAT	0	RO	Digital saturation occurred during the measurement.
3	ASAT	0	RO	Analog saturation occurred during the measurement.

Addr: 0x77		STATUS_7		
Bit	Bit Name	Default	Access	Bit Description
2	TSD	0	RO	Detecting a temperature shutdown.
1	AZ	0	RO	End of autozero.
0	ADATA	0	RO	End of measurement. New measurement data can be read.

### 10.2.21 TEMP Register (Address 0x78 – 0x7F)

The temperature channel data is stored as 16-bit of data spread across two registers.

Before reading the temperature data of the last measurement, register STATUS\_7 has to be read first.

Figure 51:  
TEMP0\_L Register

Addr: 0x78		TEMP0_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	TEMP0	0	RO	Low byte of temperature integration cycle A.

Figure 52:  
TEMP0\_H Register

Addr: 0x79		TEMP0_H		
Bit	Bit Name	Default	Access	Bit Description
15:8	TEMP0	0	RO	High byte of temperature integration cycle A.

Figure 53:  
TEMP1\_L Register

Addr: 0x7A		TEMP1_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	TEMP1	0	RO	Low byte of temperature integration cycle B.

Figure 54:  
TEMP1\_H Register

Addr: 0x7B		TEMP1_H		
Bit	Bit Name	Default	Access	Bit Description
15:8	TEMP1	0	RO	High byte of temperature integration cycle B.

Figure 55:  
TEMP2\_L Register

Addr: 0x7C		TEMP2_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	TEMP2	0	RO	Low byte of temperature integration cycle C.

Figure 56:  
TEMP2\_H Register

Addr: 0x7D		TEMP2_H		
Bit	Bit Name	Default	Access	Bit Description
15:8	TEMP2	0	RO	High byte of temperature integration cycle C.

Figure 57:  
TEMP3\_L Register

Addr: 0x7E		TEMP3_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	TEMP3	0	RO	Low byte of temperature integration cycle D.

Figure 58:  
TEMP3\_H Register

Addr: 0x7F		TEMP3_H		
Bit	Bit Name	Default	Access	Bit Description
15:8	TEMP3	0	RO	High byte of temperature integration cycle D.

### 10.2.22 CHx\_DATA Register (Address 0x80 – 0xFF)

In the registers CH0\_DATA to CH63\_DATA (0x80 to 0xFF) the spectral measurement results are stored. The full scale value of each channel is 16-bit – the low byte is stored in registers CHx\_DATA\_L and the high byte is stored in CHx\_DATA\_H.

Before reading the data of the last spectral measurement register STATUS\_7 (0x77) has to be read first.

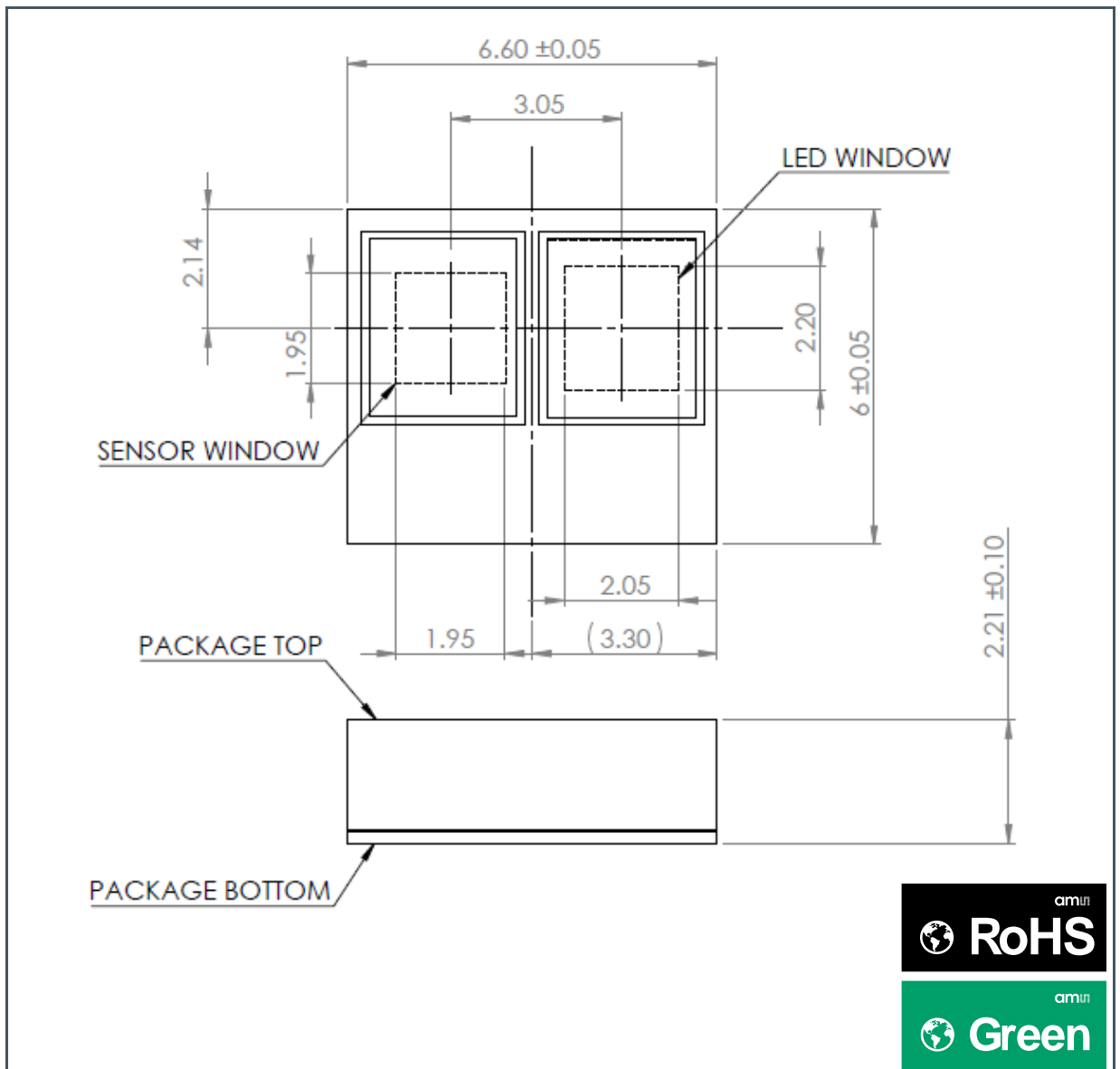
**Figure 59:**  
CHx\_DATA Register

Addr: 0x80 to 0xFF		CHx_DATA_L / CHx_DATA_H		
Bit	Bit Name	Default	Access	Bit Description
15:8	CHx_DATA	0	RO	High byte of channel x spectral data.
7:0	CHx_DATA	0	RO	Low byte of channel x spectral data.

# 11 Package Drawings & Markings

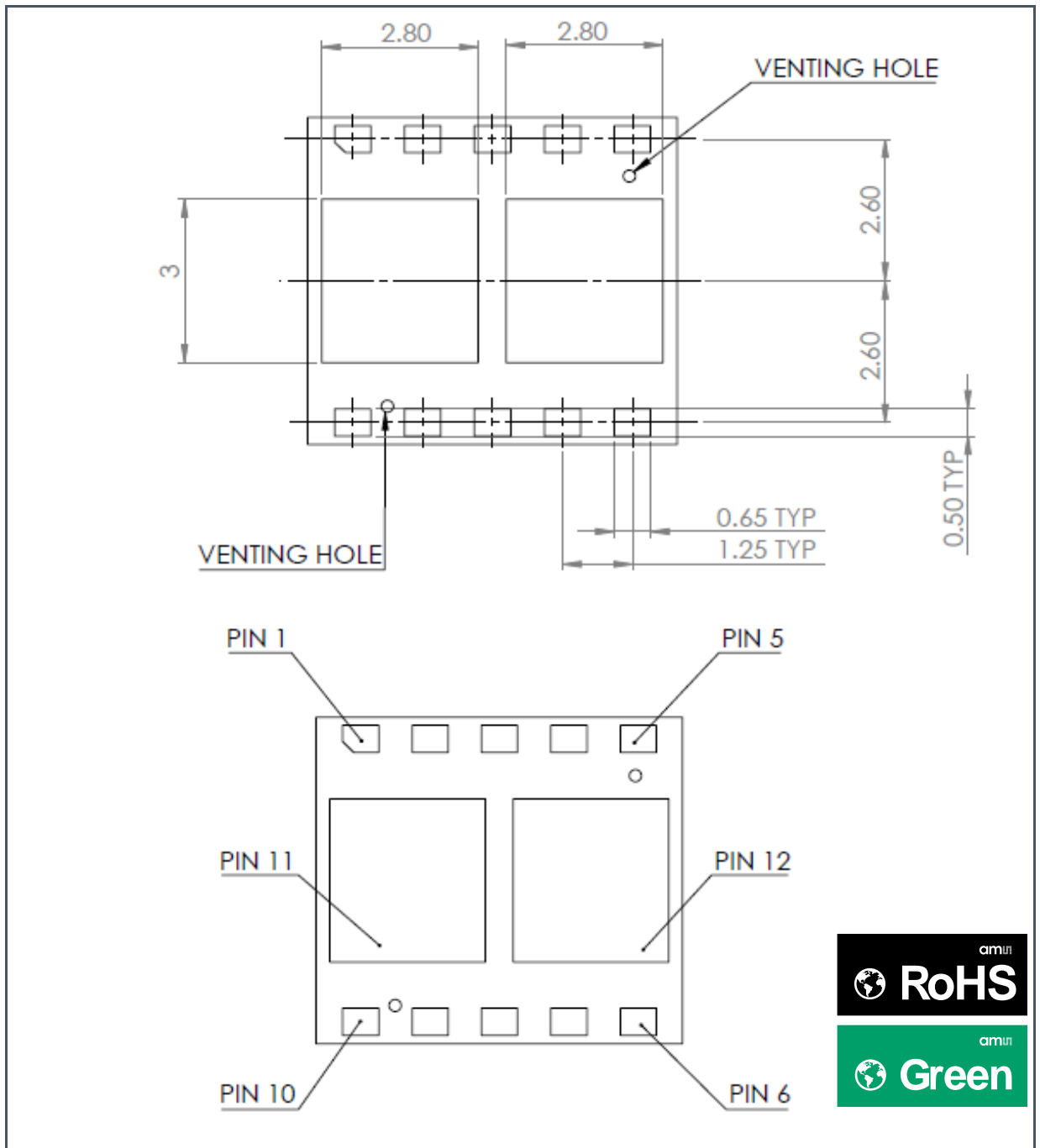
## 11.1 Package Drawings

Figure 60:  
AS7421 OLGA10 Package Outline Drawing – TOP and SIDE View



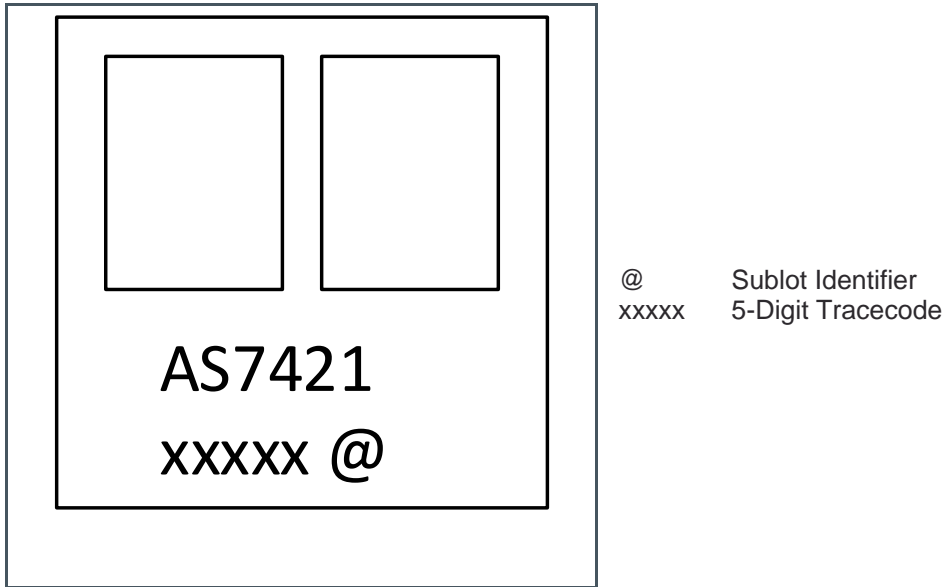
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- (3) This package contains no lead (Pb).
- (4) This drawing is subject to change without notice.

Figure 61:  
AS7421 OLGA10 Package Outline Drawing – BOTTOM View



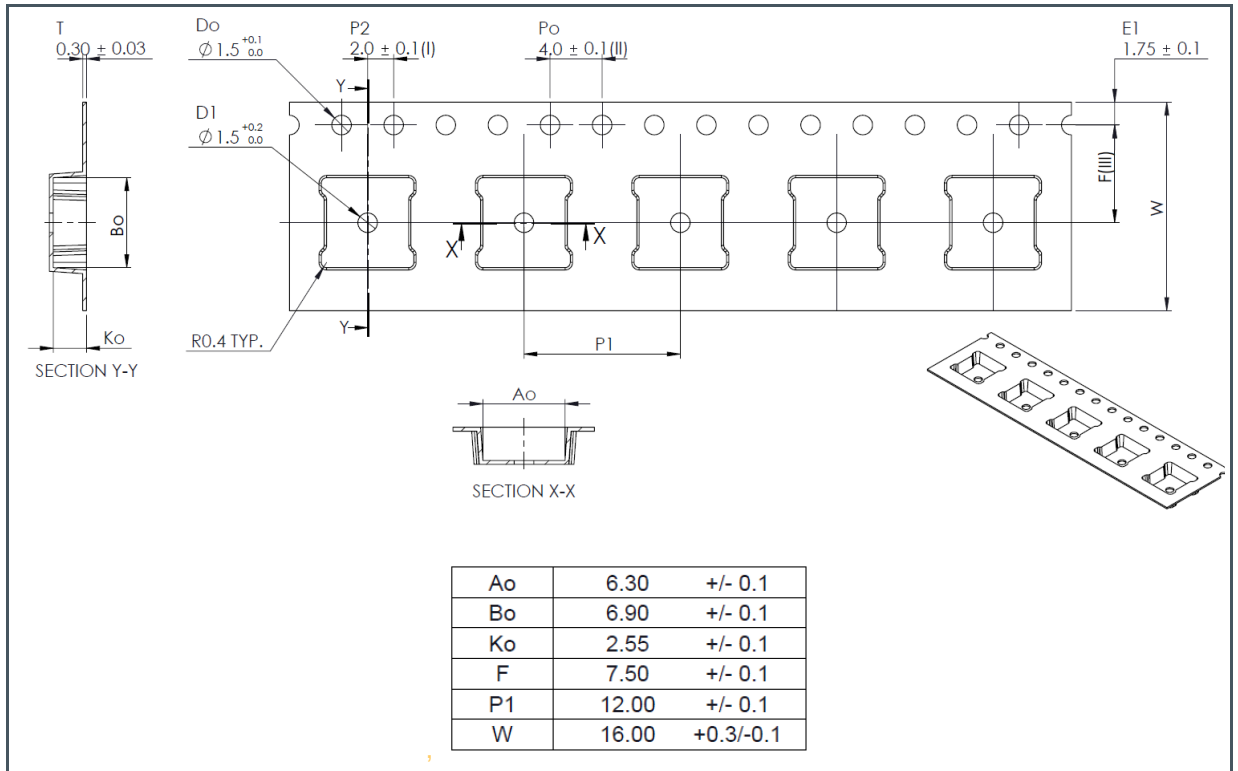
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- (3) This package contains no lead (Pb).
- (4) This drawing is subject to change without notice.

Figure 62:  
AS7421 OLGA 10 Package Marking/Code



# 12 Tape & Reel Information

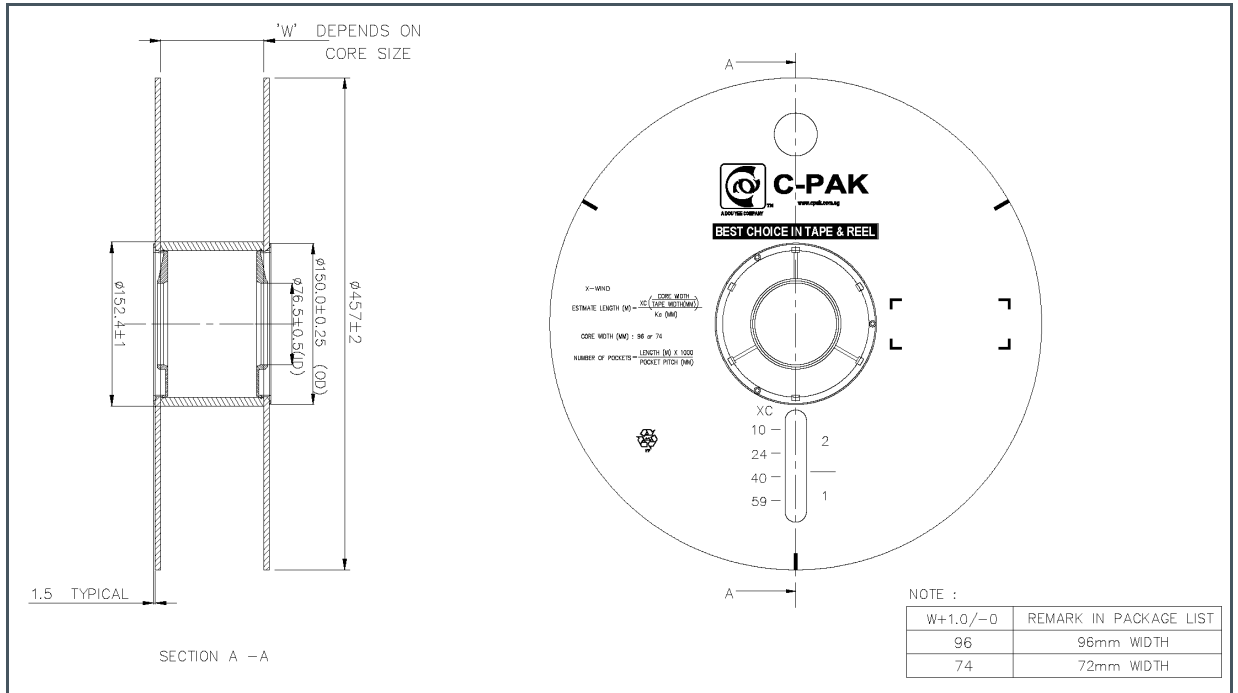
Figure 63:  
AS7421 OLGA10 Tape Dimensions<sup>(1)</sup>



(1) All dimensions are in millimeters.



Figure 64:  
AS7421 OLGA10 Reel Dimensions (1)



(1) All dimensions are in millimeters.

# 13 Soldering & Storage Information

Figure 65:  
Solder Reflow Profile Graph

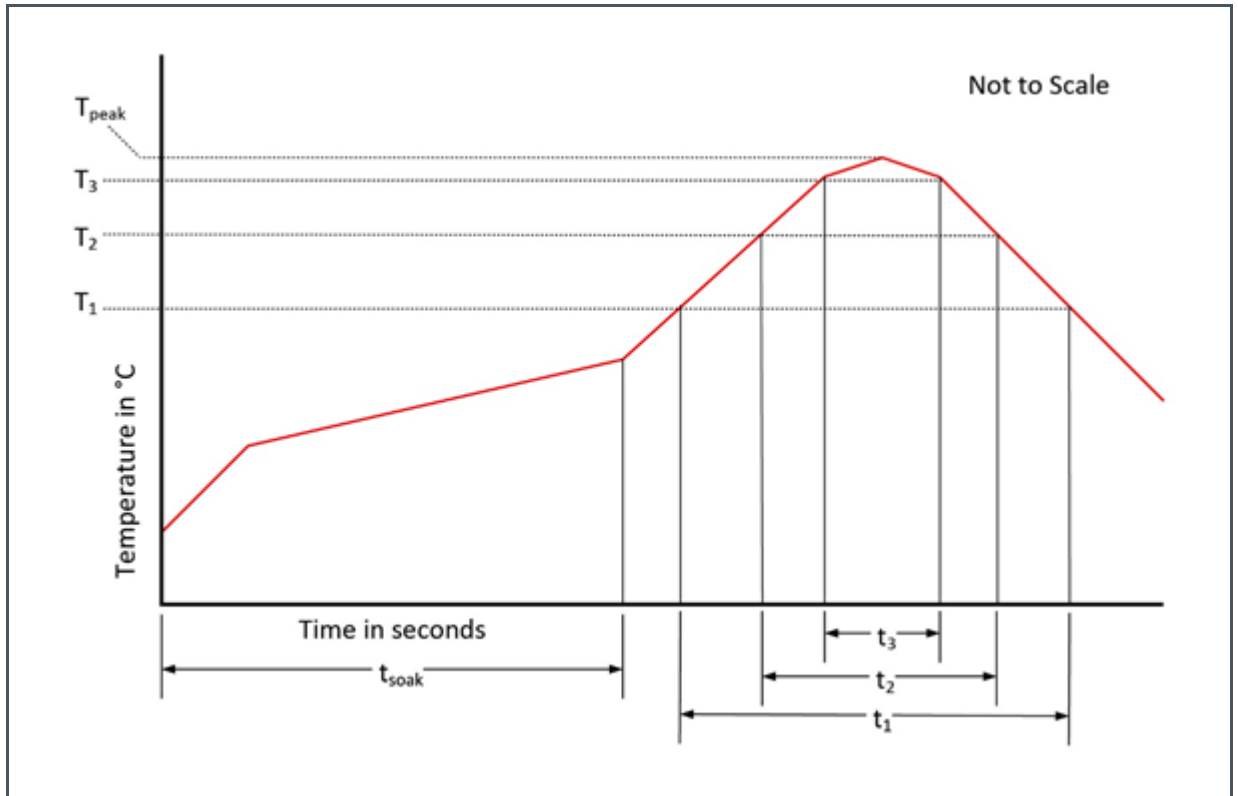


Figure 66:  
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	$t_{soak}$	2 to 3 minutes
Time above 217 °C (T1)	$t_1$	Max 60 s
Time above 230 °C (T2)	$t_2$	Max 50 s
Time above $T_{peak} - 10\text{ °C}$ (T3)	$t_3$	Max 10 s
Peak temperature in reflow	$T_{peak}$	260 °C
Temperature gradient in cooling		Max -5 °C/s

# 14 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v2-00	Page
Added description to chapter 10 (Register overview)	26

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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