AS8520

LIN Transceiver with Voltage Regulator, Attenuator, Relay Drivers, MCU Interface for Automotive Applications

1 General Description

The AS8520 is a companion IC for sensor and actuator LIN slaves. The device provides application specific add-ons, such as the resistive attenuator for battery voltage sensing, a micro controller interface to control 2 relay drivers, to access control register, and diagnosis options. The AS8520 has a window watchdog which can be enabled as a factory option.

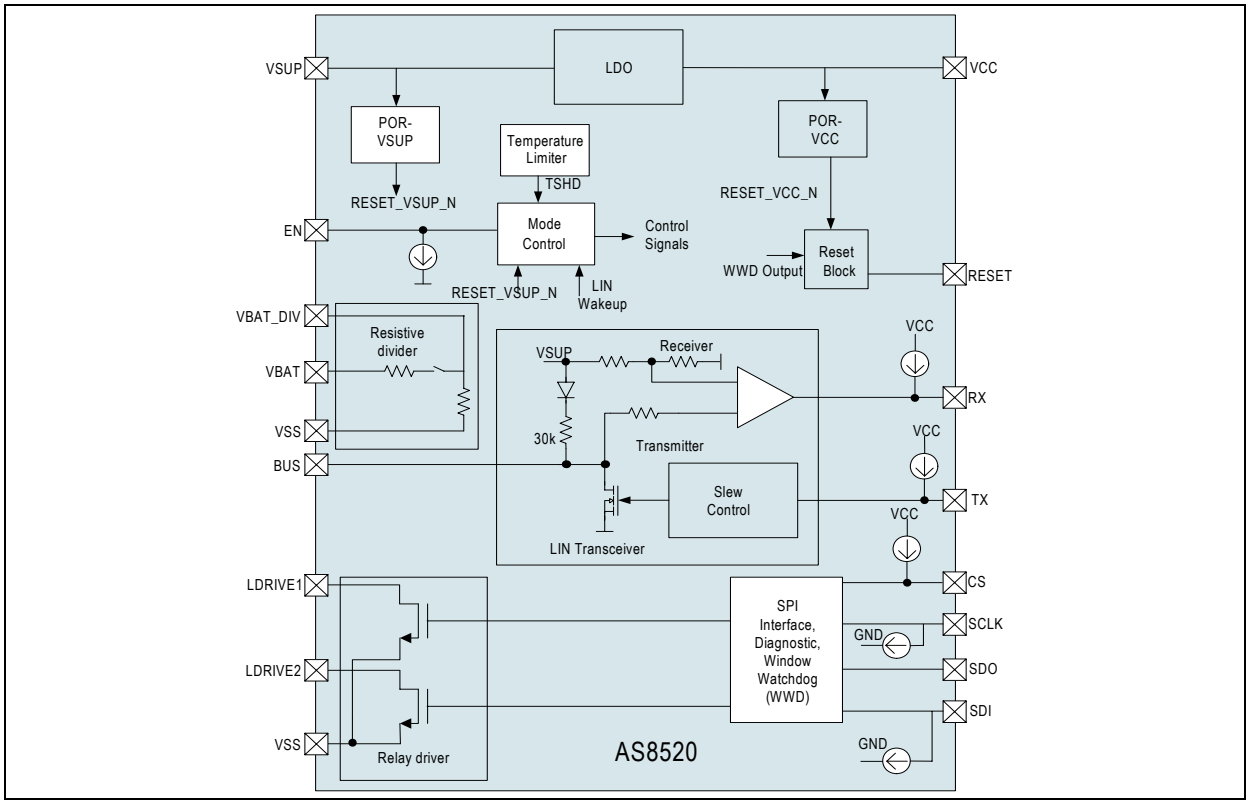
2 Key Features

- Operating voltage 6 to 18V, max. 42V for 500 ms
- Linear, low-drop voltage regulator: V_{CC} = 5V ± 3% or V_{CC} = 3.3V as a factory option
- 50mA load current
- Typical 35 µA quiescent current in standby mode
- Undervoltage detection with reset output, factory adjustable undervoltage threshold and reset time
- LIN bus transceiver with load independent slew control conforming to LIN 2.0 and SAE J2602, short circuit protection, TX time out fail safe feature, over temperature warning and shut down
- Micro controller 4-wire interface for relay driver control, device configuration, status and diagnosis read out, register read / write
- Operating modes: Normal and Standby or Normal and Sleep as a factory option
- Window Watchdog with timing options if factory enabled
- Backup registers to store MCU data during V_{CC} shut down
- Voltage attenuator with disable. Factory selectable ratio options of 21 and 481
- Two low side relay drivers R_{ON} < 5Ω
- -40°C to +125°C ambient operating temperature
- AEC Q 100 automotive qualified
- 6kV ESD on LIN pin according to IEC 61000-4-2
- 24bit chip ID for traceability and module ID
- 24-pin QFN (6x6) package

3 Applications

The AS8520 is suitable for small actuator or sensor LIN slaves. The device is ideal for LIN 2.0/2.1 network applications like Window lift actuators, Sunroof actuators, Seat actuators and battery sensors.

Figure 1. AS8520 Lin Transceiver Block Diagram



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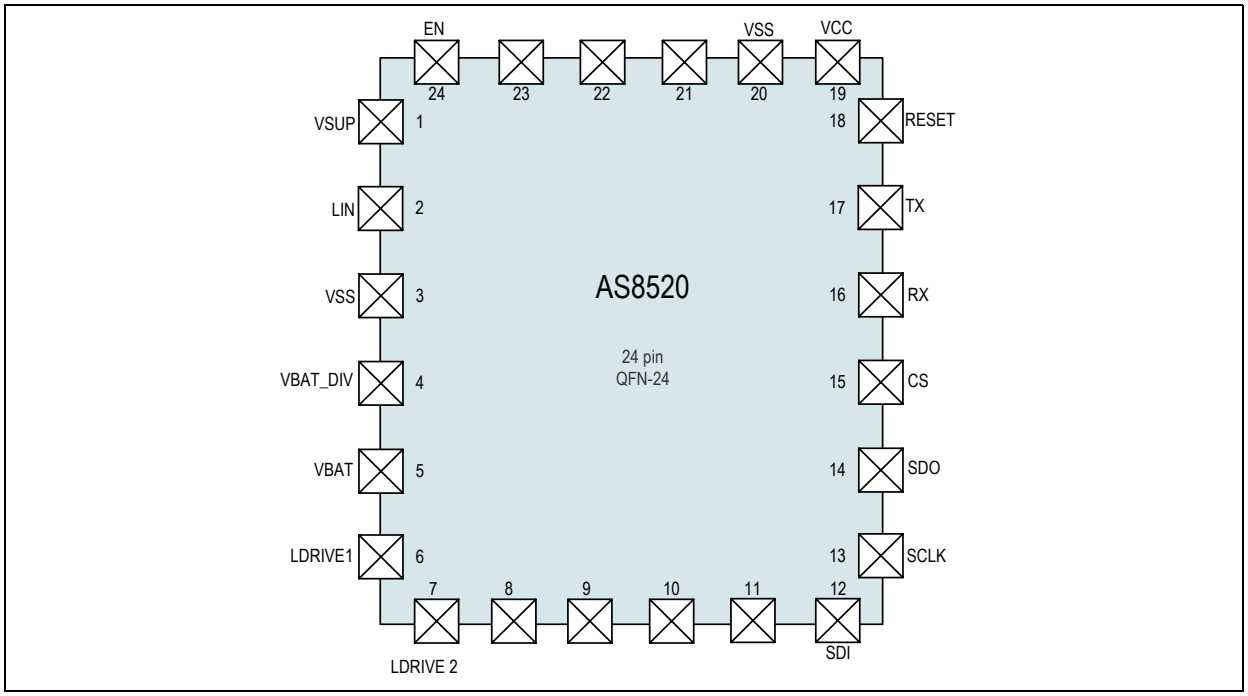
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
VSUP	1	Positive Power Supply
LIN	2	LIN Bus
VSS	3	GND
VBAT_DIV	4	Attenuated battery voltage
VBAT	5	Battery voltage sensing line
LDRIVE1	6	Low side driver
LDRIVE2	7	Low side driver
NC	8	Not connected.
NC	9	Not connected.
NC	10	Not connected.
NC	11	Not connected.
SDI	12	Serial data in
SCLK	13	Serial clock
SDO	14	Serial data out
CS	15	Chip select for Serial Interface
RX	16	LIN transceiver receive signal
TX	17	LIN transceiver transmit signal
RESET	18	Digital Output referenced to Vcc, active low

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
Vcc	19	Regulated 5V/3.3V supply for loads up to 50mA, OTP selectable (factory programmable)
VSS	20	GND
NC	21	Not connected.
NC	22	Not connected.
NC	23	Not connected.
EN	24	High voltage compatible. Enable pin with pull down to VSS, active high.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
DC Supply Voltage	VSUP	-0.3	18	V	
			42		Transient up to 500ms duration
	EN	-0.3	VSUP + 0.3	V	
	VCC	-0.3	7	V	
	LIN	-27	+40	V	
	VBAT	-27	+42	V	
	LDRIVE1, LDRIVE2	-0.3	50	V	
	RESET, RX, TX, CS, SCLK, SDO, SDI, VBAT_DIV	-0.3	VCC + 0.3	V	
Input current (latchup immunity) I_{scr}		-100	100	mA	Norm: Jedec 78
Electrostatic Discharge (ESD)		±2		kV	For on board signals VCC, TX, RX, Reset, CS, SCLK, SDO, SDI, VBAT_DIV, EN
		±4			For VBAT, VSUP, VSS, LDRIVE1, LDRIVE2
		±8			LIN to GND, HBM Model
		±6			LIN to GND, IEC6100-4-2
		±0.5			LIN to GND, CDM
		±0.1			LIN to GND, MM
Total operating power dissipation (all supplies and outputs) P_t			0.75	W	QFN 24 in still air, soldered on JEDEC standard board @125° ambient, static operation = no time limit
Thermal Package Resistance (R_{th})			33	K/W	Soldered on JEDEC standard board @125° ambient, static operation = no time limit
Storage temperature (T_{strg})		-55	+150	°C	
Package body temperature (T_{body})			+260	°C	The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices”.
Humidity non-condensing		5	85	%	

6 Electrical Characteristics

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions						
VSUP	Positive Supply Voltage	Normal operating condition	6		18	V
		Jump-start/ over-voltage condition			27	V
		Load dump condition			42	V
VSS	Negative Supply Voltage		0			V
TAMB	Ambient temperature	Max junction temperature (TJ) 150ºC	-40		+125	ºC
I_{supp}	Supply Current				65	mA
DC/AC Characteristics for Digital Inputs and Outputs[1]						
Enable Input						
VIH	High level input voltage		0.8VCC			V
VIL	Low level input voltage				0.2VCC	V
ILEAK	Input leakage current	EN = L	-1		+1	µA
I_{pd_en}	Pull down current	EN = VCC = 5V	30		100	µA
TX, CS Input						
VIH	High level input voltage		0.8VCC			V
VIL	Low level input voltage				0.2VCC	V
ILEAK	Input leakage current	TX = VCC	-1		+1	µA
I_{pu}	Pull up current	RX, TX,CS pulled to VCC	-100		-30	µA
SDI, SCLK						
VIH	High level input voltage		0.8VCC			V
VIL	Low level input voltage				0.2VCC	V
ILEAK	Input leakage current		-1		+1	µA
I_{pd_spi}	Pull down current	SDI, SCLK pulled to VSS	30		100	µA
RESET, SDO						
VOH	High level output voltage	VSUP ≥ 6V, I = 1 mA	VCC-0.5			V
VOL	Low level output voltage	VSUP ≥ 6V, I = 1 mA			VSS + 0.4	V
RX						
VOH	High level output voltage	VSUP ≥ 6V, I = 1 mA	VCC-0.5			V
VOL	Low level output voltage	VSUP ≥ 6V, I = 1 mA			VSS + 0.4	V
I_{pu_reset}	Pull-up current	Pulled up to VCC	-100		-30	µA

1. All pull-up, pull-downs are implemented with active devices. RESET, RX, SDO have been measured with 10pF load.

6.1 Detailed System and Block Specifications

Table 4. System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IDD_{nom}	Current consumption normal mode	No load on Vcc, LIN inactive, VSUP = 14V, RES_DIV enabled		300		µA
		No load on Vcc, LIN active, VSUP = 14V, RES_DIV enabled		700		
		No load on Vcc, LIN inactive, VSUP = 14V, RES_DIV disabled		250		
IDD_{stby}	Current consumption standby mode	@ 85ºC ambient (no load)		40		µA
		@125ºC ambient (no load)		45		
IDD_{sleep}	Current consumption sleep mode	@ 85ºC ambient (no load)		30		µA
		@ 125ºC ambient (no load)		35		

6.1.1 Low Dropout Regulator

The LDO is a linear voltage regulator, which provides a regulated (band-gap stabilized) output voltage (Vcc) from the battery supply voltage (VSUP).

(6V < VSUP < 18V; -40ºC < TJ < +150ºC; all voltages are with respect to ground (VSS); positive current flows into the pin), normal operating mode if not otherwise mentioned.

Table 5. LDO Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP	Battery Voltage Range	Default, Need safe operating area calculations with package Rth	6	12	18	V
Vcc	Output Voltage Range	Load < 50mA	4.85	5.0	5.15	V
		Factory option, load < 50mA	3.15	3.3	3.45	
		50 to 65mA	4.5		5.15	
		Factory option, 50 to 65mA	2.9	3.3	3.45	
		Standby mode @ ICC < 5mA	4.5		5.5	
		Load-dump condition, Iload < 50mA			5.5	
		Factory option, Standby mode @ ICC < 5mA	3		3.6	
ICC_SH	Output Short Circuit Current	Normal mode	50		250	mA
		Standby mode	5		250	
dVcc1	Line Regulation	ΔVcc / ΔVSUP			8	mV/V
LOREG_SM	Load Regulation (Standby mode)	ΔVcc / ΔICCn (for Iload > 500uA)			10	mV/mA
LOREG_NM	Load Regulation (Normal mode)	ΔVcc / ΔICCn (for Iload > 500uA)			1	mV/mA
CL1	Output Capacitor (Electrolytic)		2.2		10	µF
ESR1			1		10	Ω
CL2	Output Capacitor (Ceramic)		100		220	nF
ESR2			0.02		1	Ω
CSUP1E	Input capacitor (Electrolytic)	For EMC suppression	10		100	µF
ESR1_CSUP			1		10	Ω
CSUP2C	Input capacitor (Ceramic)	For EMC suppression	100		220	nF
ESR2_CSUP			0.02		1	Ω

6.1.2 LIN Transceiver

(4.5V < VCC < 5.5V; 6V < VSUP < 18V; -40ºC < TJ < 150ºC, VBUS is the voltage on the LIN node. All voltages are with respect to ground (VSS); positive current flows into the pin.

Table 6. DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver						
I_{bus_lim}		Current limitation in Dominant State LIN = VSUP_max	40	120	200	mA
LIN_V_{OL}		Output Voltage BUS (dominant state), I_{LIN} = 40mA (short-circuit condition tested at V_{OL} = 2.5V)			2	V
	Pull-up resistor	Normal mode (recessive BUS level on TX pin)	20	40	60	kΩ
$I_{bus\_leak\_rec}$		Driver OFF; VSUP = 7.3V, 8V<VBUS<18			20	µA
Receiver						
$I_{bus\_leak\_dom}$	Input Leakage current at receiver	Driver OFF; Vbus = 0v; VSUP = 12v; VCC = 5V	-1			mA
$I_{bus\_no\_GND}$		VSS = VSUP; VSUP = 12V; 0V<VBUS<18V, VCC = 5V	-1		1	mA
$I_{bus\_no\_bat}$		VSUP = VSS; 0V<VBUS<18V, VCC = VSS			100	µA
V_{bus_dom}					0.4	VSUP
V_{bus_rec}			0.6			VSUP
V_{bus_cnt}		$V_{bus\_cnt} = (V_{th\_dom} + V_{th\_rec})/2$ [1]	0.475		0.525	VSUP
V_{hys}		$V_{hys} = (V_{th\_dom} - V_{th\_rec})$ [1]	0.05		0.175	VSUP

1. Vth_dom: Receiver threshold of the recessive to dominant LIN bus edge
   Vth_rec: Receiver threshold of the dominant to recessive LIN bus edge

Table 7. AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D1 (worst case 20Kbps transmission)		V_{th_rec}(max) = 0.744 x VSUP; V_{th_dom}(max) = 0.581 x VSUP; VSUP = 6.0V...18V; tbit = 50µs; D1 = tbus_rec(min) / (2 x tbit) OTP selection = High Slew Mode	0.369			
D2 (worst case 20kbps transmission)		V_{th_rec} (min) = 0.422 x VSUP; V_{th_dom} (min) = 0.284 x VSUP; VSUP = 6V...18V; tbit = 50µs; D2 = tbus_rec(max) / (2 x tbit) OTP selection = High Slew Mode			0.581	
D3 (worst case 10.4kbps transmission)		V_{th_rec} (max) = 0.778 x VSUP; V_{th_dom} (max) = 0.616 x VSUP; VSUP = 6.0V...18V; tbit = 96µs; D3 = tbus_rec(min) / (2 x tbit) OTP selection = Low Slew Mode	0.417			

Table 7. AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D4 (worst case 10.4kbps transmission)		V_{th_rec} (min) = 0.389 x VSUP; V_{th_dom} (min) = 0.251 x VSUP; VSUP = 6V...18V; tbit = 96µs; D4 = tbus_rec(max) / (2 x tbit) OTP selection = Low Slew Mode			0.59	
t_{dLR}		Vcc = 5v; Propagation delay bus dominant to RX LOW			6	µs
t_{dHR}		Vcc = 5v; Propagation delay bus dominant to RX HIGH			6	µs
t_{RS}		Receiver Delay symmetry	-2		2	µs
t_{wake}		Wake-up delay time	30		150	µs
t_{sln}		Transition from standby mode to normal mode (clock frequency is 128KHz ± 25%)		4		Clock cycles
t_{nsl}		Transition from normal mode to standby mode (clock frequency is 128KHz ± 25%)		6		Clock cycles
t_{rec_deb}		Receiver De-bounce time	0.6		1	µs
C_{int}		Internal capacitance of the LIN node configured as a slave			250	pF

Table 8. Temperature Limiter

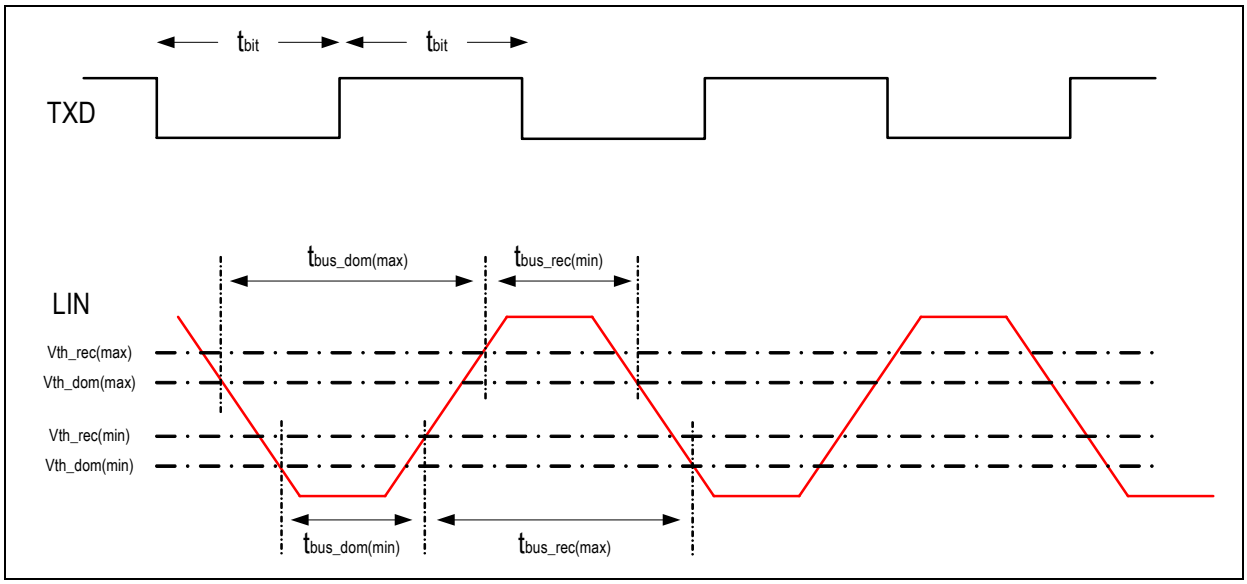
Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sd}	Shut down temperature	junction temperature	144		176	ºC
T_{ret}	Return temperature	[1] [2]	126		154	ºC
T_{otset}	Over-temp warning flag set	The temperature beyond which the warning flag is set.	126		154	ºC
$T_{otclear}$	Over-temp warning flag clear	The return temperature when the warning flag is cleared	108		132	ºC

1. During shut down, the sensor must be powered by VSUP.
2. Thermal shut down disables LDO and sets all drivers to high impedance, the IC returns from shut down with POR

Table 9. TX Timeout Watchdog

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{lin_wdog}	Time out duration (dominant state)		0.5	1	2	s

Figure 3. LIN Timing Diagram



6.1.3 Vcc Undervoltage Reset and Window Watchdog

The values in this table are valid for normal and standby modes. All parameters are tested unless mentioned.

Table 10. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vuvr_off	Vcc under-voltage threshold off	Rising edge of Vcc	2.55		2.95	V
Vuvr_on	Vcc under voltage threshold on	Falling edge of Vcc	2.3		2.7	V
Vuvr1_off	Vcc under voltage threshold off (Default)	Rising edge of Vcc	3.0		3.4	V
Vuvr1_on	Vcc under voltage threshold on (Factory Option)	Falling edge of Vcc	2.75		3.15	V
Vuvr2_off	Vcc under voltage threshold off (Factory Option)	Rising edge of Vcc	3.5		3.9	V
Vuvr2_on	Vcc under voltage threshold on (Factory Option)	Falling edge of Vcc	3.25		3.65	V
Vuvr3_off	Vcc under-voltage threshold off (Factory Option)	Rising edge of Vcc	4.0		4.4	V
Vuvr3_on	Vcc under voltage threshold on (Factory Option)	Falling edge of Vcc	3.75		4.15	V
Vhyst_vcc	Hysteresis of under-voltage threshold on/off Vcc	Default and all other OTP options	0.1	0.25	0.4	V
t_{rr}	Spike filter on Vcc	To remove disturbance	4			µs
Vsuvr_off	VSUP under-voltage threshold off			3.85		V
Vsuvr_on	VSUP under-voltage threshold on	BOR level (considered to be the Master Reset for AS8520)		3.25		V
	Hysteresis on under-voltage threshold on/off VSUP		0.2	0.5	0.7	V
WD_TCL	WWD non-service time (if factory enabled)	RESET will be generated[1]	0-75	0 -100	0-125	ms
WD_TSV	WWD Service – time (if factory enabled)	RESET will not be generated	75-150	100-200	125-250	ms

Table 10. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{Res}	Reset delay time	4ms, 16ms, 32ms (typ) are factory options (min = -25% and max = +50% of typical)	6	8	12	ms
T_{shd}	Temporary shutdown reset active time		0.1		1	s

1. -40%, -20%, +20%, +60%, and +100% timings are available as factory options.

Table 11. Resistive Divider

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{RHRL}	Division ratio[1]		20.8	21	21.2	
Vin_bat	Input Battery Voltage Range	LDO must turn ON	6.8		18	V
Vbat_leak		V_{BAT} = 18V	-1		1	µA
TC_{RHRL}	Temperature drift of dividing ratio	from -40 to +125 deg (guaranteed by design) 11V<V_{BAT}<13V			2	%

1. A division ratio of 481 is available as factory option.

Table 12. Low Side Relay Driver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOL	Output low level	@ 80 mA			0.4	V
Vovthh	Battery Over Voltage Threshold HIGH	Drivers will turn off when exceeded	20		24	V
Vovthl	Battery Over Voltage Threshold LOW		18		22	V
Vovhys	Battery Over Voltage Hysteresis		1		3	V
Vcl	Drain to Source clamp Voltage	Vcl < 50V, Iload = 10mA	VSUP + 1		VSUP + 5	V
Lload	Load Inductance		0.125		0.25	H
Rload	Load Resistance		80		120	Ω
Ron	ON Resistance				5	Ω
Ioz	Leakage in off state				1	µA

Table 13. SPI Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
B_{RSPI}	Bit rate				250	Kbps
T_{SCLKH}	Clock high time		2			µs
T_{SCLKL}	Clock low time		2			µs
Write Timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
T_{CSH}	CS hold time		20			ns
Read Timing						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns

Table 13. SPI Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Timing parameters when entering 4-Wire SPI mode (for determination of CLK polarity)						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns

7 Detailed Description

The AS8520 chip consists of a low drop-out regulator 5V/50mA, two low-side relay drivers, a resistive divider to monitor battery voltage and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller. Additionally integrated is a RESET unit with a power-on-reset delay and a programmable watchdog time. It also includes a watchdog time-out on LIN TX node to indicate if the microcontroller is stuck in a loop and the LIN bus remains in dominant time for more than the necessary time.

7.1 Block Description

The main blocks of the AS8520 are explained below.

7.1.1 Voltage Regulator (LDO)

The voltage regulator has three operating modes. The features of the operating modes are given below:

- Normal mode: Stability to be better ±0.15V over input range and temperature for load current up to 50mA. The LDO Output provides a voltage of 5V (3.3V as OTP option).
- Standby mode: The Standby mode is a low quiescent current mode used in car applications that are always switched on. The load current in standby mode is 5mA. Quiescent current (no load) is less than 25µA typically at room temperature.
- Power down mode: The Power down or temporary shutdown of the regulator can be set by a register bit. This bit can be written through 4-wire MCU interface.

The LDO takes the input from bandgap and scales it up to the required voltage. The LDO starts charging only after the POR-VSUP event occurs (RESET_VSUP_N switched from low to high). The LDO can be powered-down by a control signal (temporary shutdown register) for the temporary shutdown mode.

7.1.2 Temperature Limiter

Temperature limiter produces a power down when temperature exceeds 160ºC ±10%. It powers up and generates a reset when it returns to 140ºC ±10% junction temperature. During thermal shut down, temperature sensor is supplied by VSUP. There is an option control bit provided to enable or disable this temperature monitoring circuit. During the temperature ramp-up phase, as soon as the temperature exceeds 140ºC ±10%, a warning signal is issued and is written into the diagnostic register, which can be read through the SPI interface.

7.1.3 VSUP Undervoltage Reset

VSUP undervoltage reset generates a reset RESET_VSUP_N, switched from low to high when VSUP ramps up above VSUVR_OFF. This is used to enable proper initialization of mode control and diagnostic registers. If VSUP < VSUVR_ON, then RESET_VSUP_N switches from high level to low level (active). This is considered to be the master reset and will have the highest priority over all other signals. As soon as VSUP < VSUVR_ON, the LDO, LIN Transceiver is completely shut off and system comes to a complete stop. AS8520 enters into the normal operating mode only after VSUP > VSUVR_OFF.

7.1.3.1 VSUP Undervoltage in Normal Mode

Supply Voltages below VSUVR_OFF and above VSUVR_ON do not influence the voltage regulator. The output voltage V_{CC} follows VSUP.

7.1.3.2 VSUP Undervoltage in Standby Mode / Sleep Mode

No exit from the sleep mode or standby mode take place if the VSUP voltage drops down to VSUVR_OFF. If VSUP goes below VSUVR_ON, RESET_VSUP_N is active and resets the mode control and diagnostic register. The voltage regulator, LIN Transceiver modules are turned off. If VSUP rises again above VSUVR_OFF, RESET_VSUP_N is switched from low to high. The system enters normal mode where LIN Transceiver and LDO are switched on.

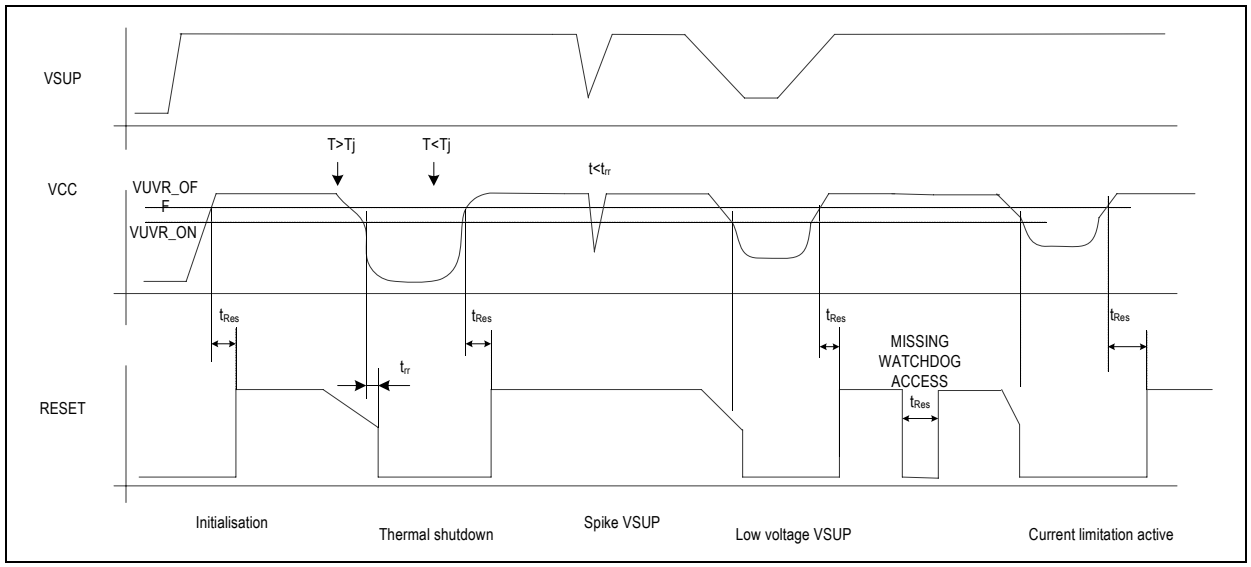
7.1.3.3 VSUP Undervoltage in Low Slew Mode

The behavior of AS8520 at low VSUP voltages is equal to the sleep mode. The low slew mode (set by control register through serial interface as an option) will be cancelled, if VSUP drops below VSUVR_ON in this mode. The AS8520 enters the normal mode, if VSUP rises again above VSUVR_OFF.

7.1.4 RESET

Reset generates an external RESET signal to reset the microcontroller and all other external circuits. The reset functionality is illustrated in Figure 4. Reset consists of a digital buffer at the output. RESET signal can be affected by RESET_VCC_N (which is the under-voltage reset on V_{CC}) and Window watchdog output. All those conditions which cause a drop in the V_{CC} voltage will be detected from the low voltage reset unit, which in-turn generates a reset signal. States like Temporary shut-down, Over-temperature monitor will influence the RESET output through RESET_VCC_N signal only.

Figure 4. Reset Functionality



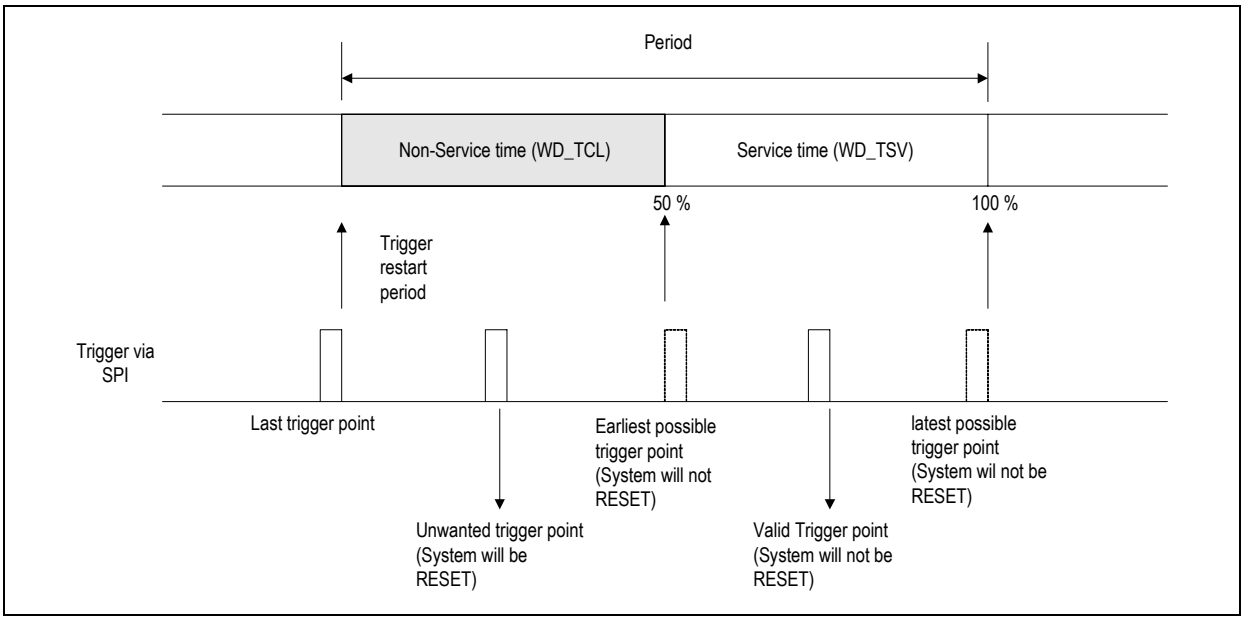
7.1.5 Vcc Undervoltage Reset

The POR-VCC generates RESET_VCC_N signal as output which determines under-voltage reset of the output of the LDO. The rising edge of the VCC gives an under-voltage reset “off” and the falling edge of the VCC gives an under-voltage reset “on”. This under-voltage signal is used to control the RESET output. When VCC rises up Vuvr_off for a period greater than reset duration (tRes) then RESET_VCC_N switches from low level to high level and pin RESET is inactive (high). If VCC falls below Vuvr_on for a period greater than a predetermined delay (trr) then RESET_VCC_N switches from high level to low level and pin RESET is active (low). The RESET_VCC_N signal is used to initialize Window watchdog timer, TX time-out, Test control circuits, 4-wire SPI, and logic associated with SPI (everything other than the SPI control registers). VCC under-voltage reset threshold voltage level adjustment can be made by 2 bit OTP as explained in OTP interface.

7.1.6 Window Watchdog (WWD)

To keep the external microcontroller always in proper function state, a window watchdog circuit is implemented. The WWD trigger is generated by external MCU through SPI interface. If the window is missed, a reset on the RESET pin with certain reset time (t_{Res}) is generated. The WWD function can be enabled or disabled by factory setting. The watchdog is started after the ASSP exits reset. Under normal working conditions, microcontroller gives a WWD trigger every time in the window period of WD_TSV (service time). If the trigger does not occur during WD_TSV or occurs too early during WD_TCL (non-service time), then RESET output is pulled low (active), which will reset the micro-controller. WWD circuit is turned on after the RESET pin goes back to high (inactive). If VCC < Vuvr_on, WWD circuit is switched off. When the WWD function is enabled, there is a 3-bit factory programming available to set the trigger window.

Figure 5. Window Watchdog Trigger



7.1.7 Resistive Divider

The resistive divider acts as a battery voltage attenuator. The output of this resistive divider can be connected to an ADC for monitoring the battery voltage. The division ratio of resistive divider is 21 but can be set also to 481 as a factory programming option. Both divider options can be disabled in standby mode using the EN signal. Reverse polarity protection of VBAT pin is provided.

7.1.8 HV Low Side Relay Driver Switches

Two NMOS open drain relay driver devices provide over voltage protection. The Driver is disabled if the MCU software hangs up (watchdog reset or time out WD for LIN TX). The input to the drivers is given through SPI (Low-side driver data register). If over voltage occurs, the Relay driver turns off irrespective of the input. The driver stays turned off till the voltage returns back to the normal operating range. An optional control bit available in the Device configuration register, which can be used to switch off the drivers independently to save power. The relay drivers are disabled using the SPI.

7.1.9 LIN Transceiver

The transceiver provides short circuit limitation, hardware watchdog and over temperature shut down features. The TX watchdog timer is active when TX is pulled low (active). As soon as the TX watchdog timeout occurs, the LIN bus is released from dominant state to recessive state. The LIN transceiver has a pull-up resistor (for the slave node; extra resistor externally for the master node) to the VSUP. A diode protection is available to protect it from back supply from bus line.

The LIN transmitter has the basic functionality of relaying the data from the micro-controller on to the LIN. The data on the LIN needs to have controlled slew to have reduced EMI. The receiver relays the data from the LIN to the micro-controller. This transmitter has optimized EMC performance across different loading conditions conforming to the LIN 2.1 standards. The wake-up detects a wake up event on the LIN.

7.2 Operating Modes and States

The AS8520 provides four main operating modes “normal”, “sleep/stand-by” (programmed by OTP), “temporary shutdown” and “thermal shutdown”. The LIN transceiver can be programmed to operate with lower slew in the normal mode. Refer to Table 14 for a detailed description on transition for each mode.

7.2.1 Normal Mode

This is the mode after the power-up. In normal mode, LDO, LIN Transceiver, Window Watchdog, Resistive divider and the line drivers are all turned on. All the blocks are completely functional. LDO is now capable of delivering maximum load current possible as per the device specifications. The LIN Transceiver is capable of sending the TX data from microcontroller to the LIN bus at a maximum rate of 20Kbps. Resistive divider is used to attenuate the battery voltage and relay drivers are used to drive the relay. EN signal is set to high and LIN, TX, RX pins can be driven into dominant (low) or recessive (high) states. If the junction temperature increases more than T_{otset}, a warning flag is set in the diagnostic register, which can be read through the SPI interface.

7.2.2 Standby Mode

Standby mode is a functional low-power mode where the LDO is switched into a low-power state with low drive capability and lower accuracy of the output voltage. LIN Transceiver is disabled. The LIN wake-up circuit and over-temperature monitor circuit is enabled. Window watchdog, TX timeout watchdog, Resistive divider, relay driver circuits are disabled. EN pin held low in this mode. TX pin is in recessive state (high). CS is pulled to VCC while SDI and SCLK outputs are pulled to VSS.

7.2.3 Sleep Mode

As a factory programming option on request the AS8520 offers as a replacement to the standby mode with sleep mode. Sleep mode is the most current saving mode. If EN is held low, the LDO, LIN Transceiver, the gate drivers, the resistive divider and the reset and window watchdog unit will be switched off. VCC is pulled down to zero. CS is low. The LIN wake-up circuit, oscillator and over-temperature monitor circuit is active. LIN bus is in recessive state (high). Only wake-up possible is through remote wake-up, through LIN pin, pulling it to dominant state for 100µs typical (low), can change the state of the system.

7.2.4 Temporary Shutdown Mode

In this mode, the VCC is pulled down and the LDO is powered down. This mode is introduced to interface with other components which do not have a pin for the reset functionality. This provides an alternative way to reset those components interfacing with AS8520. This mode is default disabled but can be enabled by an OTP option. In this mode, all internal modules supplied by the LDO are disabled. Only the oscillator, control registers are enabled. The VCC output can be temporarily switched off and pulled to VSS. EN signal, RX, TX is pulled low and LIN Transceiver along with the LIN wake-up circuit is powered down. No remote wake-up functionality is possible. LIN bus enters into recessive state. The system goes out of this mode to normal mode after the time-out of an internal counter delay (T_{shd}). Normal mode to temporary shutdown transition will be controller by register bit in configuration register.

7.2.5 Thermal Shutdown State

If the junction temperature TJ is higher than T_{sd}, the AS8520 will be switched into the thermal shutdown mode. The transceiver is completely disabled. No wake-up functionality is available. Window watchdog, TX timeout watchdog and LDO are completely turned off. Only the over-temperature monitor would be working. As soon as the temperature returns back to T_{ret}, the system enters normal mode. For more information on transition, see Table 14.

Table 14. Transition Table

Transition		Interface				Reg. 0x05 D0	Flags				
From mode	To mode	LIN	RX	TX	EN		rwake	Uvbat	OT	Uvcc	Comments
Normal Mode	Stand-By	X-RS	X-H[2]	H[3]	H-L[3]	L	X	X	inactive	inactive	TX is high for $T_{STNDY\_triggerr}$
	Sleep[1]	X-RS	X-H[2]	H[3]	H-L[3]	L	X	X	inactive	set	TX is high for $T_{STNDY\_triggerr}$[1]
	Temporary Shutdown	X-RS	X-H[2]	X	H[3]	H	X	X	inactive	set	The Control Bit is set through the 4-Wire SPI interface
	Over-Temperature	X-RS	X-H[2]	X	X	L	X	X	set	set	Temperature monitor output asserted (covered by scan)
Stand-By Mode	Normal (LW)	X	H-X[2]	X	L-H[3]	L	X	X	inactive	inactive	
	Normal (RW)	X	H-X[2]	H	X	L	set	X	inactive	inactive	Remote Wake up Event occurred on LIN
	Temporary Shutdown	RS	H[2]	H	L	H[3]	X	X	inactive	set	The Control Bit is set through the 4-Wire SPI interface
	Over-Temperature	RS	H[2]	H	L	L	X	X	set	set	Temperature monitor output asserted (covered by scan)

Table 14. Transition Table

Transition		Interface				Reg. 0x05 D0	Flags				
From mode	To mode	LIN	RX	TX	EN		rwake	Uvbat	OT	Uvcc	Comments
Temporary Shutdown Mode	Normal	RS-X	H-X[2]	X	X	L	X	X	inactive	clear	Internal 128ms timer expired
Over-Temperature Mode	Normal	RS-X	H-X[2]	X	X	L	X	X	clear	clear	Temperature monitor output de-asserted (covered by scan)
Sleep Mode[3]	Normal	RS-X	H-X[2]	X	X	L	set	X	inactive	clear	Remote Wake up Event occurred on LIN
	Over-Temperature	RS	H[2]	X	X	L	X	X	set	hold	Temperature monitor output asserted (covered by scan)
All States	Power Off	X	X	X	X	X	X	L-H[3]	X	X	

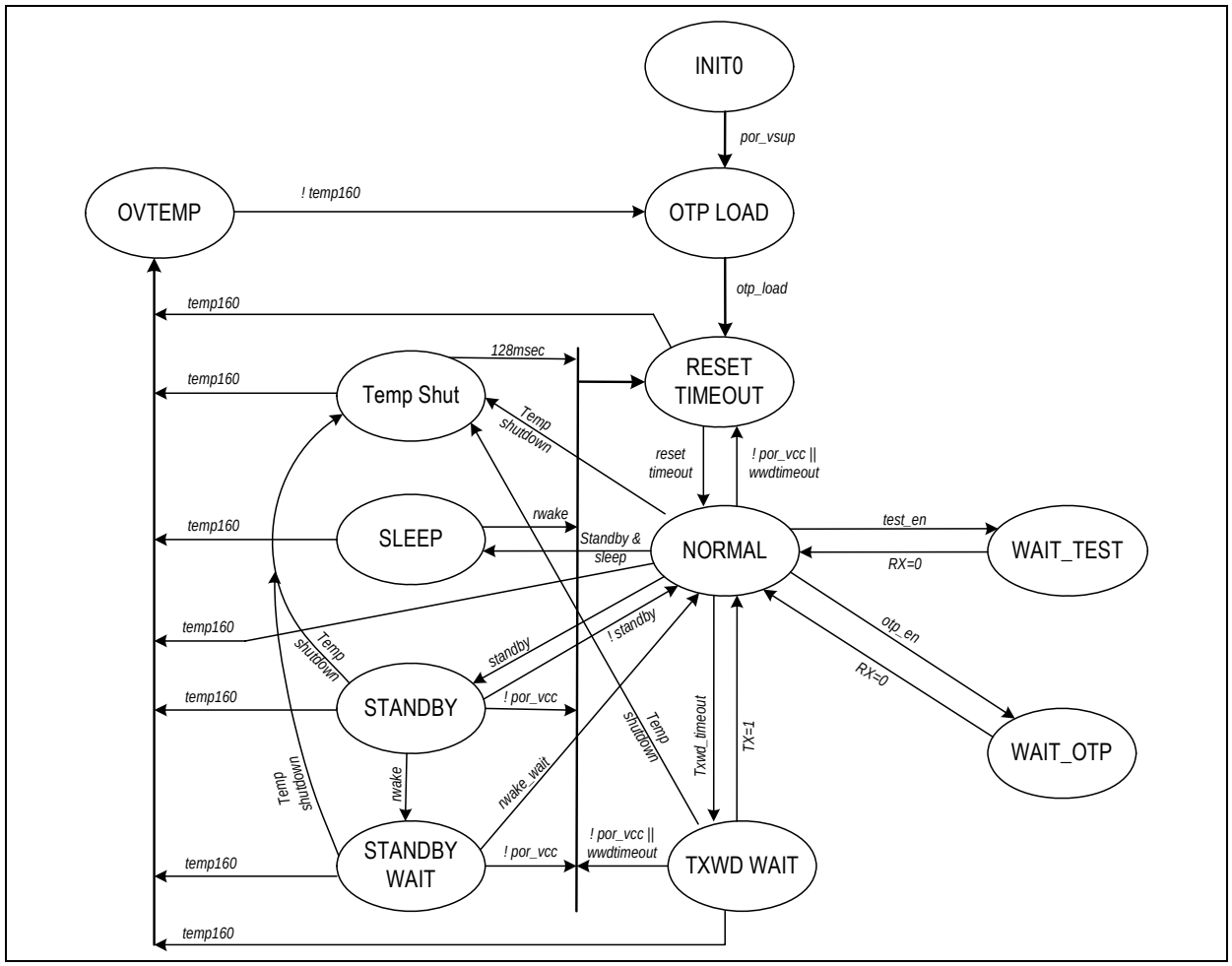
1. Chosen by factory programming option
2. Effect of Transition
3. Cause for Transition

Note: L = low state, H = high state, OT = Over-temperature Reset, Uvcc = Undervoltage Vcc, Uvbat = Undervoltage VBAT, rwake =remote wake, X = don't care.

7.3 State Diagram

The complete functional state machine for AS8520 is illustrated in Figure 6. Some soft-states in the FSM like “TXWD Wait”, “Standby Wait” and other “wait” states have been included for the sake of completeness.

Figure 6. Finite State Machine Model for the AS8520 System



8 Application Information

8.1 Initialization

When the power supply is switched on, if VSUP > VSUVR_OFF, RESET_VSUP_N becomes inactive (high). After this, the voltage regulator starts with a default LDO output setting of 3.3V and Vuvr_off setting of 2.75V. If VCC > Vuvr_off (2.75V), active-low PORN_2_OTP is generated. The rising edge of PORN_2_OTP loads contents of fuse onto the OTP latch after load access time T_{Load}. LOAD_OTP_IN_PREREG signal loads contents of OTP latch onto the pre-regulator domain register. This register gives actual settings of LDO, Vuvr_off and Reset Timeout period T_{Res}. This is done because the OTP block is powered by the VCC. If VCC > Vuvr_off (phase 2), Reset timeout is restarted. RESET signal is de-asserted after Reset Timeout period T_{Res} (phase 2) and then device enters into normal mode. The circuit also needs to initialize correctly for very slow ramp rates on VSUP (of the order of 0.5V/min).

Figure 7. Initialization Sequence for AS8520

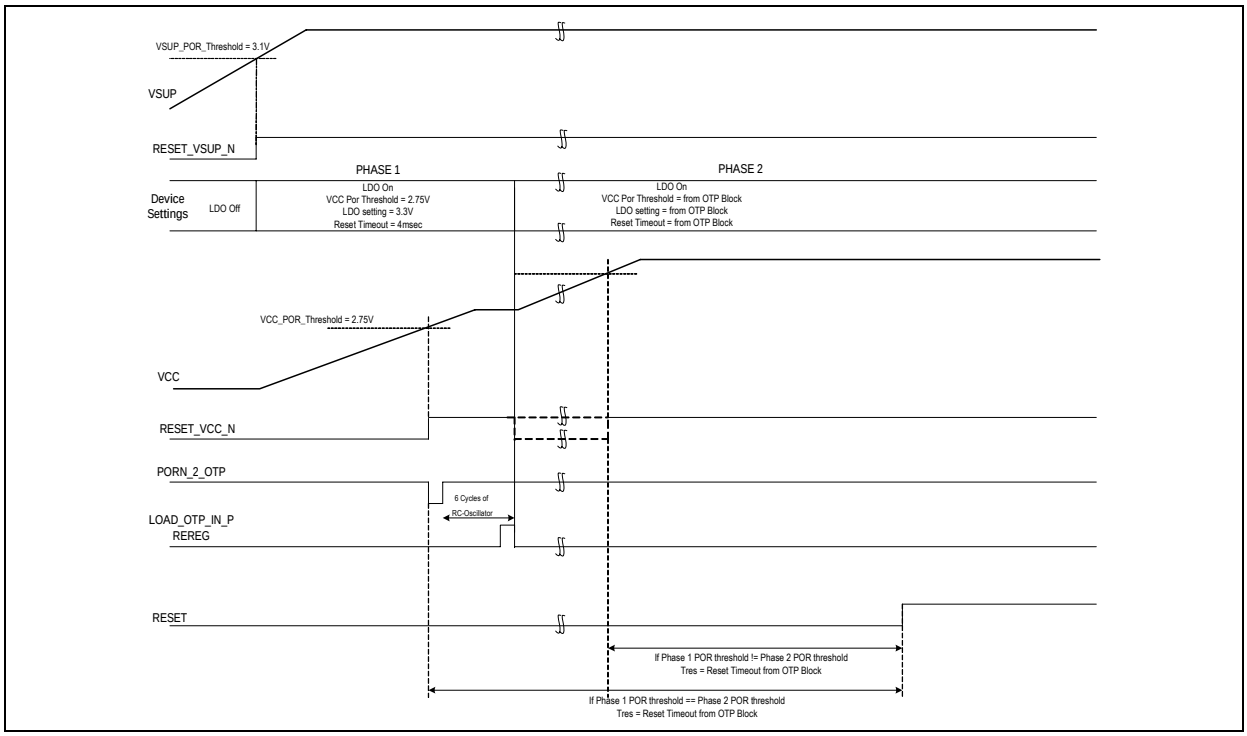


Table 15. VSUP>Vsuvr_on and VCC<Vuvr_on

Block	Output Signal
TRANSCEIVER = Enabled (disabled only during initial VSUP ramp-up)	LIN = high-z, RX = follows V
LDO = Enabled (disabled only during initial ramp-up)	VCC = low
RELAY DRIVER = Enabled	LDRIVE1 = high, LDRIVE2 = high
RESET = Enabled	RESET = high-z
RESISTIVE DIVIDER = Enabled	VBAT= high, VBAT_DIV = enabled

Table 16. VSUP<Vsuvr_on

Block	Output Signal
TRANSCEIVER = Disabled	LIN = high-z, RX = high-z
LDO = Disabled	VCC = low
RELAY DRIVER = Disabled	LDRIVE1 = high, LDRIVE2 = high

Table 16. VSUP<Vsuvr_on

Block	Output Signal
RESET = Disabled	RESET = high-z
RESISTIVE DIVIDER = Disabled	VBAT = high, VBAT_DIV = low

8.2 Wake-Up

If the regulator is put into sleep/standby mode, it can be woken up with the BUS interface. A transition on the BUS (high to low) with a minimum predefined low time (t_{wake}) puts the regulator into normal mode.

8.3 Over-Temperature Shutdown

If the junction temperature increases beyond T_{sd} the over-temperature recognition will be activated and the regulator voltage will be switched off. The VCC voltage drops down, the reset state is entered and the bus transceiver is switched off (recessive state). After TJ falls below T_{ret}, the AS8520 will be initialized again. This initialization starts independently from the voltage levels on EN and BUS. Within the thermal shutdown mode, the transceiver cannot switch to the normal mode either with local or with remote wake-up. The operation of the AS8520 is possible between TJ (125ºC) and the switch off temperature T_{sd}, but small parameter differences can appear. After over-temperature switch-off, the IC initializes as explained in Initialization on page 20. The low slew mode for LIN Transceiver has to be selected again on re-initialization, if necessary.

8.4 LIN BUS Transceiver

The AS8520 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller. The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a de-bouncing unit.

8.4.1 Transmit Mode

During transmission the data at the pin TX will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:

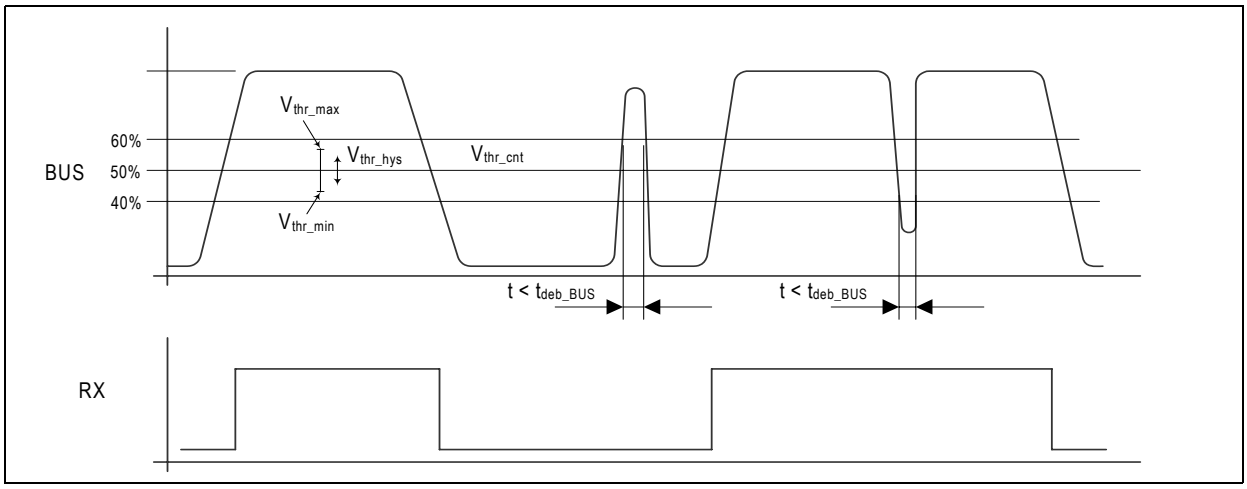
- Sleep mode
- Thermal Shutdown active
- Master Reset (VSUP < Vsuvr_on)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS (VBUS>VSUP). No additional termination resistor is necessary to use the AS8520 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

8.4.2 Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin RX. Short spikes on the bus signal are suppressed by the implemented de-bouncing circuit. Including all tolerances the LIN specific receive threshold values of 0.4*VSUP and 0.6*VSUP will be securely observed.

Figure 8. Receive Mode Impulse Diagram

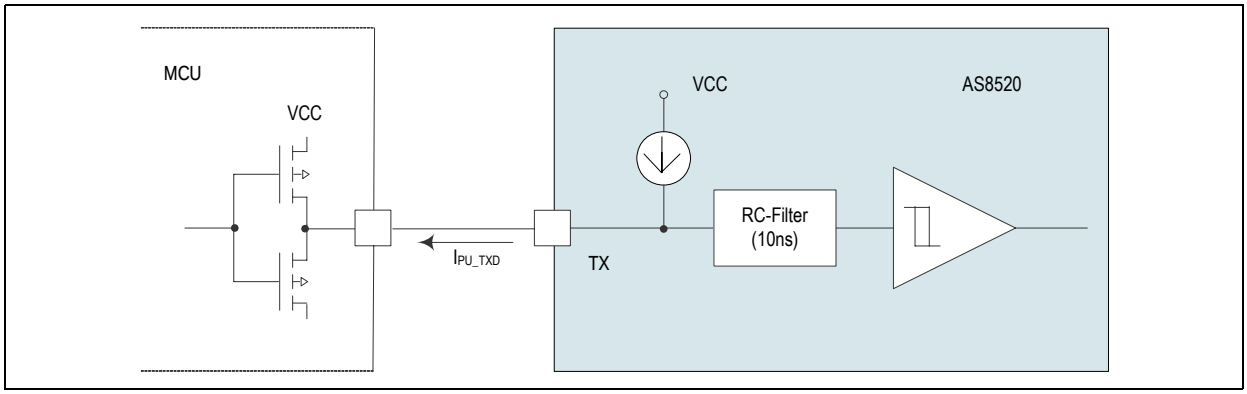


8.5 RX and TX Interface

8.5.1 Input TX

The 5V input TX controls directly the BUS level. LIN Transmitter acts like a slew-controlled level shifter. A dominant state (low) on TX leads to the LIN bus being pulled low (dominant state) too. The TX pin has an internal active pull up connected to VCC. This guarantees that an open TX pin generates a recessive BUS level.

Figure 9. TX Input Circuitry



8.5.2 Output RX

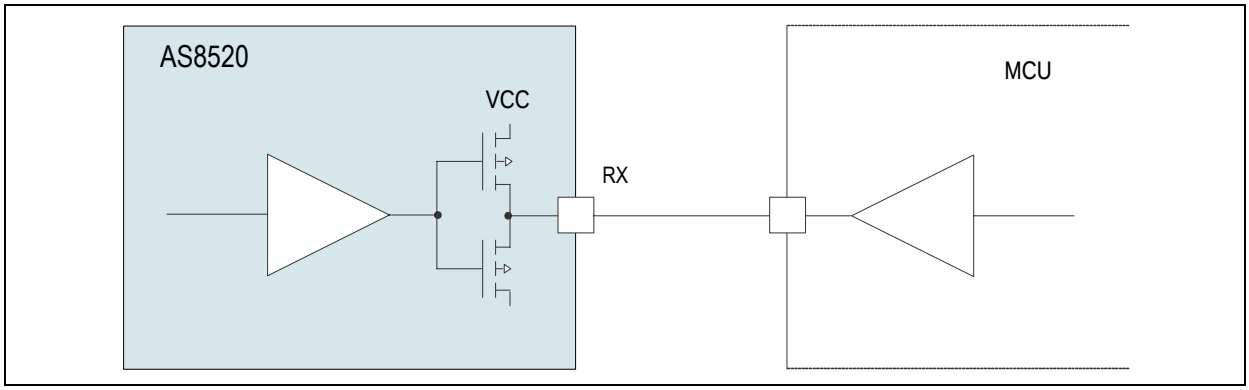
The received BUS signal will be output to the RX pin:

BUS < Vthr_cnt – 0.5 * Vthr_hys → RX = low

BUS > Vthr_cnt + 0.5 * Vthr_hys → RX = high

This output is a push-pull driver between VCC and GND with an output current of 1mA.

Figure 10. RX Output Circuitry

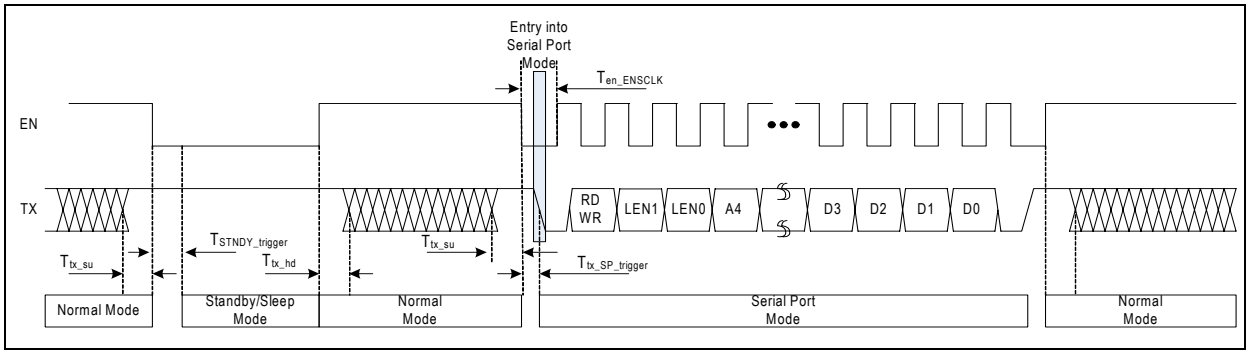


8.6 MODE Input EN

The AS8520 is switched from normal mode to the standby/sleep mode with a falling edge on EN and keeping TX high for $T_{STNDY\_trigger}$ time. Device is switched from standby mode to normal mode with a rising edge at the EN pin. The mode change for AS8520 with a falling edge at EN can be done independently from the state of the bus transceiver. Device enters into Serial port mode (for factory test purpose only) by forcing EN low and driving TX high to low within $T_{tx\_SP\_trigger}$ time after EN forced to low.

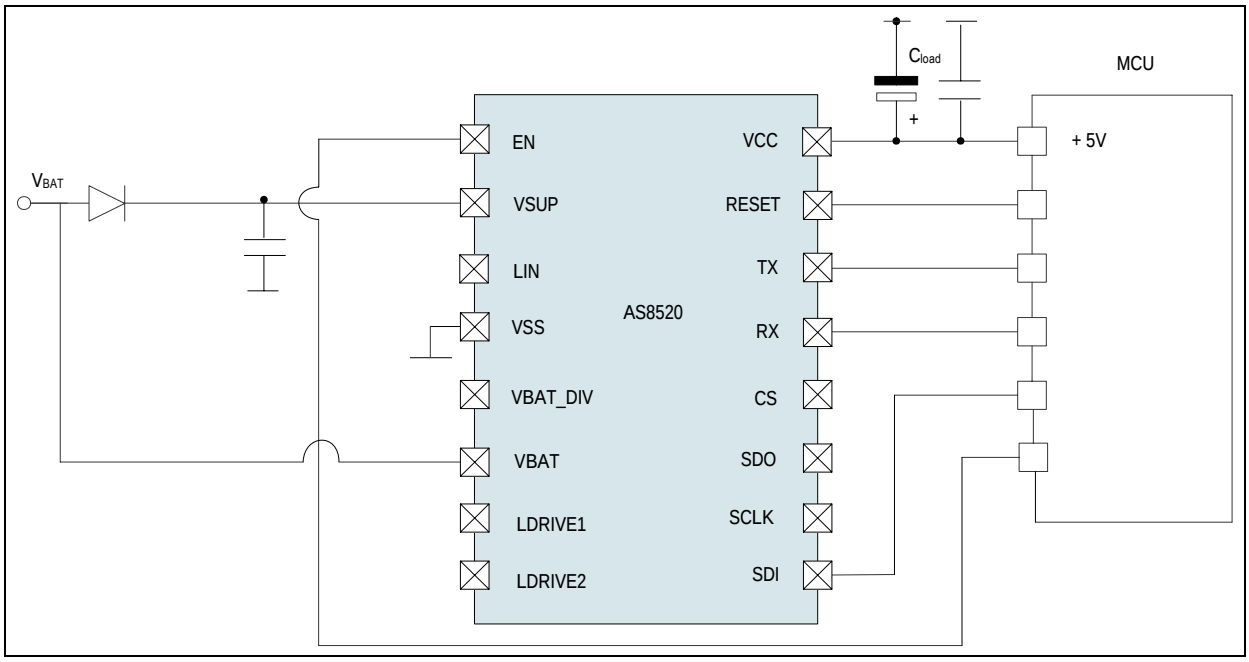
This ensures the direct control of device to enter into Standby/Sleep mode by microcontroller using EN pin.

Figure 11. EN Pin Functionality



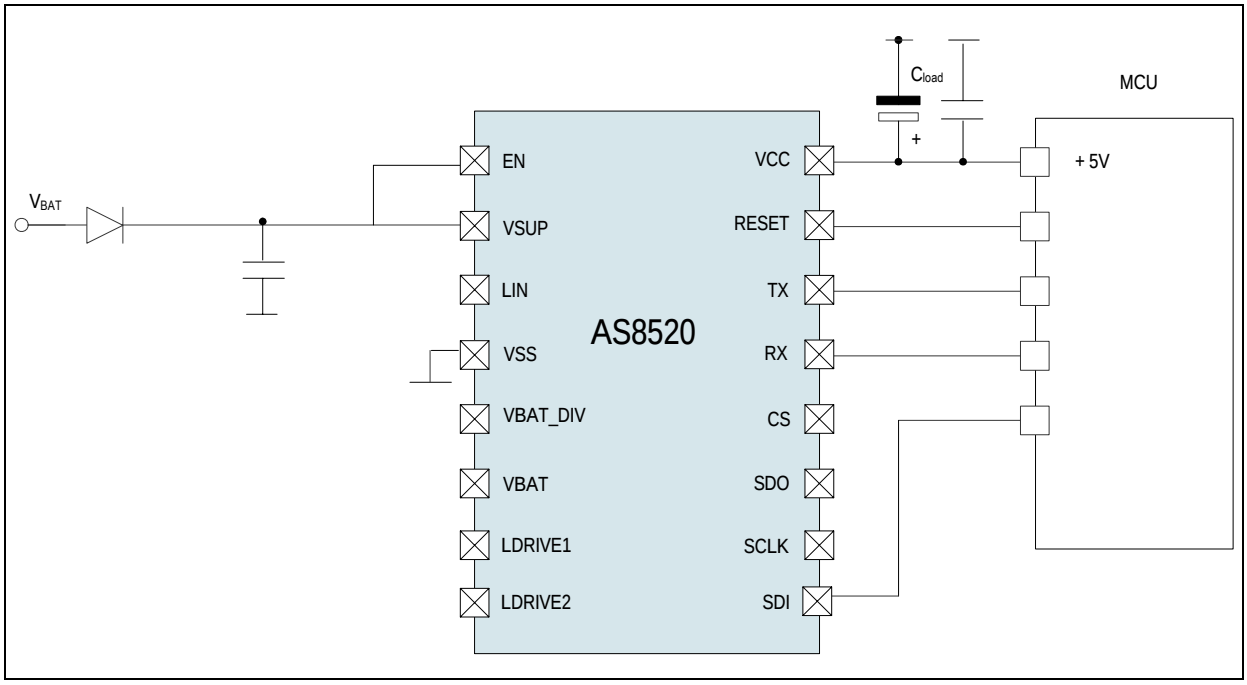
The EN input has an internal active pull down to secure that if this pin is not connected, a low level will be generated.

Figure 12. Enable Controlled via. MCU



If the application doesn't need the wake up capability of the AS8520, a direct connection EN to VCC is possible. In this case the AS8520 operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via. VSUP signal as shown below.

Figure 13. Permanent Normal Mode



8.7 Serial Port Interface

The 4-wire interface is essentially used to control the relay driver, to shutdown LDO temporarily and to trigger the window watchdog. It is also used to access test mode and read out diagnostic information for the AS8520. The description of this interface and the protocol is explained below. Information on block status and errors can be displayed by diagnosis registers.

8.7.1 Device Configuration using 4-Wire Serial Port

The SPI interface can be used as interface between the AS8520 and an external microcontroller to configure the device and access the status information. The interface is a slave and then only the microcontroller can start the communication. The SPI protocol is very simple and the length of each frame is an integer multiple of byte except when a transmission is started. Basically each frame has 1 command bit, 5 address/ configuration bits, 1 or more data bytes. SPI clock polarity settings depend on the value of the SCLK on the CS falling edge. This setting is done on each start of the SPI transaction. During the transaction, the SPI clock polarity will be fixed to the settings done. On the CS falling edge, the values on SCLK signal decide setting of the active SPI clock edge for data transfer. (see table below)

Table 17. CS and SCLK

CS	SCLK	Description
FALL	LOW	Serial data transferred on rising edge of SPI clock. Sampled at falling edge of SPI clock.
FALL	HIGH	Serial data transferred on falling edge of SPI clock. Sampled at rising edge of SPI clock.
ANY	ANY	Serial data transfer edge is unchanged.

8.7.1.1 SPI Frame

A frame is formed by a first byte for command and address/configuration and a following bit stream that can be formed by an integer number of bytes. Command is coded on the 1 first bit, while address is given on LSB 5 bits. (see table below)

Table 18. Command Bits

Command Bits			Register Address or Transmission Configuration				
C0	Reserved	Reserved	A4	A3	A2	A1	A0

C0	Command	<A4:A0>	Description
0	WRITE	ADDRESS	Writes data byte on the given starting address.
1	READ	ADDRESS	Read data byte from the given starting address.

If the command is read or write, one or more bytes follow. When the micro-controller sends more bytes (keeping CS LOW and SCLK toggling), the SPI interface increments the address of the previous data byte and writes/reads data to/from consecutive addresses.

8.7.1.2 Write Command

For Write command C0 = 0.

After the command code C0 and two reserved bits, the address of register to be written has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred, always from the MSB to the LSB. For each data byte following the first one, used address is the incremented value of the previously written address. Each bit of the frame has to be driven by the SPI master on the SPI clock transfer edge and the SPI slave on the next SPI clock edge samples it. These edges are selected as per Table 17. The following figures illustrate two examples of write command (without and with address self-increment.)

Figure 14. Protocol for Serial Data Write with Length = 1

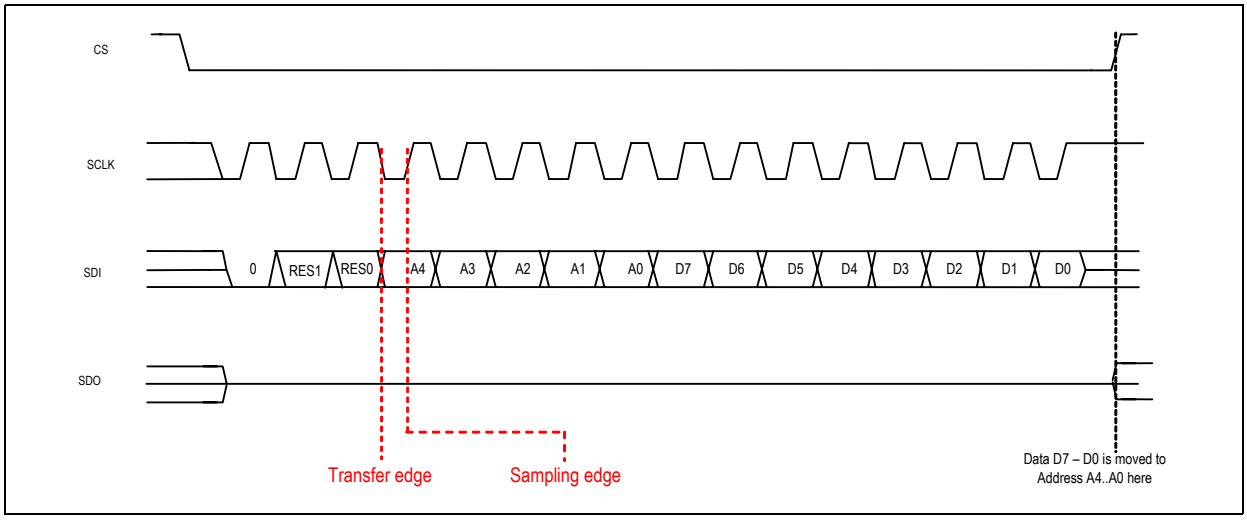
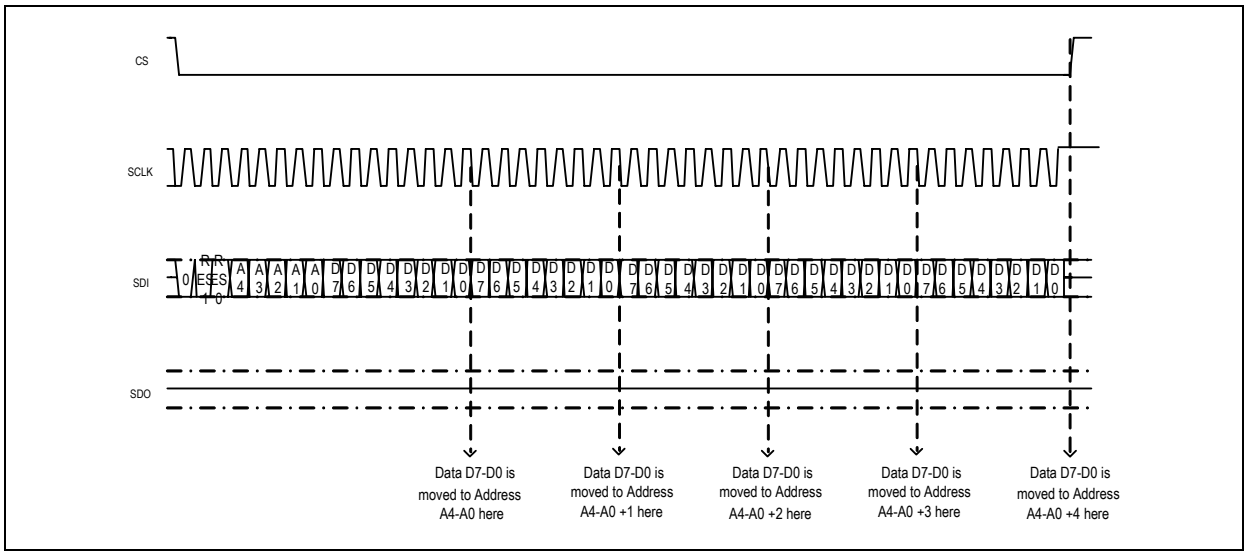


Figure 15. Protocol for Serial Data Write with Length = 4



8.7.1.3 Read Command

For Read command C0 = 1.

After the command code C0 and two reserved bits, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB. To transfer more bytes from consecutive addresses, SPI master has to keep active the SPI CS signal and the SPI clock as long as it desires to read data from the slave. Each bit of the command and address sections of the frame have to be driven by the SPI master on the SPI clock transfer edge and the SPI slave on the next SPI clock edge samples it. Each bit of the data section of the frame has to be driven by the SPI slave on the SPI clock transfer edge and the SPI master on the next SPI clock edge samples it. These edges are selected as per Table 17. The following figures illustrate two examples of read command (without and with address self-increment.)

Figure 16. Protocol for Serial Data Read with Length = 1

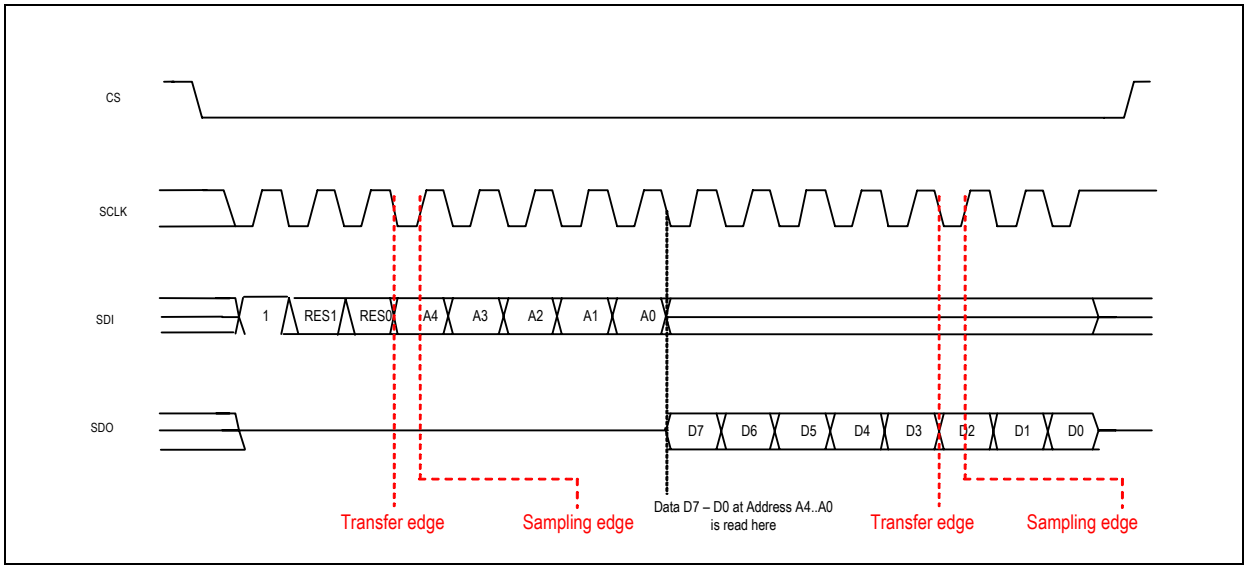
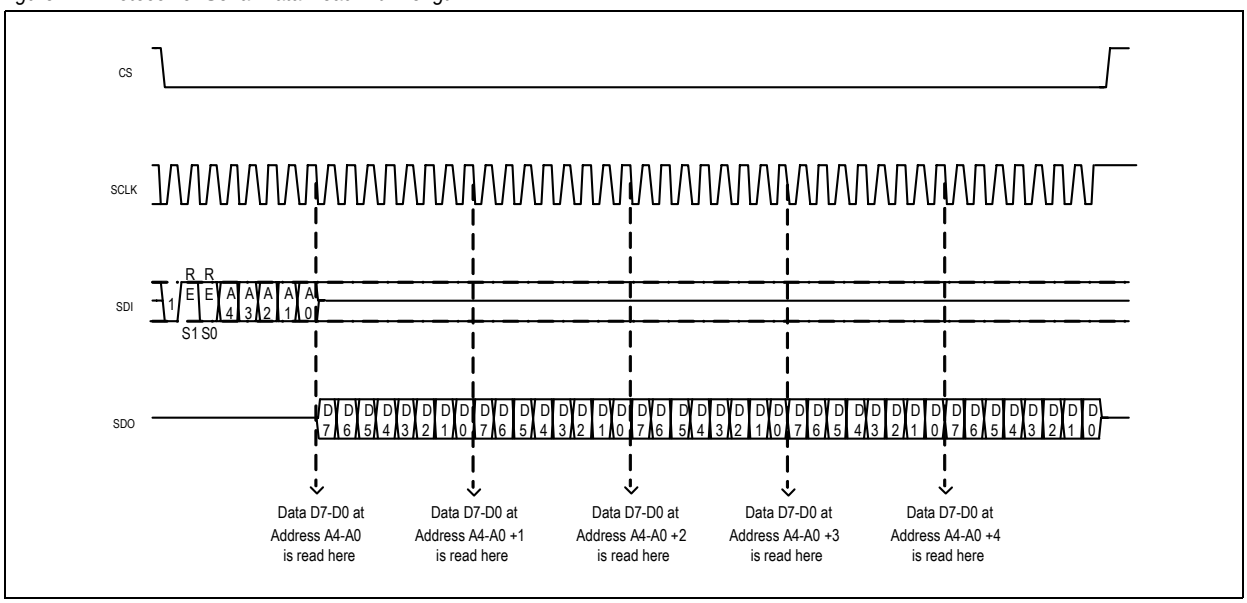


Figure 17. Protocol for Serial Data Read with Length = 4



8.7.1.4 Timing

The following figures illustrate timing waveforms and parameters.

Figure 18. Timing for Writing

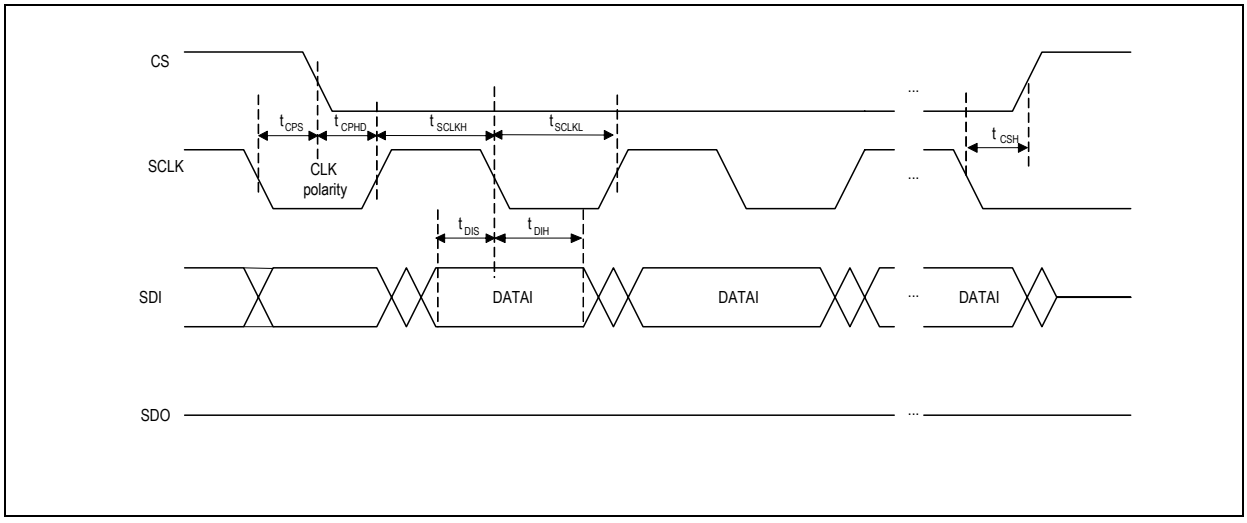
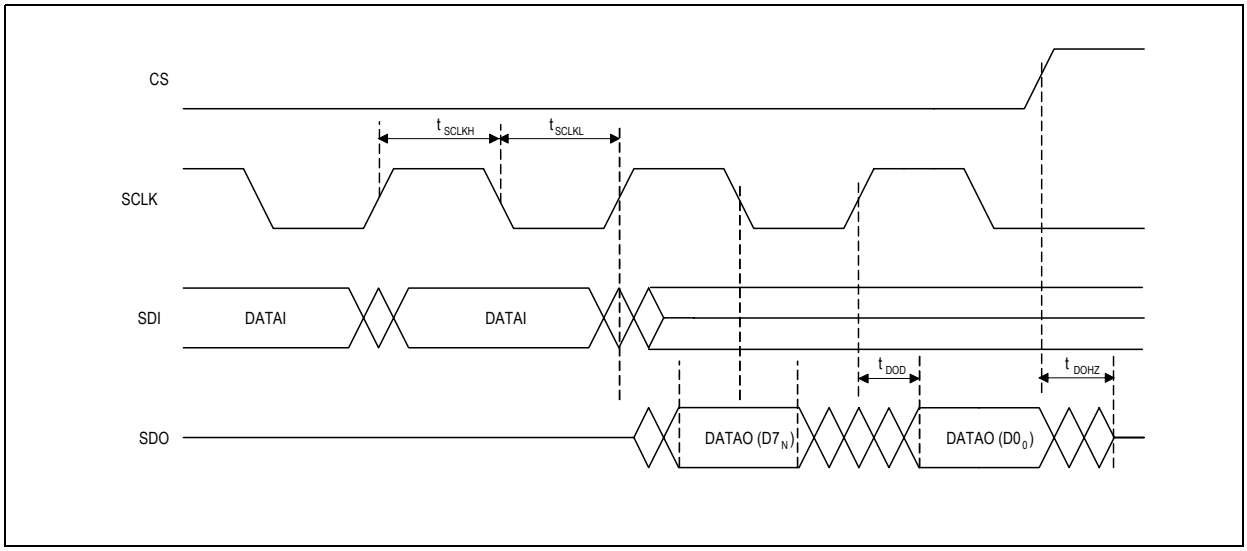


Figure 19. Timing for Reading



8.8 Control and Diagnosis Registers

The serial interface can be used as interface between the ASSP AS8520 and an external micro-controller. The interface is a slave and only the micro-controller can start the communication. This interface will be used for device configuration, entering into test mode and carrying out diagnostic options. Refer to Table 19 for details on the configuration registers.

8.8.1 Definition of Control and Status Registers

A total of 32 control, diagnosis and test registers, each of 8-bit can be accessed using the 4-wire serial interface. Table 19 provides a description of all control and status registers.

Table 19. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description	
Control and Configuration Register						
0 x 02	OTP Interface Control Register	On POR_VCC 0000_0000	b[7:1]	R/W	Reserved	
			b[0]		OTP feature is only for factory use!	
					0	OTP interface is disabled.
					1	OTP interface is enabled. When this bit is set, EN, TX, RX are used as OTP interface pads. These pads can be used for OTP programming. OTP interface is disabled on seeing high to low transition on RX (MODE).
0 x 03	Device Configuration Register	On POR_VCC 0000_1011	b[7:4]	R/W	Reserved	
			b[3]		0	LIN Transceiver disabled
					1	LIN Transceiver enabled
			b[2]		0	Over-Temperature Monitor disabled
					1	Over-Temperature Monitor enabled
			b[1]		0	Low side Driver2 disabled
					1	Low side Driver2 enabled
			b[0]		0	Low side Driver1 disabled
					1	Low side Driver1 enabled
0 x 04	Device Control Register	On POR_VSUP 0000_0001	b[7:1]	R/W	Reserved	
			b[0]		Slew control	
					0	Low Slew Mode
					1	High Slew mode
0 x 05	Temporary Shutdown Register	On POR_VCC 0000_0000	b[7:1]	R/W	Reserved	
			b[0]		Temporary shutdown control bit	
					0	No Temporary shutdown
					1	Enter into Temporary shutdown
0 x 06	Window Watch Dog Trigger Register	On POR_VCC 0000_0000	b[7:1]	W	Reserved	
			b[0]		Window Watch Dog Trigger. This bit will be set by MCU to indicate trigger event. If this trigger occurs outside the Window of Watchdog counter, then RESET signal is asserted. Also on this trigger WWD counter is restarted and this bit will be cleared internally within 2 cycles of 128KHz clock.	
0 x 07	Low Side Driver Data Register	On POR_VCC 0000_0000	b[7:2]	R/W	Reserved	
			b[1]		This bit is Data input to Low Side Driver 2 gate input	
			b[0]		This bit is Data input to Low Side Driver 1 gate input	

Table 19. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description
Diagnosis Register					
0 x 08	Diagnostic Register 1	On POR_VSUP 0000_001		R	b[7:0] are 8 LSB bits of the 24 bit Diagnostic Register
			b[7]		WWDT Window watchdog timeout (set on failure of Window watchdog timeout, cleared after µC read
			b[6]		RWAKE Remote Wakeup (set on Remote Wakeup event on LIN Bus, cleared after µC read)
			b[5]		Reserved
			b[4]		OVVBAT Overvoltage VBAT (set when VSUP > Vovthh, cleared after µC read)
			b[3]		OTEMP140 Over-temperature warning (set when temp > Totset, cleared after µC read)
			b[2]		OTEMP160 Over-temperature Reset (set when temp > Tsd, cleared after µC read)
			b[1]		UVVCC Undervoltage Vcc (set when Vcc < Vuvr_on, cleared after µC read)
			b[0]		PORVSUP (set when VSUP < Vsuvr_on, cleared after µC read)
0 x 09	Diagnostic Register 2	On POR_VSUP 0000_0000		R	b[7:0] = DR[15:8] Next 8 LSB bits of the 24 bit Diagnostic Register.
			b[7:2]		Reserved
			b[1]		TEMPSHUT this bit is set on entering into temporary shutdown state and cleared after µC read.
			b[0]		TXTIMEOUT Tx timeout of 1sec (set on TX low > 1sec, cleared after µC read)
0 x 0A					Reserved
0 x 0B					Reserved
0 x 0C					Reserved
0 x 0D					Reserved
0 x 0E					Reserved
0 x 0F					Reserved
0 x 10	Backup Register 1	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.
0 x 11	Backup Register 2	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.
0 x 12	Backup Register 3	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.
0 x 13	Backup Register 4	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.
0 x 14	Backup Register 5	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.
0 x 15	Backup Register 6	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.

Table 19. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description
0 x 16	Backup Register 7	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.
0 x 17	Backup Register 8	On POR_VSUP 0000_0000	b[7:0]	R/W	This can be used to store configuration/status data during Sleep mode.

8.9 ESD/EMC REMARKS

8.9.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

8.9.2 ESD-Test

The AS8520 is tested according CDF-AEC-Q100-002 / MIL883-3015.7 (human body model), IEC 61000-4-2, JESD22-C101/ AEC-Q100-011, JESD22-A115/AEC-Q100-003.

8.9.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data and signal pins.

9 Package Drawings and Markings

The device is available in a 24-pin QFN (6x6) package.

Figure 20. Package Drawings

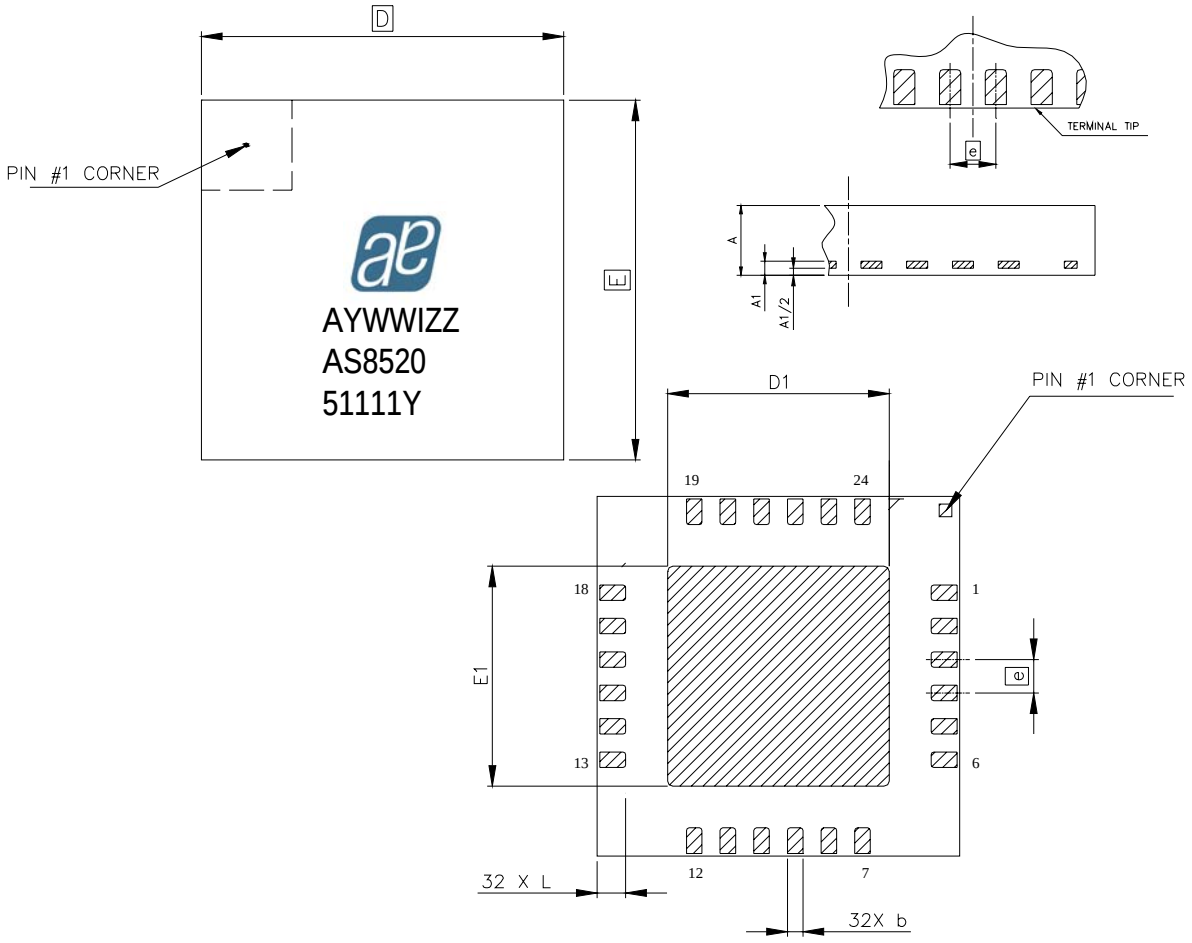


Table 20. Package Dimensions

Symbol	mm		
	Min	Typ	Max
D		6	
E		6	
D1	4.40	4.50	4.60
E1	4.4	4.50	4.60
L	0.35	0.40	0.45
b	0.25	0.30	0.35
e		0.65	
A	0.80	0.85	0.9
A1		0.203	

Revision History

Table 21. Revision History

Revision	Date	Owner	Description

10 Ordering Information

The devices are available as the standard products shown in Table 22.

Table 22. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS8520-AQFT	Vcc = 5V	Tape & Reel	24-pin QFN (6x6)

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
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