AS8525

LIN Transceiver with Voltage Regulators, Programmable Gain High Side Amplifier, and Voltage Attenuator

1 General Description

The AS8525 is a companion IC for automotive battery sensor systems for both low-side and high-side current sensing applications.

The device provides two regulated 3.3V supplies from the battery supply, attenuated battery voltage in differential form, and amplified version of a high-side current-sense element's voltage with a translated common-mode voltage. The device also communicates the system output to a LIN bus.

AS8525 is designed in a high-voltage 0.35µm CMOS process and packaged on QFN-32.

2 Key Features

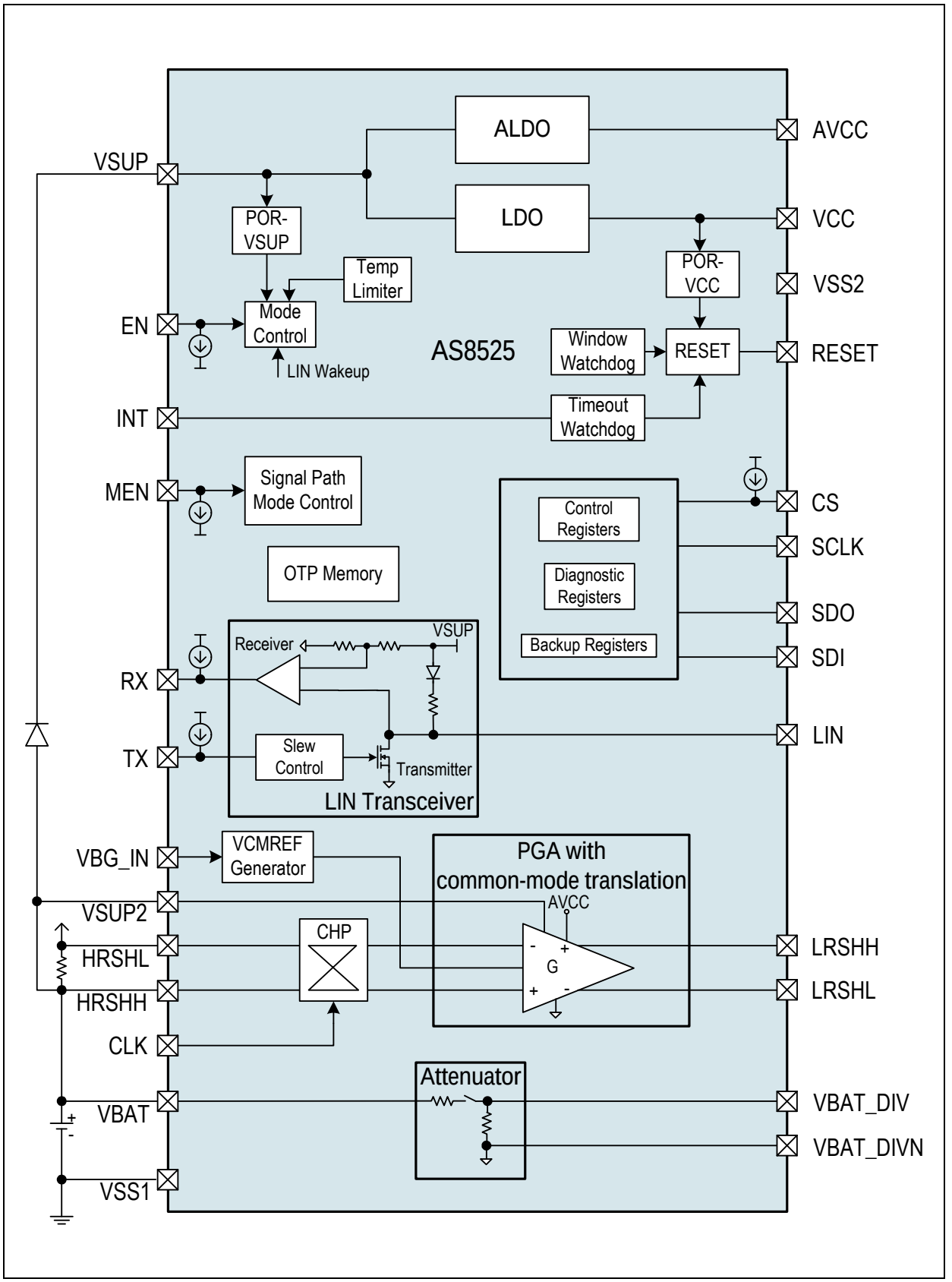
- Operating voltage 4.3V to 18V, max. 42V for 500 ms
- Two linear low-drop voltage regulators: VCC = 3.3V with 50mA drive capability
- Typical 50µA quiescent current in standby mode
- Typical 35µA quiescent current in sleep mode
- Precision voltage attenuator with power down facility
  - 0.05% ratio drift accuracy and disable
- Precision fully-differential programmable gain amplifier (PGA)
  - High-voltage to low-voltage common-mode translation
  - Gain steps 5, 25, 50, 100
- LIN bus transceiver
  - Load independent slew control conforming to LIN 2.1
  - Short circuit protection
  - TX time out fail safe feature
  - Over temperature warning and shut down
- Power-On Reset with OTP adjustable reset timeout and brown-out detection
- Over temperature warning & shutdown functions
- Operating modes: Normal, Standby, Sleep, Temporary shut down
- Microcontroller 4-wire interface
- RC oscillator and programmable timer
- Optional window watchdog in normal mode and time-out watchdog in standby mode
- 8 backup registers to store MCU data during VCC shut down
- Load dump protection for all battery supplied pins, LIN bus pin and Enable pin
- Internal reverse polarity protection (up to -27V) for all battery-sensing pins and LIN bus pin
- Chip ID for traceability
- -40ºC to +115ºC ambient operating temperature
- 32-pin QFN (5x5) package

3 Applications

The AS8525 is suitable for LIN networked 14V battery sensor slaves for current measurement in positive battery power rail (high side) or in minus rail (PGA is left un-used in that case).

The device is also ideal for general purpose system basis chip for actuator LIN slaves with battery voltage sensing and actuator high side current sensing.

Figure 1. AS8525 Block Diagram



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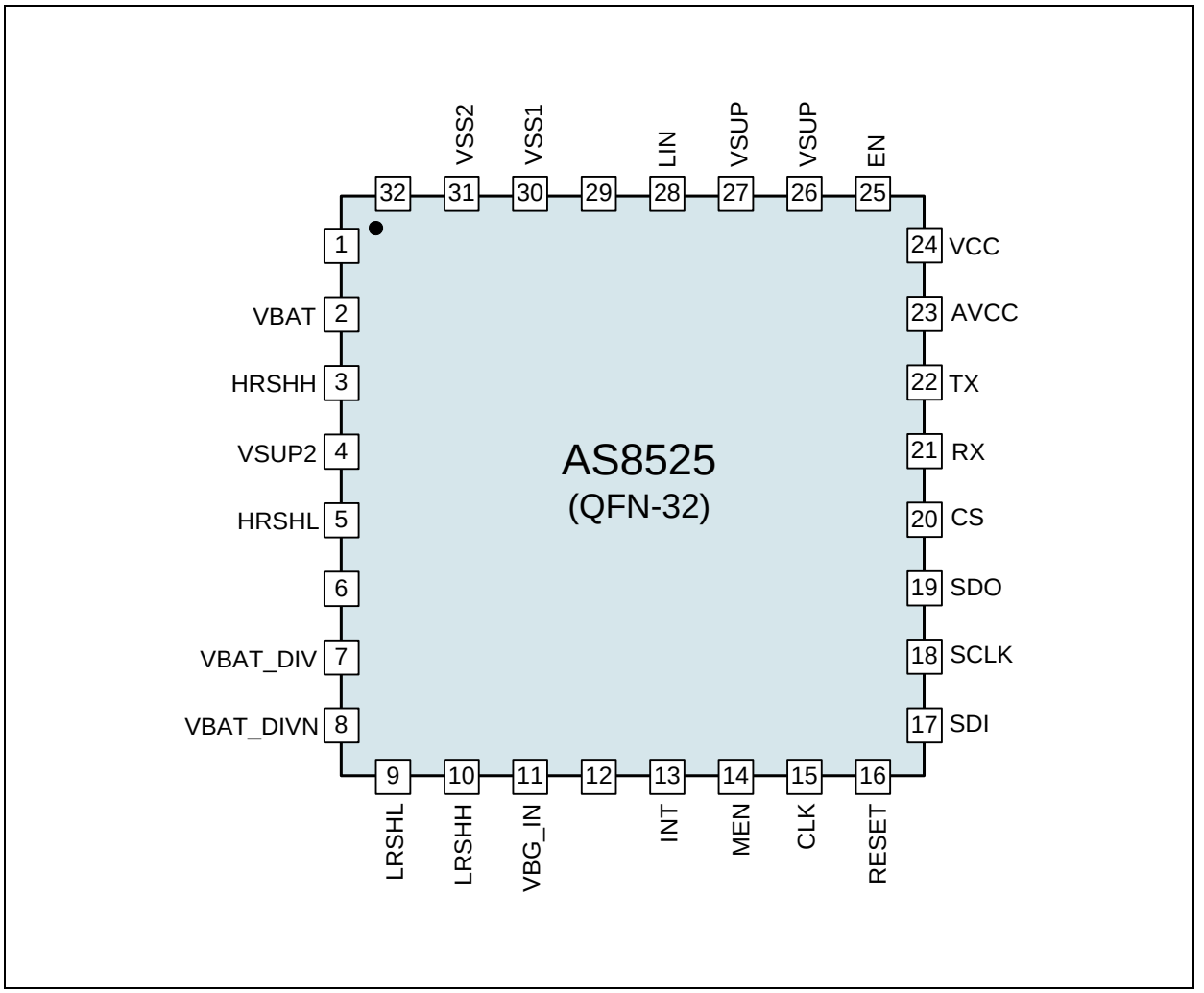
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
NC	1	Not connected	
VBAT	2	Analog Input	Battery voltage input
HRSHH	3		Battery-side connection to high-side current-sense element
VSUP2	4	Supply	Supply input for the high-side amplifier
HRSHL	5	Analog Input	Load-side connection to high-side current-sense element
NC	6	Not connected	
VBAT_DIV	7	Analog Output	Attenuated battery voltage output (differential)
VBAT_DIVN	8		
LRSHL	9		Gained current-sense element voltage output with translated common-mode voltage (differential)
LRSHH	10		

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
VBG_IN	11	Analog Input	Low noise Bandgap reference voltage input
NC	12	Not connected	
INT	13	Digital Input	Reference input for time-out Watchdog in the device standby mode
MEN	14	Digital I/O with Pull-Down	Enable input for analog signal paths in the device standby mode
CLK	15	Digital Input with Pull-Down	Chopper clock input
RESET	16	Digital Output	Reset output (active low)
SDI	17	Digital Input	Serial data in
SCLK	18		Serial clock
SDO	19	Digital Output / Tristate	Serial data out
CS	20	Digital Input with Pull-Up	Chip select
RX	21	Digital I/O with Pull-Up	LIN transceiver receive pin
TX	22		LIN transceiver transmit pin
AVCC	23	Supply	Regulated 3.3V regulated output supply-2 for loads up to 50mA **Note:** The OTP selection option is common for VCC & AVCC
VCC	24		Regulated 3.3V regulated output supply-1 for loads up to 50mA
EN	25	Digital Input with Pull-Down	Enable input
VSUP	26	Supply	Supply input from battery (through external reverse polarity protection device)
	27		
LIN	28	Analog Input / Output	LIN bus
NC	29	Not connected	
VSS1	30	Ground	Ground
VSS2	31		Ground (VCC and AVCC are generated with reference to this ground)
NC	32	Not connected	

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
VSUP	Supply voltages	-0.3		42	V	Maximum allowed potential difference between any two pins in the set HRSHH, HRSHL and VSUP2 is 0.3V
VSUP2		-27		42		
VBAT, HRSHH, HRSHL	Battery voltage inputs	-27		42	V	
EN	Enable input	-0.3		42	V	
VCC, AVCC	Regulated output supplies	-0.3		7	V	
LIN	LIN bus	-27		40	V	
	Analog & digital inputs and outputs	-0.3		7	V	
I_{scr}	Input current (latchup immunity)	-100		100	mA	Norm: AEC-Q100
ESD	Electrostatic Discharge[1] Norm: AEC-Q100	±2			kV	For VCC, AVCC, TX, RX, Reset, CS, SCLK, SDO, SDI, EN, VBAT_DIV, VBAT_DIVN, LRSHH, LRSHL, VBG_IN, CLK, INT, MEN, VSUP2, HRSHH and HRSHL
		±4				VSUP, VBAT Short of VSUP2, HRSHH and HRSHL (shorted by shunt)
		±8				LIN to VSS1, HBM Model
		±6				LIN to VSS1, IEC6100-4-2
		±0.5				LIN to VSS1, CDM
		±0.1				LIN to VSS1, MM
P_{tot}[2]	Total operating power dissipation (all supplies and outputs)			500	mW	QFN 32 in still air, soldered on JEDEC standard board @115º ambient, static operation = no time limit
R_o	Package thermal resistance		25		ºC/W	
T_{stg}	Storage temperature	-55		+150	ºC	
T_{body}	Package body temperature			+260	ºC	The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages in matte tim (100% Sn).
	Humidity non-condensing	5		85	%	
MSL	Moisture Sensitive Level	3				Represents a maximum floor time of 168h

1. ESD Human Body model: R=1500Ω and C=150pF
2. Total power dissipation cannot exceed 0.500W to avoid increase in junction temperature, i.e. greater than 130ºC. VCC LDO can supply current externally, which is not greater than 15mA at 18V VSUP and 18mA at 16V VSUP. AVCC LDO can supply current externally, which is not greater than 10mA at 18V VSUP and 12mA at 16V VSUP.

6 Electrical Characteristics

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP	Supply voltages	Regulators after power-on reset	4.3		18	V
		Regulators for power-on reset	6			
VSUP2			4.5		18	V
VBAT, HRSHH, HRSHL	Battery voltage inputs		4.5		18	V
ΔVHiSide	Difference between any two pins in the set HRSHH, HRSHL and VSUP2				±0.2	V
LIN	LIN bus		0		18	V
EN	Enable input		0		18	V
VCC, AVCC	Regulated output supplies		0		3.6	V
ΔVCC	Difference in regulated supplies				±0.2	V
VBG_IN	Bandgap reference input		0		1.32	V
	Analog & digital inputs and outputs		0		3.6	V
T_{AMB}	Ambient temperature	Maximum junction temperature (T_J)=130ºC	-40		+115	ºC
I_{sup}	Supply Current	Though the two regulators are individually capable of 50mA, the total current is limited.			65	mA

6.1 Characteristics of Digital Inputs and Outputs

All pull-up, pull-downs have been implemented with active devices. RX, SDO, RESET have been measured with 100pF load.

Table 4. Characteristics of Digital Inputs and Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EN Input						
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current	EN=VSS	-1		+1	µA
I_{pd_en}	Pull down current	EN=VCC	30		100	µA
TX, CS, INT Inputs						
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current	TX=VCC	-1		+1	µA
Ipu	Pull up current	TX,CS, INTN pulled down to VSS	-30		-100	µA
CLK, MEN Inputs						
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current		-1		+1	µA
I_{pd_spi}	Pull down current	CLK, MEN pulled up to VCC	30		100	µA
SDI, SCLK						
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current		-1		+1	µA

Table 4. Characteristics of Digital Inputs and Outputs (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RX Output						
V_{OH}	High level output voltage					V
V_{OL}	Low level output voltage	I_{OUT} = 1mA, VSUP ≥ 6V			VSS+0.4	V
I_{pu_reset}	Pull-up current	Pulled down to VSS			-100	µA
SDO, RESET Output						
V_{OH}	High level output voltage					V
V_{OL}	Low level output voltage	VSUP ≥ 6V			VSS+0.4	V

6.2 Detailed System and Block Specifications

Table 5. System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Ivsupnom	Current consumption normal mode	No load on VCC, AVCC, LIN bus in recessive state, Current sense channel ON		850		µA
Ivbatnom				60		
Ivsup2nom		Current sense channel ON		600		
Ivsupstdby	Current consumption standby / sleep mode	No load on VCC, AVCC, LIN bus in recessive state		40		µA
Ivsupsleep				30		
Ivbatoff		Voltage sense channel OFF			2	
Ivsup2off		Current sense channel OFF			5	

6.2.1 Programmable Gain Amplifier (PGA)

Table 6. Programmable Gain Amplifier (PGA)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G1	Gain	DC gain		5		V/V
G2				25		
G3				50		
G4				100		
V_{IN_AMP}	Input signal range	V(HRSHH)-V(HRSHL) Gx represents typical gain value (x=1,2,3,4) after Offset trimming			±0.18*5/ Gx	V
V_{ICM_AMP}	Input common-mode voltage	V(HRSHH), VSUP2	4.5	12	18	V
V_{OCM_AMP}	Output common-mode voltage	When AVCC=3.3V Only for information	1.5	1.65	1.8	V
$\varepsilon_{p1,G}$	Gain error	Temperature: -40 to +115ºC @ VSUP2 = 12V Post system calibration			±0.5	%
$\varepsilon_{p2,G}$		At room temperature V(HRSHH), VSUP2=12V Without system calibration			±5	%
T_{Settle_AMP}	Time for settling to within 0.05% final value	Includes the settling of chopper			45	µs
$f_{-3dB\ AMP}$	3-dB bandwidth	G1	650			kHz
		G2	250			
		G3	150			
		G4	75			
V_{NDin_AMP}	Input referred thermal noise density (rms)	This excludes 1/f noise Guaranteed by design		35		nV/√Hz
THD_{AMP}	Total harmonic distortion	Till 500Hz single-ended sinusoidal inputs (after offset trimming). Guaranteed by design	70			dB
C_{L_AMP}	Load capacitance	Single ended (Includes the capacitance presented by the pad and pin of the host chip)			100	pF
V_{BG_AMP}	Bandgap reference voltage	External low noise reference	1.176	1.2	1.224	V
V_{NDBG_AMP}	Bandgap reference thermal noise density	When noise bandwidth < signal bandwidth, take it as 200nV/√Hz (Noise Bandwidth / Signal Bandwidth)			200	nV/√Hz
V_{OSin_AMP}	Input referred offset before trimming	Refers to the standalone amplifier without chopper stabilization			±37.5	mV
V_{OSinT_AMP}	Input referred offset after trimming	Refers to the standalone amplifier without chopper stabilization; Only at room temperature			±1.5	mV

6.2.2 VCMREF Generator

Table 7. VCMREF Generator

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CMREF_AMP}	Common-mode reference voltage	When AVCC=3.3V	1.55	1.65	1.75	V

6.2.3 Voltage Attenuator

Table 8. Voltage Attenuator

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RDIV	Division ratio			481		V/V
		Factory option		21		
V_{BAT}	Input voltage range/ Battery voltage range		4.5	12	18	V
$\varepsilon_{p,RDIV}$	Ratio error	At room temperature, V_{BAT}=12V			±1	%
$\varepsilon_{dt1,RDIV}$	Ratio drift (w.r.t Temperature)	Temperature: -25 to +65ºC @VBAT = 12V		±0.05	0.1	%
$\varepsilon_{dt2,RDIV}$		Temperature: -40 to +115ºC @VBAT = 12V		0.1	0.2	

6.2.4 Voltage Regulators (LDO & ALDO)

Table 9. Voltage Regulators (LDO & ALDO)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP	Input Supply Voltage		4.3	12	18	V
VCC AVCC	Output Voltage Range		3.15	3.3	3.45	V
I_{LOAD}	LDO Load Current				50	mA
	ALDO Load Current		0.01		50	mA
ICC_SH	Output Short Circuit Current	Normal mode			250	mA
dVCC1	Line Regulation	ΔVCC / ΔVSUP for VSUP range			8	mV/V
LOREG	Load Regulation	ΔVCC / ΔICCn (0.5mA < I_{LOAD} < 50mA)			1	mV/mA
CL1	Output Capacitor1 LDO	Electrolytic	2.2		10	µF
ESR1			1		10	Ω
CL2	Output Capacitor2 LDO	Ceramic	100		220	nF
ESR2			0.02		1	Ω
CL1	Output Capacitor1 ALDO	Electrolytic	2.2		5	µF
ESR1			1		10	Ω
CL2	Output Capacitor2 ALDO	Ceramic	100		220	nF
ESR2			0.02		1	Ω

6.2.5 LIN Transceiver

Table 10. DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver						
I_{bus_lim}		Current limitation in Dominant State LIN=VSUP_max	40	120	200	mA
LIN_V_{OL}		Output Voltage BUS (dominant state), I_{LIN}=40mA (short-circuit condition tested at V_{OL}=2.5V)			2	V
	Pull-up resistor	Normal mode (recessive BUS level on TX pin)	20	40	60	kΩ
$I_{bus\_leak\_rec}$		Driver OFF; 7.3V < VSUP < 18; 8V < VBUS < 18, VSUP < VBUS < 1.08 * VSUP (to be tested at VBUS=18V)			20	µA
Receiver						
$I_{bus\_leak\_dom}$		Input Leakage current at receiver Driver OFF; Vbus=0V; VSUP=12V; VCC=3.3V	-1			mA
$I_{bus\_no\_GND}$		VSS=VSUP; VSUP=12V; 0V < VBUS < 18V, VCC=3.3V (to be tested at VBUS=18V)	-1		1	mA
$I_{bus\_no\_bat}$		VSUP=VSS; 0V < VBUS < 18V, VCC=VSS (to be tested at VBUS=18V)			100	µA
V_{bus_dom}					0.4	VSUP
V_{bus_rec}			0.6			VSUP
V_{bus_cnt}		$V_{bus\_cnt} = (V_{th\_dom} + V_{th\_rec})/2$[1]	0.475		0.525	VSUP
V_{hys}		$V_{hys} = (V_{th\_dom} - V_{th\_rec})$[1]	0.05		0.175	VSUP

1. V_{th_dom}: Receiver threshold of the recessive to dominant LIN bus edge,
   V_{th_rec}: Receiver threshold of the dominant to recessive LIN bus edge

Table 11. AC Electrical Characteristics

Symbol	Conditions	Min	Typ	Max	Units
LIN Driver, Bus load conditions (C_{BUS}; R_{BUS}): 1nF; 1kΩ / 6.8nF; 660Ω / 10nF; 500Ω					
D1 Worst case 20Kbps transmission	$V_{th\_rec\ (max)}$ = 0.744 x VSUP; $V_{th\_dom\ (max)}$ = 0.581 x VSUP; VSUP = 6.0V...18V; t_{bit} = 50µs; D1 = $t_{bus\_rec\ (min)}$ / (2 x t_{bit}) OTP selection = High Slew Mode	0.396			
D2 Worst case 20kbps transmission	$V_{th\_rec\ (min)}$ = 0.422 x VSUP; $V_{th\_dom\ (min)}$ = 0.284 x VSUP; VSUP = 6V...18V; t_{bit} = 50µs; D2 = $t_{bus\_rec\ (max)}$ / (2 x t_{bit}) OTP selection = High Slew Mode			0.581	
D3 Worst case 10.4kbps transmission	$V_{th\_rec\ (max)}$ = 0.778 x VSUP; $V_{th\_dom\ (max)}$ = 0.616 x VSUP; VSUP = 6.0V...18V; t_{bit} = 96µs; D3 = $t_{bus\_rec\ (min)}$ / (2 x t_{bit}) OTP selection = Low Slew Mode	0.417			

Table 11. AC Electrical Characteristics (Continued)

Symbol	Conditions	Min	Typ	Max	Units
D4 Worst case 10.4kbps transmission	$V_{th\_rec\ (min)}$ = 0.389 x VSUP; $V_{th\_dom\ (min)}$ = 0.251 x VSUP; VSUP = 6V...18V; t_{bit} = 96µs; D4 = $t_{bus\_rec\ (max)}$ / (2 x t_{bit}) OTP selection = Low Slew Mode			0.59	
t_{dLR}	VCC= 3.3V; Propagation delay bus dominant to RX LOW			6	µs
t_{dHR}	VCC= 3.3V; Propagation delay bus dominant to RX HIGH			6	µs
t_{RS}	Receiver Delay symmetry	-2		2	µs
t_{wake}	Wake-up delay time	30		150	µs
t_{sln}	Transition from standby mode to normal mode (clock frequency is 128kHz ±25%)		4		Clock cycles
t_{nsl}	Transition from standby mode to normal mode (clock frequency is 128kHz ±25%)		6		Clock cycles
t_{rec_deb}	Receiver De-bounce time	0.6		1	µs
C_{int}	Internal capacitance of the LIN node			250	pF

6.2.6 TX Timeout Watchdog

Table 12. TX Timeout Watchdog

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{lin_wdog}	Time out period for the dominant state		0.5	1	2	s

6.2.7 Temperature Limiter

Table 13. Temperature Limiter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sd}	Shut down temperature	Junction temperature	155	170	185	°C
T_{otset}	Over-temperature warning	Junction temperature	142	157	172	°C
T_{ret}	Return temperature	Junction temperature	125	140	155	°C

6.2.8 Other Modules

Table 14. Other Modules

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vuvr_off	VCC under-voltage threshold off (default)	Rising edge of VCC	2.55		2.95	V
Vuvr_on	VCC under-voltage threshold on (default)	Falling edge of VCC	2.3		2.7	V
Vuvr1_off	VCC under voltage threshold off (factory option)	Rising edge of VCC	3.0		3.4	V
Vuvr1_on	VCC under voltage threshold on (factory option)	Falling edge of VCC	2.75		3.15	V
Vuvr2_off	VCC under voltage threshold off (factory option)	Rising edge of VCC	3.5		3.9	V
Vuvr2_on	VCC under voltage threshold on (factory option)	Falling edge of VCC	3.25		3.65	V
Vuvr3_off	VCC under-voltage threshold off (factory option)	Rising edge of VCC	4.0		4.4	V
Vuvr3_on	VCC under voltage threshold on (factory option)	Falling edge of VCC	3.75		4.15	V
Vhyst_vcc	Hysteresis of under-voltage threshold on/ off VCC	For all OTP options	0.1	0.25	0.4	V
t_{rr}	Glitch filter on VCC under-voltage detection	See Reset Functionality (page 18)			4	µs
Vsuvr_off	VSUP under-voltage threshold off	Rising edge of VSUP		5.1		V
Vsuvr_on	VSUP under-voltage threshold on	Falling edge of VSUP		3.8		V
WD_TCL	WWD non-service time (factory option)	RESET will be generated	0-75	0-100	0-125	ms
WD_TSV	WWD Service time (factory option)	RESET will not be generated	75-150	100-200	125-250	ms
WD_TCL1	WWD non-service time (factory option)	RESET will be generated	0-60	0-80	0-100	ms
WD_TSV1	WWD Service time (factory option)	RESET will not be generated	60-120	80-160	100-200	ms
WD_TCL2	WWD non-service time (factory option)	RESET will be generated	0-45	0-60	0-75	ms
WD_TSV2	WWD Service time (factory option)	RESET will not be generated	45-90	60-120	75-150	ms
WD_TCL3	WWD non-service time (factory option)	RESET will be generated	0-150	0-200	0-250	ms
WD_TSV3	WWD Service time (factory option)	RESET will not be generated	150-300	200-400	250-500	ms
WD_TCL4	WWD non-service time (factory option)	RESET will be generated	0-120	0-160	0-200	ms
WD_TSV4	WWD Service time (factory option)	RESET will not be generated	120-240	160-320	200-400	ms
WD_TCL5	WWD non-service time (factory option)	RESET will be generated	0-90	0-120	0-150	ms
WD_TSV5	WWD Service time (factory option)	RESET will not be generated	90-180	120-240	150-300	ms
WD_T	TWD service time	T is configured through SPI	0.75*T	T	1.25*T	s
t_{Res}	Reset period	Min = -25% and Max = +50%	6	8	12	ms
T_{shd}	Temporary shutdown reset active time		0.1		1	s

6.2.9 4-Wire Serial Port Interface

Table 15. 4-Wire Serial Port Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
BR_{SPI}	Bit rate				250	Kbps
T_{SCLKH}	Clock high time		2			µs
T_{SCLKL}	Clock low time		2			µs
Write Timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
T_{CSH}	CS hold time		20			ns
Read Timing						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns
Timing parameters when entering 4-Wire SPI mode (for determination of CLK polarity)						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns
$T_{STNDY\_trigger}$	TX high time from EN falling edge	To enter into Sleep/Standby mode	5			cycles

6.3 Timing Diagrams

Figure 3. Timing Diagrams for Propagation Delays

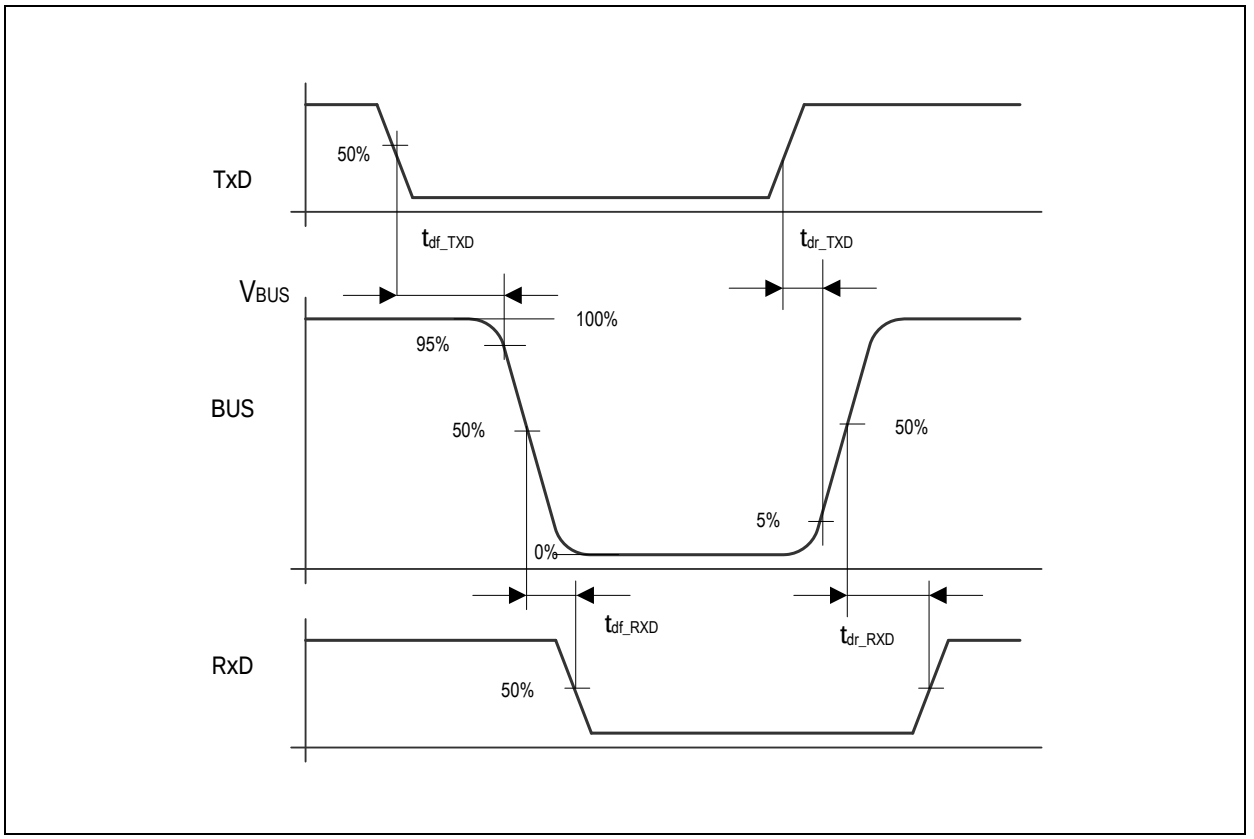
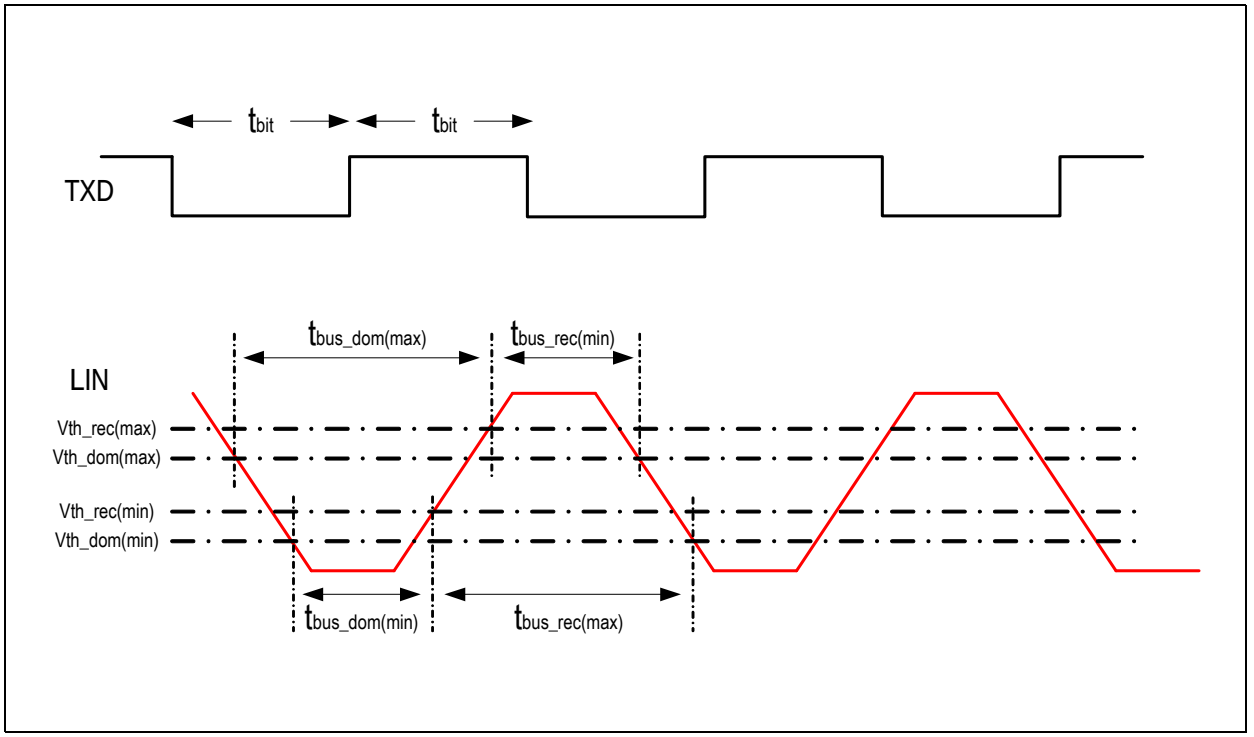


Figure 4. Timing Diagram for Duty Cycle According to LIN 2.1 and J2602



7 Detailed Description

The following modules are described in detail under this section:

- Programmable-Gain Amplifier (PGA) / Current-Sense Amplifier (CSA)
- Voltage Attenuator
- Voltage Regulators (LDO & ALDO)
- LIN Transceiver
- Temperature Monitor/Limiter
- VSUP Under-Voltage Reset
- RESET
- VCC Under-Voltage Reset
- Window Watchdog (WWD)
- Timeout Watchdog (TWD)

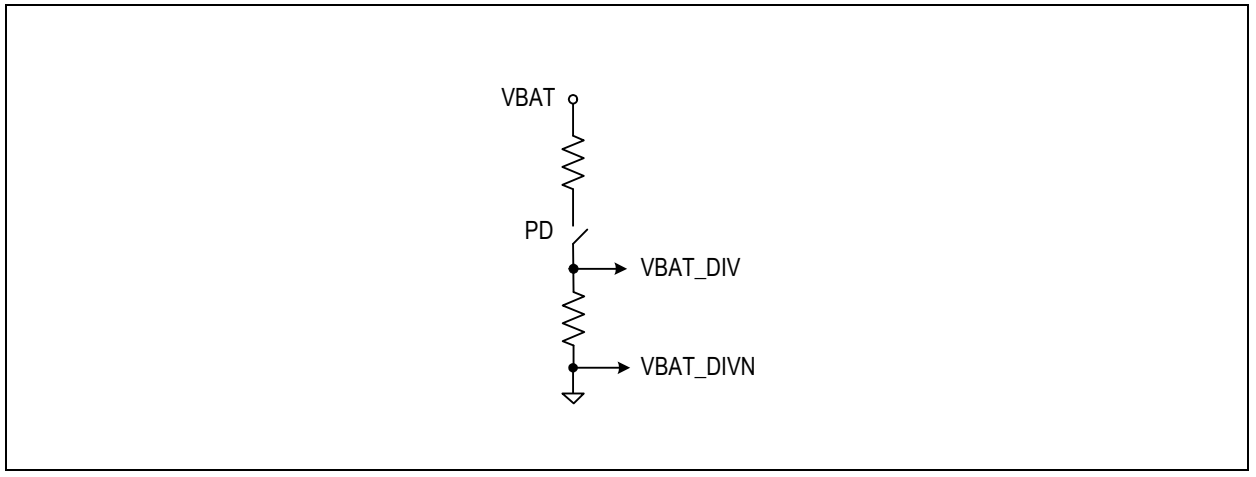
7.1 Programmable-Gain Amplifier (PGA) / Current-Sense Amplifier (CSA)

The current-sense amplifier primarily serves the purpose of shifting the common-mode level of the signal from around the battery voltage to a low voltage which is nominally half the regulated supply voltage. The input to the amplifier can be optionally chopped for offset and low-frequency noise mitigation. As the name indicates, it also provides a programmable gain for the measurement of different battery current ranges which can be programmed through SPI.

7.2 Voltage Attenuator

A resistive divider is used as a battery voltage attenuator. Like the amplifier, the attenuator can be enabled or disabled through SPI, and in the device standby mode, we additionally need logic high on MEN pin for enabling. Internal reverse polarity protection is provided for VBAT pin.

Figure 5. Attenuator Implementation



7.3 Voltage Regulators (LDO & ALDO)

The device has two low-dropout voltage regulators, named LDO and ALDO, with one-time programmable 3.3V voltage output. The output of the LDO is VCC and that of the ALDO is AVCC. The regulated voltage choice is common to both the regulators. The regulators are always ON except when the device enters the sleep mode or over-temperature shutdown.

The two regulators have inbuilt short-circuit current limitation feature.

The regulators can be temporarily shut down for hard reset of the external circuitry by configuring the device to temporary shutdown mode through SPI.

The LDO power-up happens when the POR-VSUP event occurs (RESET_VSUP_N switching from low to high), and the ALDO powers up when POR-VCC event occurs (RESET_VCC_N switching from low to high). The start-up sequence is the same even after a temporary shutdown phase. The ALDO will be switched off if there is an under-voltage on VCC, that is, when RESET_VCC_N switches back to low.

7.4 LIN Transceiver

The device has a LIN transceiver with slew-controlled bus driver for controlling the electromagnetic emissions from the LIN bus. Further, the slew rate is independent of the bus load. The transmitter relays the data from the LIN controller (TX pin) to the bus (LIN pin), and the receiver provides the data on the bus to the controller (RX pin). The transceiver conforms to the LIN 2.1 standard.

The LIN transceiver has a timeout watchdog for TX. After the timeout, the LIN bus will be released to the recessive state from the dominant state.

The bus driver has an inbuilt short-circuit current limitation facility to protect the device from damage when there is a short between the bus and the supply.

In addition to the data receiver, there is a low-power receiver active in the device standby/sleep mode which received a wake-up event from the bus to bring the device to normal mode.

7.5 Temperature Monitor / Limiter

The temperature limiter circuit powers down the device when the junction temperature exceeds 170°C (nominal). It also issues an over-temperature warning at 160°C (nominal). The device is powered up again when the junction temperature falls below 140°C (nominal). The over-temperature warning flag is also cleared at this temperature.

The temperature limiter circuit can be optionally disabled through SPI.

7.6 VSUP Under-Voltage Reset

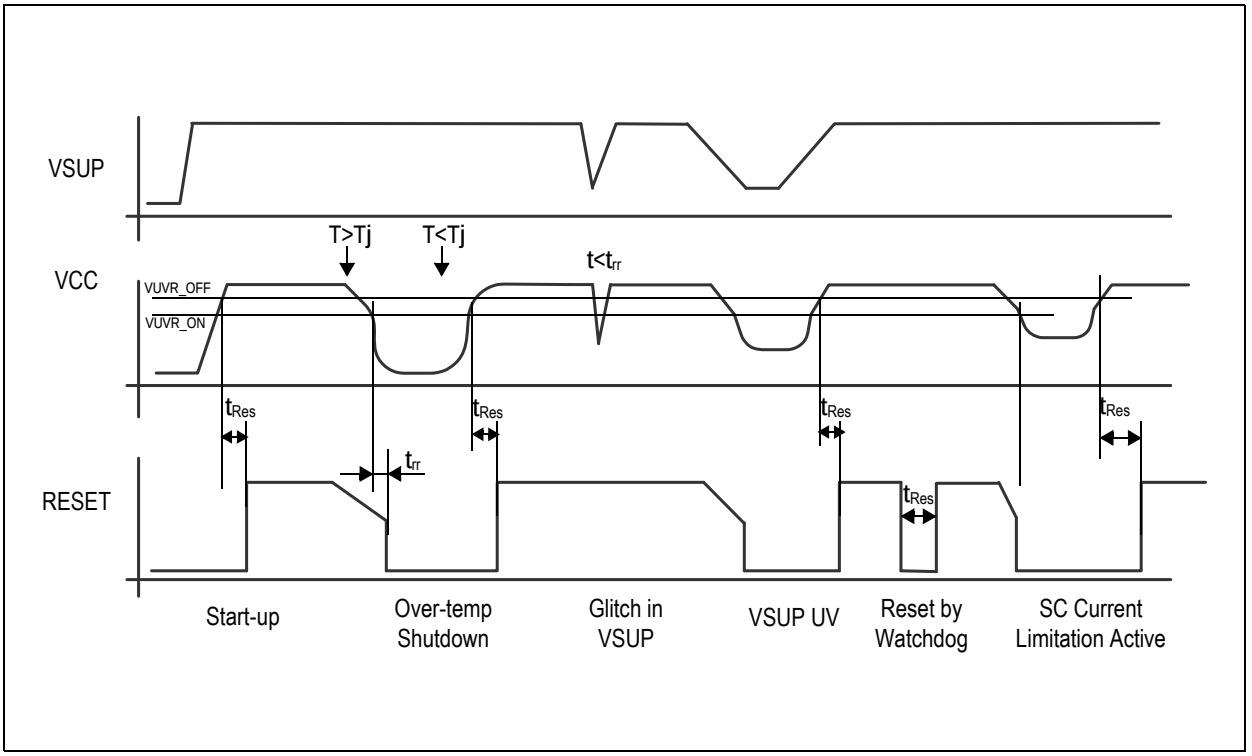
When VSUP drops below VSUVR_ON, the RESET_VSUP_N switches back to low level. This is treated as a master reset and will have the highest priority over all other signals. In this case, the regulators, LIN transceiver, and all other blocks are shut off, and the device comes to a complete stop. The device returns to the normal mode when VSUP rises over VSUVR_OFF again irrespective of the mode it was in prior to this under-voltage condition.

7.7 RESET

RESET module generates an active-low reset signal for the external circuitry supplied by VCC. The behavior of the reset output is depicted in Figure 6 in different cases. As shown, RESET signal is affected by an under-voltage condition on VCC and Watchdogs which are described in detail in the subsequent sections.

The reset period can be one-time programmed to 4, 16, and 32 ms with a default value of 8 ms.

Figure 6. Reset Functionality



7.8 VCC Under-Voltage Reset

When VCC drops below VUVR_ON, the RESET_VCC_N switches back to low level. This event generates a reset output. The reset output is released again only a reset period (t_{Res}) later after VCC rises above VUVR_OFF. If the time difference between the VCC falling below VUVR_ON and rising above VUVR_OFF is less than t_{rr}, there will be no reset output. The reset output is affected in the conditions like over-temperature shutdown and temporary shutdown only through VCC under-voltage.

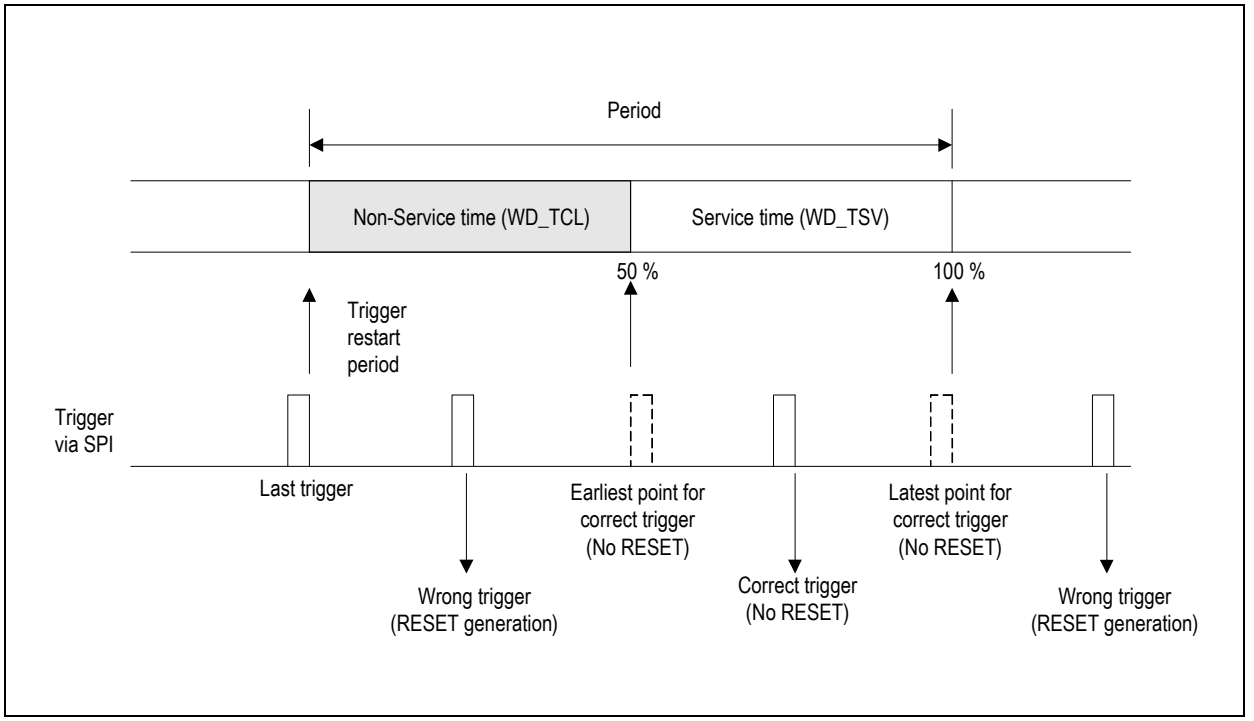
VCC under-voltage reset thresholds (VUVR_ON and VUVR_OFF) can be chosen by OTP.

7.9 Window Watchdog (WWD)

The Window Watchdog ensures that the Microcontroller is properly functioning in the normal mode of the device. The Watchdog is started after a reset and the Microcontroller needs to send a trigger in the window of WD_TSV (service time). If the trigger occurs early, in the period WD_TCL, or after WD_TSV, a reset output is generated.

The Microcontroller can access the trigger bit for the watchdog through SPI. The WWD can be enabled and the window times can be programmed through OTP bits.

Figure 7. Window Watchdog Functionality



7.10 Timeout Watchdog (TWD)

The Timeout Watchdog ensures that the Microcontroller is in proper functional state in the device standby mode. The Watchdog timer will be started upon a rising edge on INT and will generate a reset output if the Microcontroller doesn't send a trigger before the timeout.

The Microcontroller can access the trigger bit for the watchdog through SPI. The TWD can be enabled by OTP and the timeout interval can be programmed through SPI.

8 Application Information

The AS8525 chip consists of a programmable gain amplifier, a resistive divider, two low drop-out regulators, and a LIN bus transceiver. Additionally integrated are a RESET unit with a power-on-reset delay and programmable window watchdog and timeout watchdog timers. It also includes a watchdog time-out on LIN TX node to indicate if the Microcontroller is stuck in a loop and the LIN bus remains in dominant time for more than the necessary time.

8.1 Operating Modes and States

The device provides four main operating modes ‘normal’, ‘sleep/stand-by’ (programmed by OTP), “temporary shutdown” and ‘thermal shutdown’. The LIN transceiver can be programmed to operate with lower slew in the normal mode. A detailed state transition table is shown in the following section (see Table 16).

8.1.1 Normal Mode

This is the mode after the power-up. In this mode, voltage regulators, LIN transceiver, window Watchdog are all active. The PGA and resistive divider can be enabled through SPI. LIN transceiver is capable of sending the TX data from micro-controller to the LIN bus at a maximum rate of 20Kbps.

8.1.2 Standby Mode

Standby mode is a functional low-power mode and is entered by pulling EN to ground. The LIN transceiver, PGA, resistive divider, window watchdog, and TX timeout watchdog circuits are disabled. But, it is possible to selectively enable the voltage and current measurement paths in this mode using an externally generated measurement enable (MEN) signal on the MEN pin. The timeout Watchdog can be enabled in this mode to make sure that the Microcontroller is active.

8.1.3 Sleep Mode

Sleep mode is the current saving mode. The voltage regulators are disabled in this mode. Also, the PGA, resistive divider, LIN transceiver, and the reset and Watchdog units are switched off. The LIN wake-up circuit and oscillator are active. Wake-up is possible only through remote wake-up through LIN pin pulling it to dominant state for 100us.

8.1.4 Temporary Shutdown Mode

In this mode, the regulators are powered down and the VCC, AVCC are pulled down. This provides an alternative way to reset those components powered by AS8525. The feature has to be enabled by an OTP bit and can be invoked through SPI. The LIN transceiver along with the LIN wake-up circuit is powered down. No remote wake-up functionality is possible. LIN bus enters into recessive state. The system goes out of this mode to normal mode after the timeout of an internal timer.

8.1.5 Thermal Shutdown Mode

If the junction temperature T_J is higher than T_{sd}, the device will be switched into the thermal shutdown mode. The regulators and the transceiver are completely disabled. Only the over-temperature monitor is active. As soon as the temperature returns back to T_{ret}, the system enters normal mode.

8.2 State Transition Diagram

The complete functional state machine of AS8525 is shown in this section. Soft states like “TXWD Wait” and “Standby Wait”, and other wait states have also been included here for completeness.

Figure 8. Finite State Machine Model of AS8525

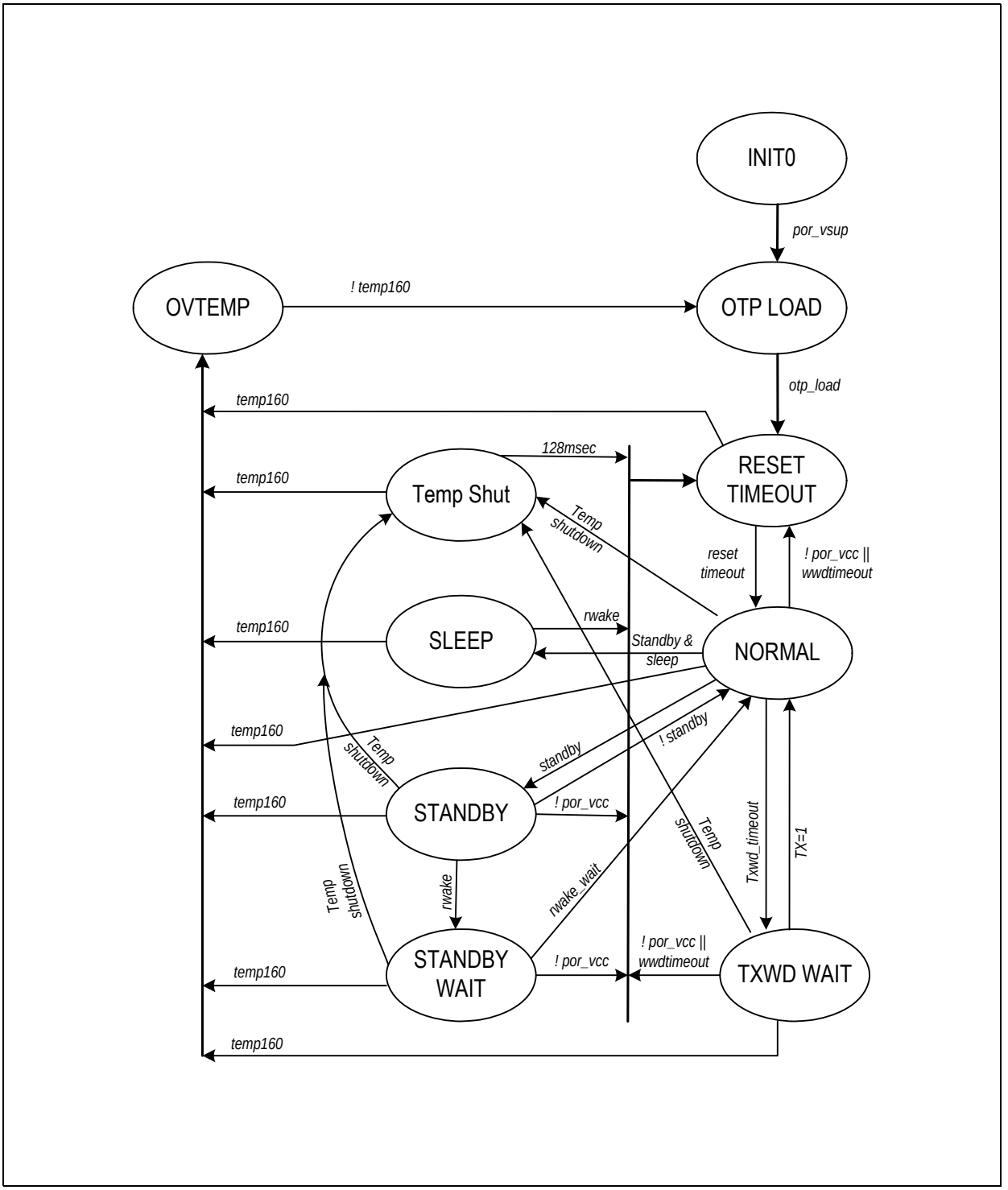


Table 16. Transition Table

Transition		Interface				Reg. 0x05 D0	Flags				
From mode	To mode	LIN	RX	TX	EN		rwake	Uvbat	OT	Uvcc	Comments
Normal Mode	Stand-By	X-RS	X-H[2]	H[3]	H-L[3]	L	X	X	inactive	inactive	TX is high for $T_{STNDY\_trigger}$
	Sleep[1]	X-RS	X-H[2]	H[3]	H-L[3]	L	X	X	inactive	set	TX is high for $T_{STNDY\_trigger}$[1]
	Temporary Shutdown	X-RS	X-H[2]	X	H	H[3]	X	X	inactive	set	The Control Bit is set through the 4-Wire SPI interface
	Over-Temperature	X-RS	X-H[2]	X	X	L	X	X	set	set	Temperature monitor output asserted (covered by scan)
	2-Wire Interface	X	X	H-L[3]	H-L[3]	L	X	X	inactive	inactive	TX goes High to low within $T_{tx\_SP\_trigger}$ Window.
2-Wire Interface (This is a testing condition only)	Normal Mode	X	X	X	H	L	X	X	inactive	inactive	Completion of 2-Wire Read/Write command
	Temporary Shutdown	X-RS	X-H[2]	X	X	H[3]	X	X	inactive	set	Completion of 2-Wire Write command to 0x05
	Over-Temperature	X-RS	X-H[2]	X	X	L	X	X	set	set	Temperature monitor output asserted (covered by scan)
Stand-By Mode	Normal (LW)	X	H-X[2]	X	L-H[3]	L	X	X	inactive	inactive	
	Normal (RW)	X	H-X[2]	H	X	L	set	X	inactive	inactive	Remote Wake up Event occurred on LIN
	Temporary Shutdown	RS	H[2]	H	L	H[3]	X	X	inactive	set	The Control Bit is set through the 4-Wire SPI interface
	Over-Temperature	RS	H[2]	H	L	L	X	X	set	set	Temperature monitor output asserted (covered by scan)
Temporary Shutdown Mode	Normal	RS-X	H-X[2]	X	X	L	X	X	inactive	clear	Internal 128ms timer expired
Over-Temperature Mode	Normal	RS-X	H-X[2]	X	X	L	X	X	clear	clear	Temperature monitor output de-asserted (covered by scan)
Sleep Mode[3]	Normal	RS-X	H-X[2]	X	X	L	set	X	inactive	clear	Remote Wake up Event occurred on LIN
	Over-Temperature	RS	H[2]	X	X	L	X	X	set	hold	Temperature monitor output asserted (covered by scan)
All States	Power Off	X	X	X	X	X	X	L-H[3]	X	X	

1. Chosen by OTP option
2. Effect of Transition
3. Cause for Transition

Note: L = low state, H = high state, OT = Over-temperature Reset, Uvcc = Under-voltage VCC, Uvbat = Under-voltage VBAT, rwake =remote wake, X = don't care.

8.3 Initialization

When the power supply is switched on, when VSUP > VSUVR_OFF, RESET_VSUP_N becomes high. This starts the regulator LDO with 3.3V and Vuvr_off option of 2.75V. When VCC > Vuvr_off (2.75V), active-low PORN_2_OTP is generated and the regulator ALDO is turned on with 3.3V. The rising edge of PORN_2_OTP loads contents of fuse onto the OTP latch after load access time T_{Load}. LOAD_OTP_IN_PREREG signal loads contents of OTP latch onto a register. This register provides the actual settings of LDO (and ALDO), Vuvr_off and Reset Timeout period T_{Res}. This is done as the OTP block is powered by the VCC. If VCC > Vuvr_off (phase 2), Reset timeout is restarted. RESET signal is de-asserted after Reset Timeout period T_{Res} (phase 2) and then device enters into normal mode. The circuit also needs to initialize correctly for very slow ramp rates on VSUP (of the order of 0.5V/min).

Figure 9. Initialization Sequence for AS8525

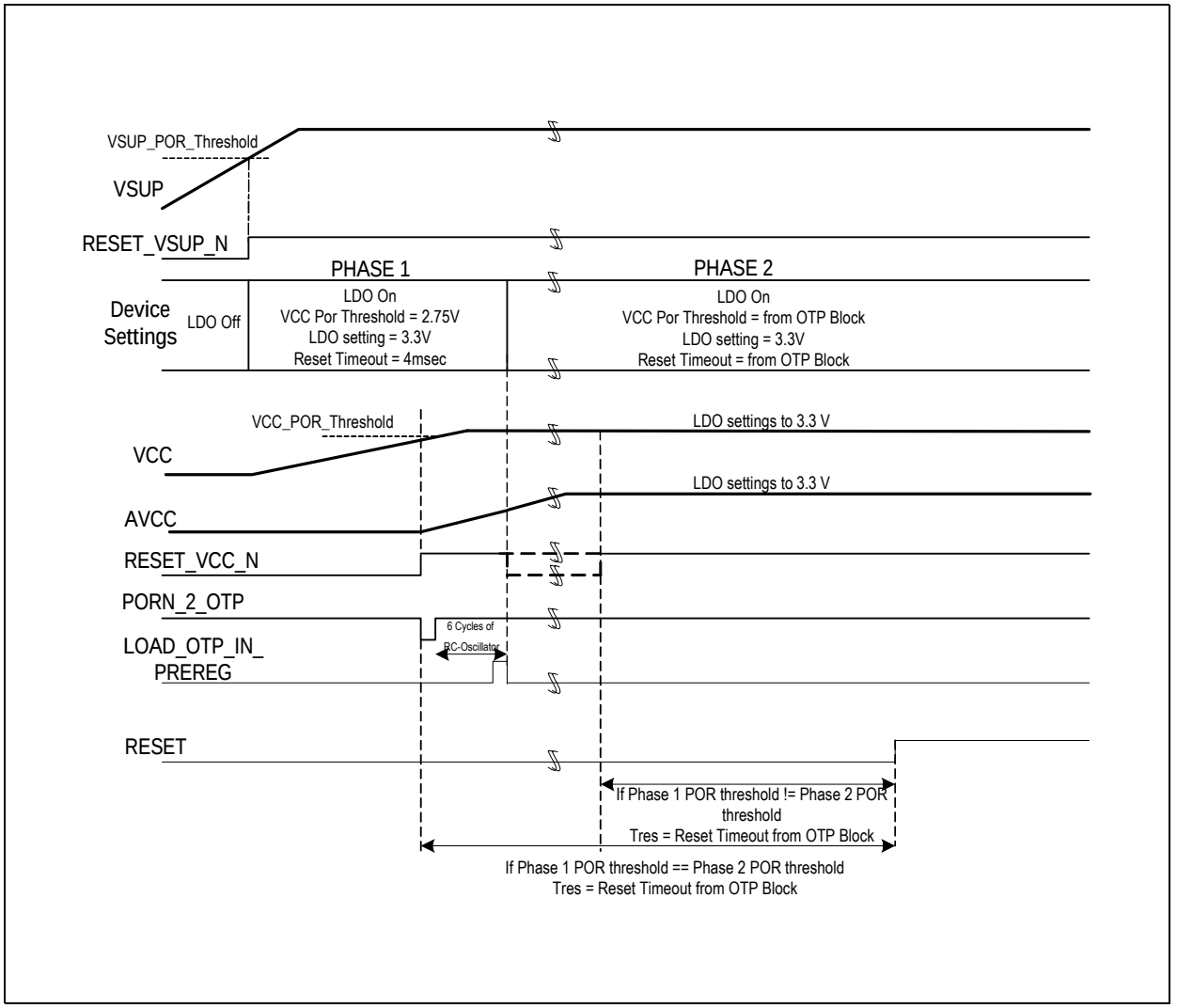


Table 17. VSUP>Vsuvr_on and VCC<Vuvr_on

Block	Output Signal
TRANSCEIVER=Enabled (disabled only during initial VSUP ramp-up)	LIN=high-z, RX=follows VCC…
LDO=Enabled (disabled only during initial ramp-up)	VCC=low…
RELAY DRIVER=Enabled	LDRIVE1=high… LDRIVE2=high…
RESET BLOCK=Enabled	RESET=high-z…
RESISTIVE DIVIDER=Enabled	VBAT=high…, VBAT_DIV=enabled

Table 18. VSUP<Vsuvr_on

Block	Output Signal
TRANSCEIVER=Disabled	LIN=high-z, RX=high-z…
LDO=Disabled	VCC=low
RELAY DRIVER=Disabled	LDRIVE1=high LDRIVE2=high
RESET BLOCK=Disabled	RESET=high-z
RESISTIVE DIVIDER=Disabled	VBAT=high, VBAT_DIV=low

8.4 Wake-Up

When the device enters sleep/standby mode, it can be brought back to the normal mode with the BUS interface. A dominant state on the BUS for t_{wake} will result in the device wakeup.

8.5 LIN BUS Transceiver

The AS8525 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller. The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a de-bouncing unit.

8.5.1 Transmit Mode

During transmission the data at the pin TX will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:

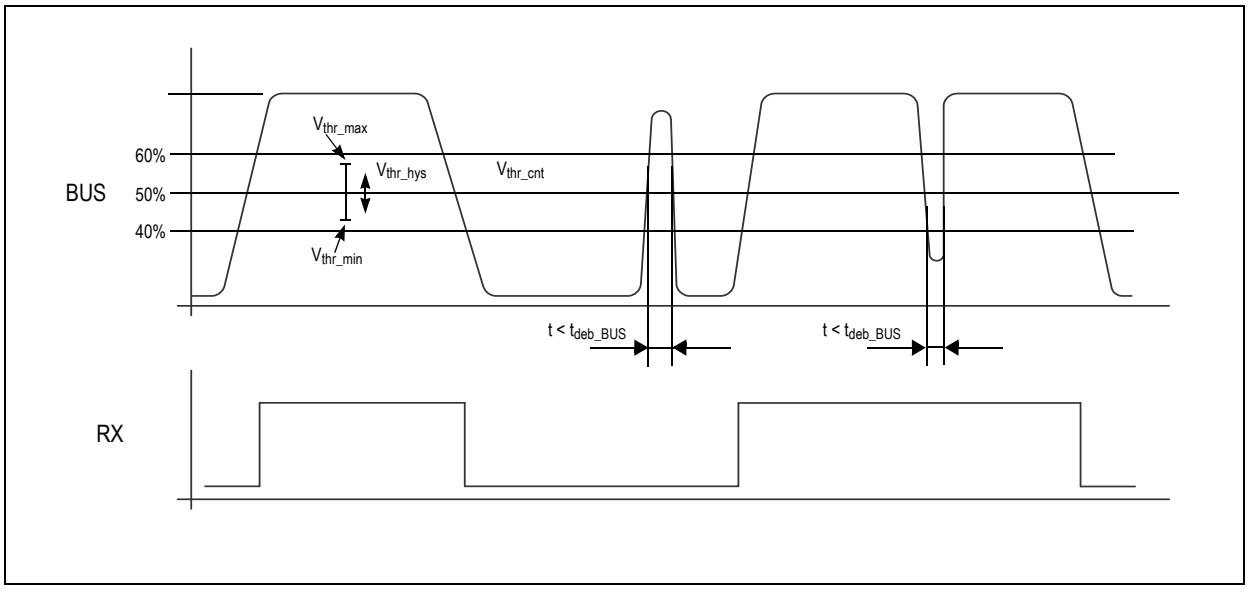
- Sleep mode
- Thermal Shutdown active
- Master Reset (VSUP < Vsuvr_on)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS (VBUS>VSUP). No additional termination resistor is necessary to use the AS8525 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

8.5.2 Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin RX. Short spikes on the bus signal are suppressed by the implemented debouncing circuit. Including all tolerances the LIN specific receive threshold values of 0.4*VSUP and 0.6*VSUP will be securely observed.

Figure 10. Receive Mode Impulse Diagram

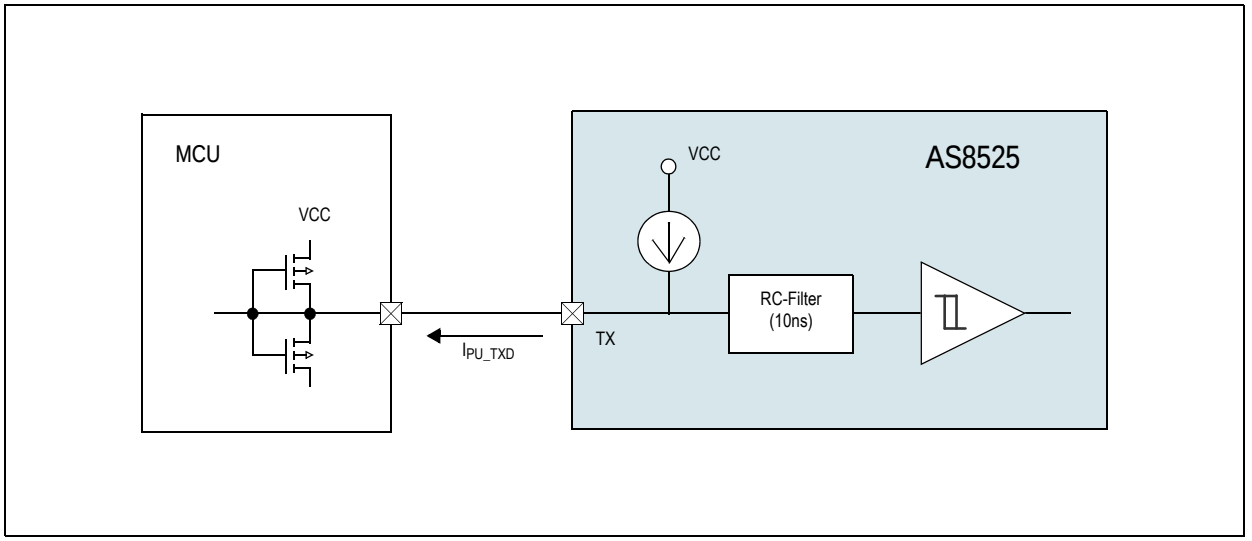


8.6 RX and TX Interface

8.6.1 Input TX

The Tx input controls directly the BUS level. LIN Transmitter acts like a slew-controlled level shifter. A dominant state (low) on TX leads to the LIN bus being pulled low (dominant state) too. The TX pin has an internal active pull up connected to VCC. This guarantees that an open TX pin generates a recessive BUS level.

Figure 11. TX Interface



8.6.2 Output RX

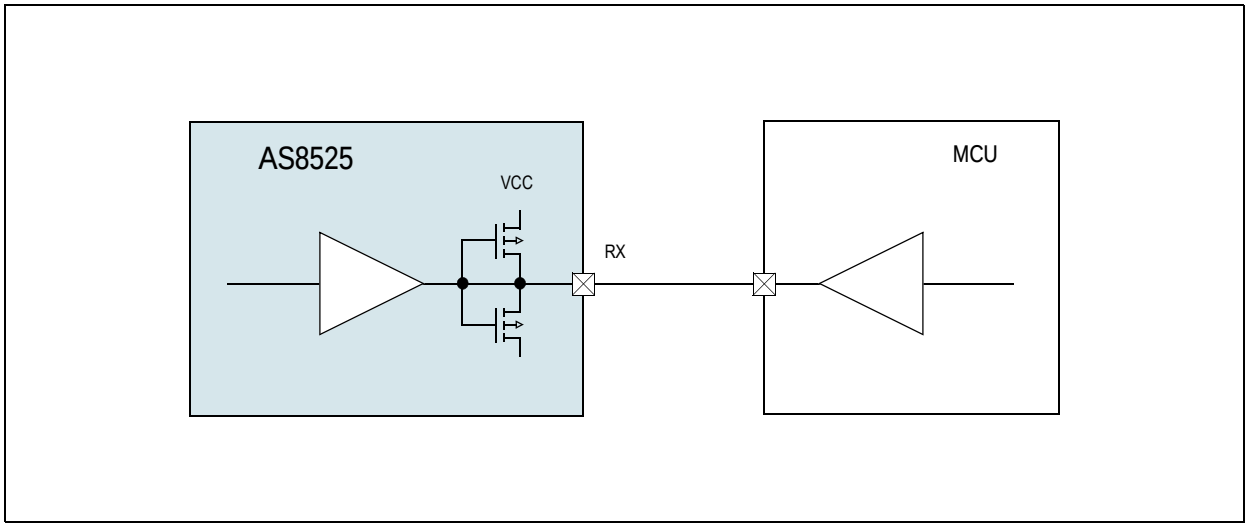
The received BUS signal will be output to the RX pin:

BUS < Vthr_cnt – 0.5 * Vthr_hys → RX = low

BUS > Vthr_cnt + 0.5 * Vthr_hys → RX = high

This output is a push-pull driver between VCC and GND with an output current of 1mA.

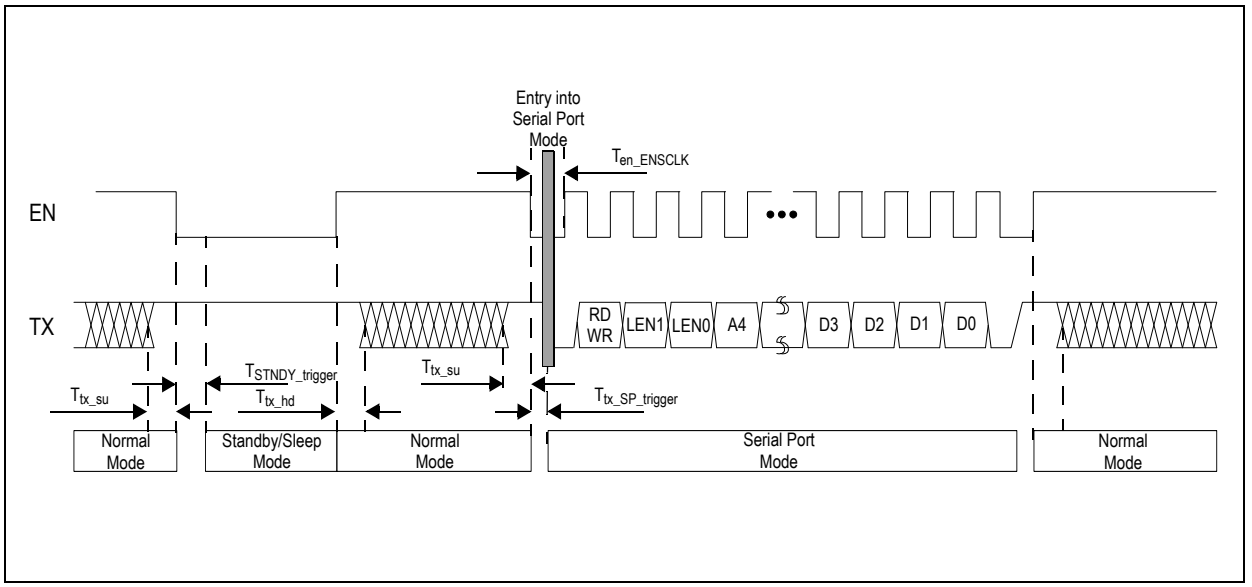
Figure 12. RX Interface



8.7 MODE Input EN

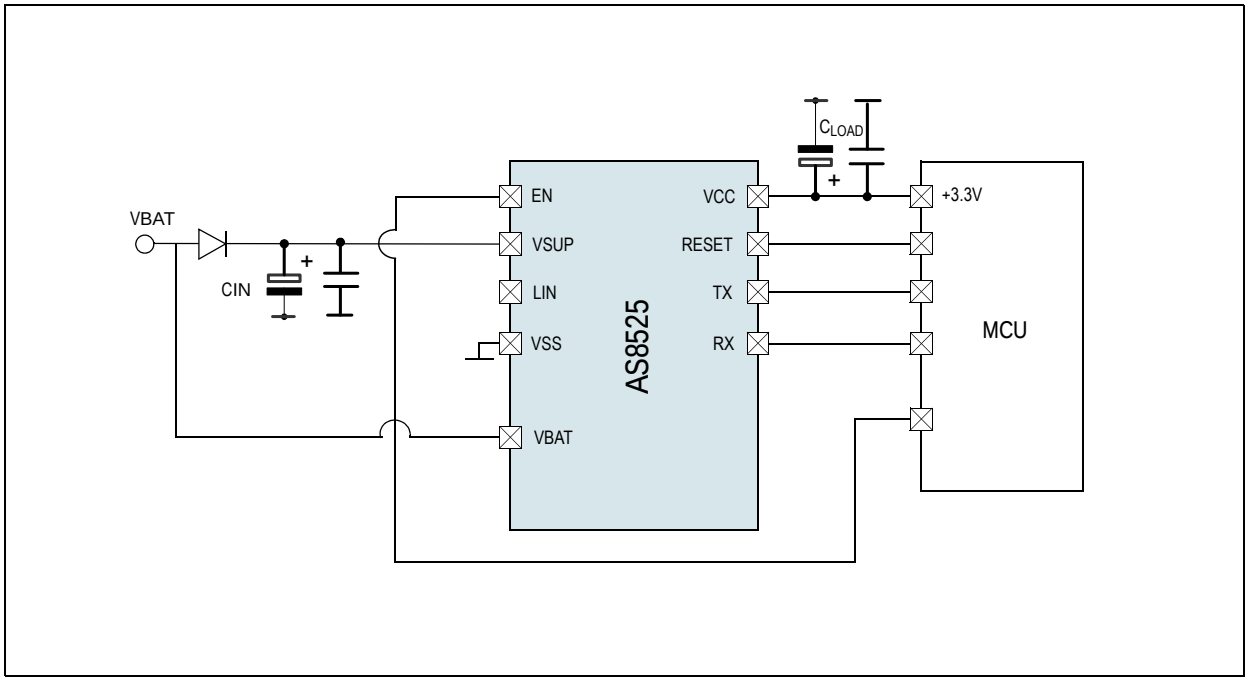
The AS8525 is switched from normal mode to the standby/sleep mode with a falling edge on EN and keeping TX high for $T_{STNDY\_trigger}$ time. Device is switched from standby mode to normal mode with a rising edge at the EN pin. The mode change for AS8525 with a falling edge on EN can be done independently from the state of the transceiver bus. The device enters into Serial port mode by forcing EN low and driving TX high to low within $T_{tx\_SP\_trigger}$ time after EN forced to low. This ensures the direct control of device to enter into standby/sleep mode by microcontroller using EN pin.

Figure 13. EN Pin Functionality



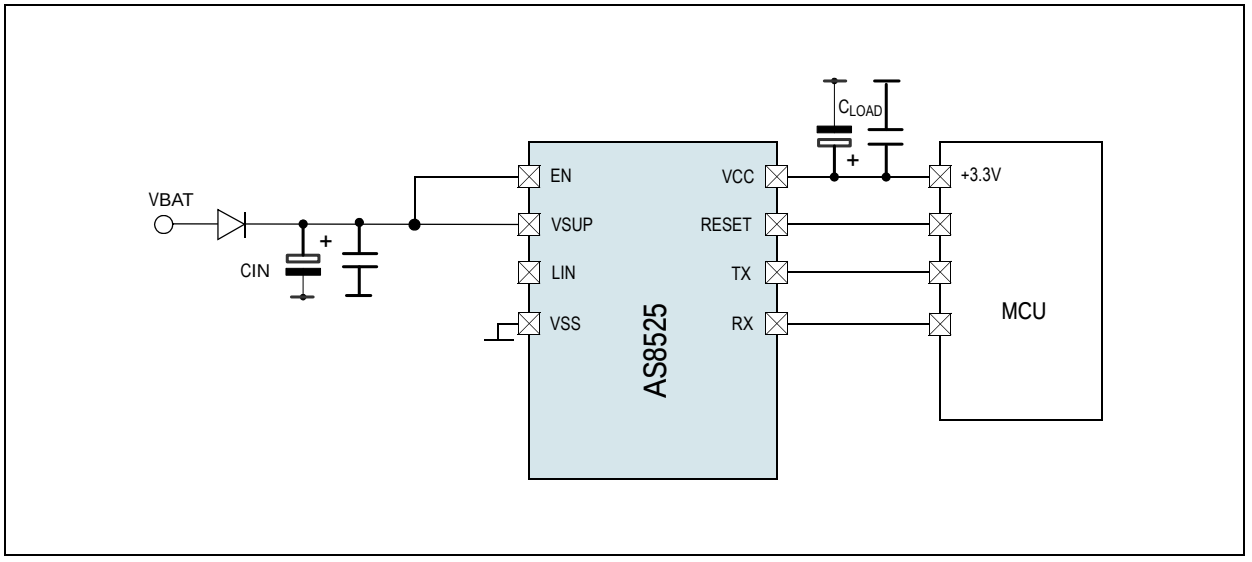
The EN input has an internal active pull down to secure that if this pin is not connected, a low level will be generated.

Figure 14. Enable Interface



If the application doesn't need the low-power modes of the device, a direct connection of EN to VCC is possible. In this case the AS8525 operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via VSUP signal as shown below.

Figure 15. EN Connection for Permanent Normal Mode



8.8 4-Wire SPI Interface

SPI interface is essentially used for programming the gain of the PGA, to enable the PGA and resistive attenuator in the standby mode, to temporarily shutdown the LDOs, etc. The SPI interface can also be used as interface between the AS8525 and an external micro-controller to configure the device and access the status information. The interface is a slave and then only the microcontroller can start the communication. The SPI protocol is very simple and the length of each frame is an integer multiple of byte except when a transmission is started. Basically each frame has 1 command bits, 5 address/configuration bits, 1 or more data bytes. SPI clock polarity settings depend on the value of the SCLK on the CS falling edge. This setting is done on each start of the SPI transaction. During the transaction SPI clock polarity will be fixed to the settings done. On the CS falling edge the values on SCLK signal decide setting of the active SPI clock edge for data transfer (see Table below).

Table 19. CS and SCLK

CS	SCLK	Description
FALL	LOW	Serial data transferred on rising edge of SPI clock. Sampled at falling edge of SPI clock.
FALL	HIGH	Serial data transferred on falling edge of SPI clock. Sampled at rising edge of SPI clock.
ANY	ANY	Serial data transfer edge is unchanged.

8.8.1 SPI Frame

A frame is formed by a first byte for command and address/configuration and a following bit stream that can be formed by an integer number of bytes. Command is coded on the 1 first bit, while address is given on LSB 5 bits (see table below).

Table 20. Command Bits

Command Bits			Register Address or Transmission Configuration				
C0	Reserved	Reserved	A4	A3	A2	A1	A0

C0	Command	<A4:A0>	Description
0	WRITE	ADDRESS	Writes data byte on the given starting address.
1	READ	ADDRESS	Reads data byte from the given starting address.

If the command is read or write, one or more bytes follow. When the micro-controller sends more bytes (keeping CS LOW and SCLK toggling), the SPI interface increments the address of the previous data byte and writes/reads data to/from consecutive addresses.

8.8.2 Write Command

For Write command C0 = 0.

After the command code C0 and two reserved bits, the address of register to be written has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred, always from the MSB to the LSB. For each data byte following the first one, used address is the incremented value of the previously written address. Each bit of the frame has to be driven by the SPI master on the SPI clock transfer edge and the SPI slave on the next SPI clock edge samples it. These edges are selected as per clock polarity settings. In the following figures two examples of write command (without and with address self-increment.

Figure 16. Protocol for Serial Data Write with Length = 1

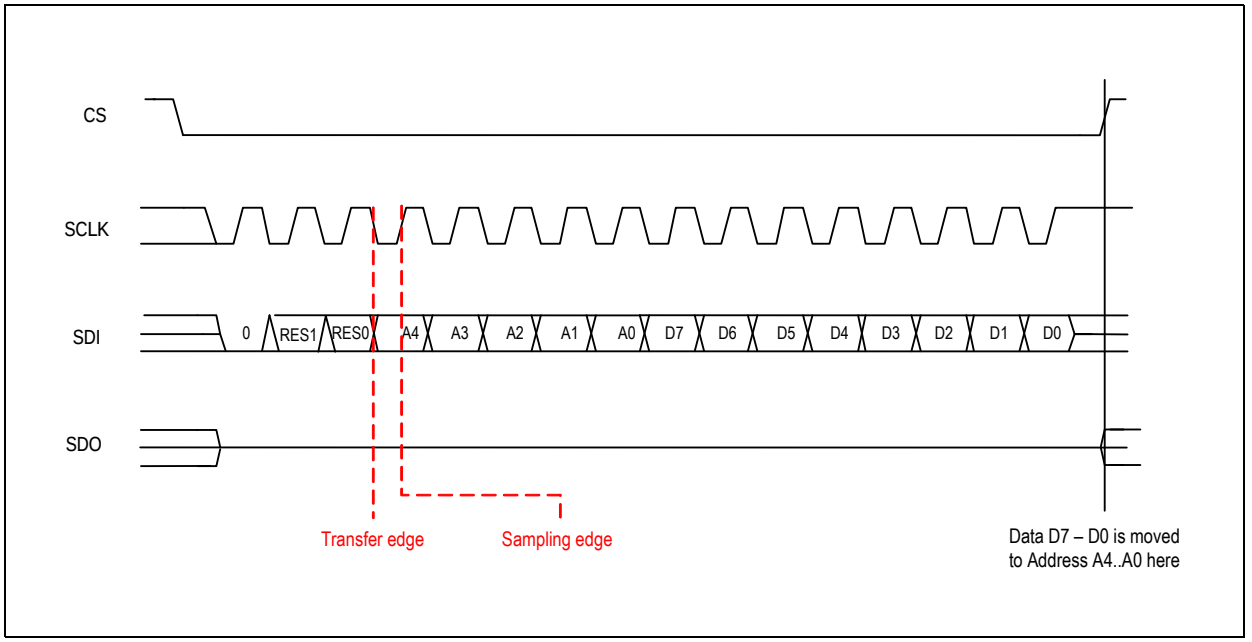
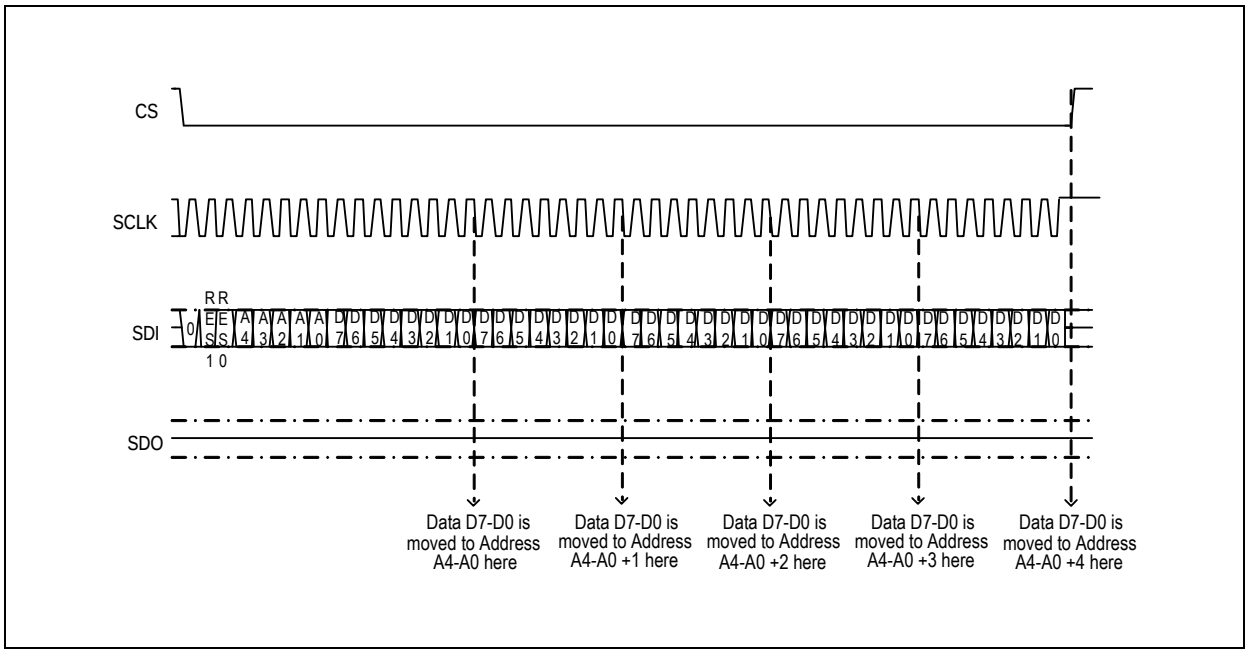


Figure 17. Protocol for Serial Data Write with Length = 4



8.8.3 Read Command

For Read command C0=1.

After the command code C0 and two reserved bits, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB. To transfer more bytes from consecutive addresses, SPI master has to keep active the SPI CS signal and the SPI clock as long as it desires to read data from the slave. Each bit of the command and address sections of the frame have to be driven by the SPI master on the SPI clock transfer edge and the SPI slave on the next SPI clock edge samples it. Each bit of the data section of the frame has to be driven by the SPI slave on the SPI clock transfer edge and the SPI master on the next SPI clock edge samples it. These edges are selected as per clock polarity settings. In the following figures, two examples of read command (without and with address self-increment) have been shown.

Figure 18. Protocol for Serial Data Read with Length = 1

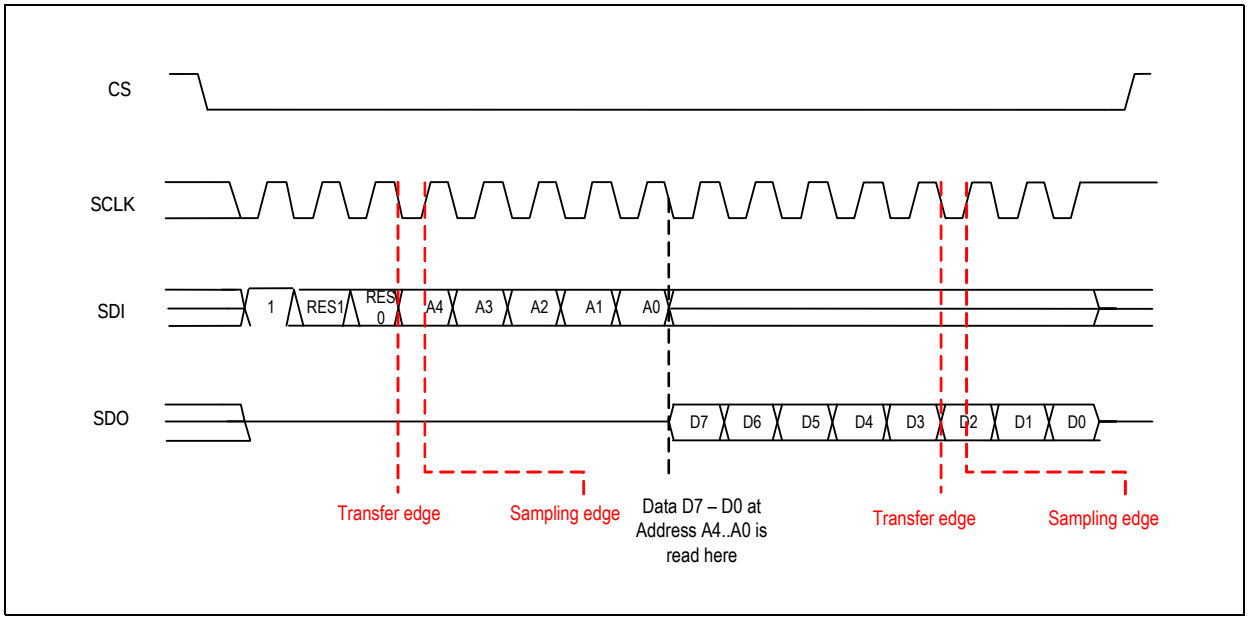
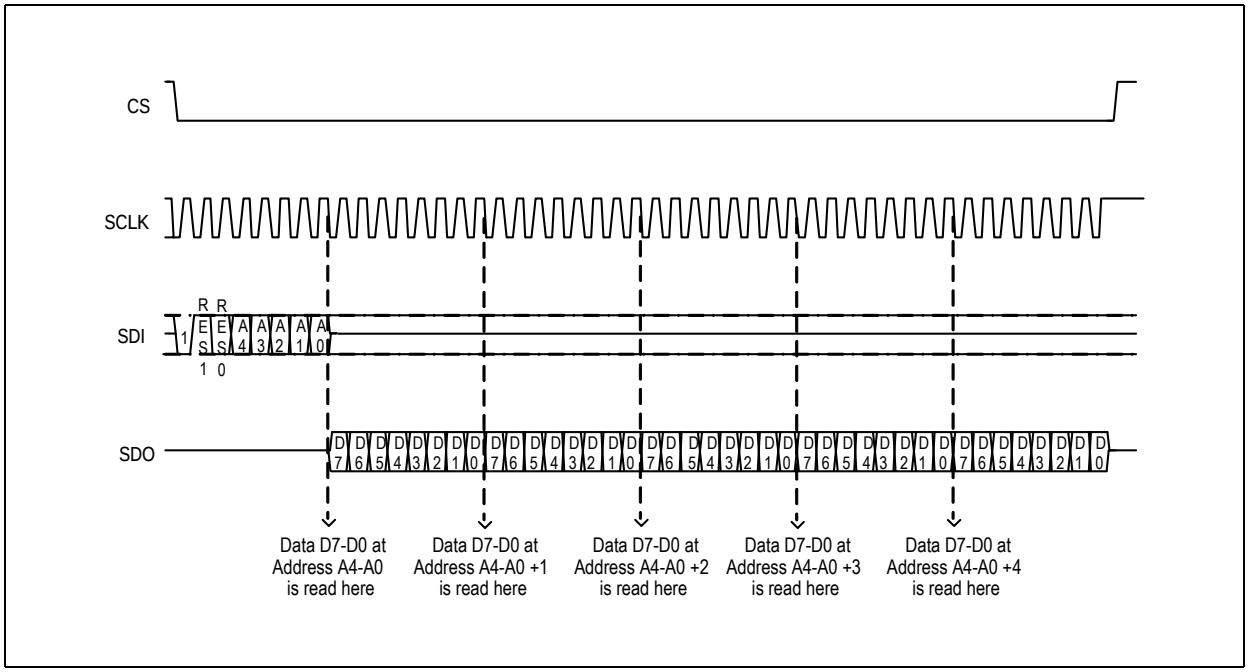


Figure 19. Protocol for Serial Data Read with Length = 4



8.8.4 Timing

In the following figures timing waveforms and parameters are exposed.

Figure 20. Timing for Writing

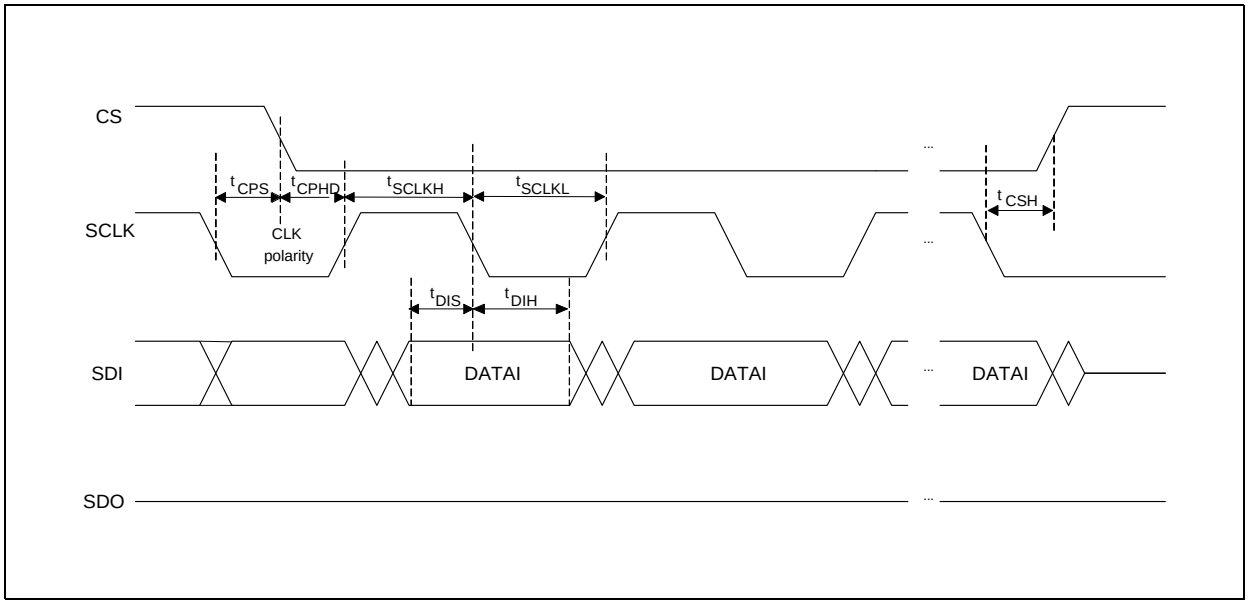
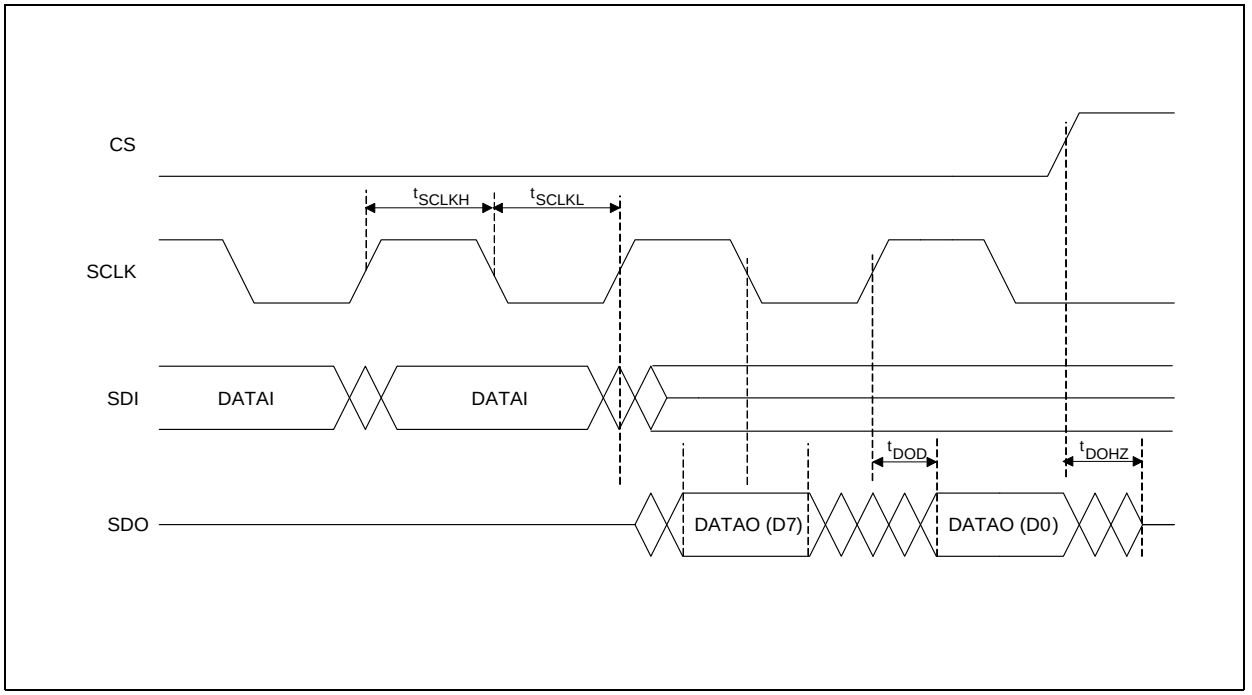


Figure 21. Timing for Reading



8.9 Configuration and Diagnostic Registers

The serial interface can be used for communication between AS8525 and an external microcontroller. The device is only a slave and the microcontroller has to initiate the communication. The device can be configured by writing into the control registers and the diagnostic information can be read out from the diagnostic registers.

8.9.1 Register Definitions

A total of 32 registers, each of 8-bits which include configuration, diagnostic, and backup are available. The registers can be accessed using the 2-wire or the 4-wire serial interface. Table 21 provides a description of all registers.

Table 21. Registers

Addr	Register Name	Default Value	RD/WR	Description
Configuration and Control Registers				
0x00	Reserved			
0x01	Reserved			
0 x 02	Reserved			
0 x 03	Device Configuration Register	On POR_VCC 0000_1100	RD/WR	D0 Reserved D1 Reserved D2 Enable/Disable Over-Temperature Monitor. (0-Disabled, 1-Enabled) D3 Enable/Disable LIN Transceiver. (0-Disabled, 1-Enabled) D4- D7 Reserved
0 x 04	Device Control Register	On POR_VSUP 0000_0001	RD/WR	D0 High Slew / Low Slew control. 1 High Slew mode 0 Low Slew Mode D1- D7 Reserved
0 x 05	Temporary Shutdown Register	On POR_VCC 0000_0000	RD/WR	D0 Temporary shutdown control bit 1 Enter temporary shutdown D1- D7 Reserved
0 x 06	Window Watch Dog Trigger Register	On POR_VCC 0000_0000	WR	D0 Window Watchdog Trigger D1 Timeout Watchdog trigger bit Upon a trigger, the bit will be cleared within 2 internal clock cycles. D2- D7 Reserved
0 x 07	Reserved			
0x0A	Signal Path Control Register	On POR_VCC 0000_0000	RD/WR	D0 Reserved D1 Enable/Disable current channel chopper (0 Disabled, 1 Enabled) D2 Reserved D3 Reserved D4 Enable/Disable voltage attenuator (0 Disabled, 1 Enabled) D5 Enable/Disable PGA (0 Disabled, 1 Enabled) D6-D7 PGA gain selection 10 00 Gain-5, 01 Gain-25, 10 Gain-50, 11 Gain-100
0x0B	Reserved			
0x0C	Reserved			
0x0D	Reserved			
0x0E	Watchdog Timer Control Register	On POR_VCC 0000_0000	RD/WR	D0 Timer resolution 0 1 second, 1 32 seconds D1-D7 Timeout period If D0=1, then timeout period = D[7:1]*64*0.512 seconds, else timeout period = D[7:1]*0.512 seconds
0x0F	Reserved			

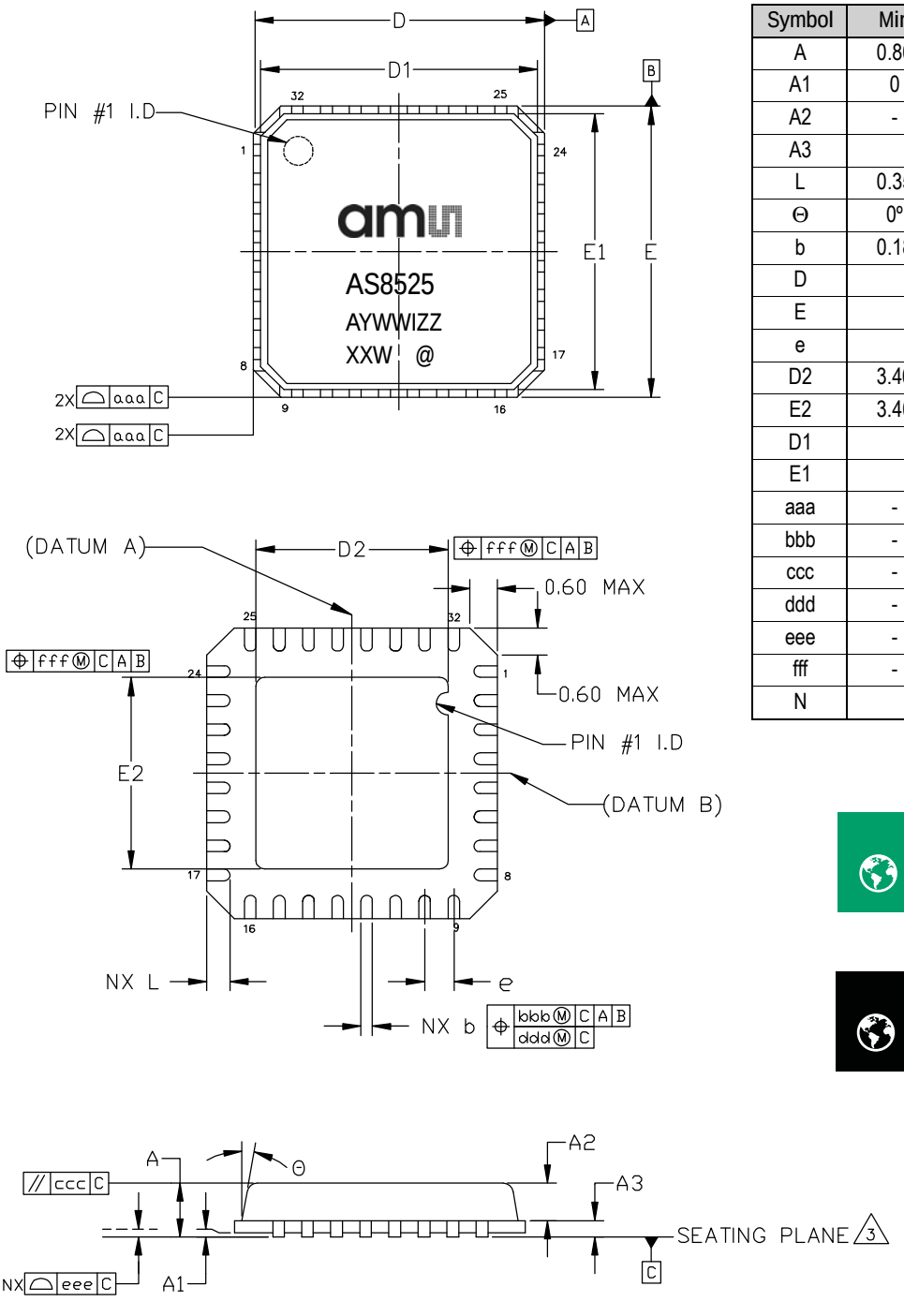
Table 21. Registers

Addr	Register Name	Default Value	RD/WR	Description
Backup Registers				
0x10 ..... 0x17	Backup-0 ..... Backup-7	On POR_VSUP 0000_0000	RD/WR	8 backup registers These registers can be used by MCU to backup any system configuration before sending the device to sleep mode. If Test Control Register D[5] =1, Backup-0 to Backup-3 are used for testing connectivity between OTP and digital modules. Backup-0 = OTP[25:32] Backup-1 = OTP[33:40] Backup-2 = OTP[41:47] Backup-3 = OTP[48:49]
Diagnostic Registers				
0 x 08	Diagnostic Register 1	On POR_VSUP 0000_0011	RD	D7-D0 = DR[7:0] 8-LSB bits of the 24-bit Diagnostic Register. D0 POR-VSUP (set when VSUP < Vsuvr_on, cleared after µC read) D1 UVVCC Under-voltage VCC (set when VCC < Vuvr_on, cleared after µC read) D2 OTEMP160 Over-temperature Reset. (set when temp > T_{sd}, cleared after µC read) D3 OTEMP140 Over-temperature warning (set when temp > T_{otset}, cleared after µC read) D4 OVVBAT Overvoltage VBAT. (set when VSUP > Vovthh, cleared after µC read) D5 Reserved D6 RWAKE Remote Wakeup. (set on Remote Wakeup event on LIN Bus, cleared after µC read) D7 WWDT Window watchdog timeout. (set on failure of Window watchdog timeout, cleared after µC read)
0 x 09	Diagnostic Register 2	On POR_VSUP 0000_0000	RD	D7-.D0 = DR[15:8] Next 8 LSB bits of the 24 bit Diagnostic Register. D0 TXTIMEOUT Tx timeout of 1sec. (set on TX low > 1sec, cleared after µC read) D1 (TEMPSHUT) This bit is set on entering into temporary shutdown state and cleared after µC read. D2 Set on failure of timeout Watchdog trigger, cleared after µC read D7- D3 Reserved

9 Package Drawings and Markings

The devices are available in a 32-pin QFN (5x5) package.

Figure 22. 32-pin QFN (5x5) Package



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.35	0.40	0.45
Θ	0°	-	14°
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
D1		4.75 BSC	
E1		4.75 BSC	
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

Marking Info:

- 1st line is AS8525 - Product Name
- 2nd Line is YYWWIZZ - Date Code
- 3rd line: XXW is place holder for 2 numbers and one letter as factory option designator. Default option this is void. '@' is a place holder for assembly lat designator.

Marking for default option:

YYWWIZZ

AS8525

@

For factory options please contact ams sales force for quotation, marking and order code.

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Revision History

Revision	Date	Owner	Description
0.1	Oct 20, 2008	mbr	Initial revision
2.1	Nov 02, 2009	mbr	Updated the entire datasheet according to spec 2.1
2.2	Oct 11, 2012	mbr	Removed LDO 5V option, added Section 6.1 Characteristics of Digital Inputs and Outputs
2.3	Nov 23, 2012	mbr	Updated Section 6.2.1 Programmable Gain Amplifier (PGA)
	Dec 31, 2012	sju	Updated ordering table.
2.4	Mar 14, 2013	mbr	Removed 5V LDO option, Removed SCLK & SDI pins and added Marking Information to Section 9.
	Apr 17, 2013		Updated Table 2 & Section 6.2.3 Voltage Attenuator
	Apr 19, 2013		Updated Marking Information to Section 9
	May 17, 2013		Updated T_{AMB} to 115ºC, Footnote added to P_{tot} in Table 2
	Dec 22, 2014	sju	Updated Ordering Information

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 22.

Table 22. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS8525-AQFP[1]	High Side current sensor companion IC	Tape and Reel (4000 pcs)	32-pin QFN (5x5)
AS8525-AQFM [1]	High Side current sensor companion IC	Tape and Reel (500 pcs)	32-pin QFN (5x5)
AS8525-AQFP-21[2]	High Side current sensor companion IC	Tape and Reel (4000 pcs)	32-pin QFN (5x5)
AS8525-AQFM-21[2]	High Side current sensor companion IC	Tape and Reel (500 pcs)	32-pin QFN (5x5)

1. For version (attenuator ratio 481)
2. For version (attenuator ratio 21)

Note: All products are RoHS compliant and ams green.

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Contact Information:

Headquarters
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com