2M x 32 FLASH
FLASH MEMORY MODULE

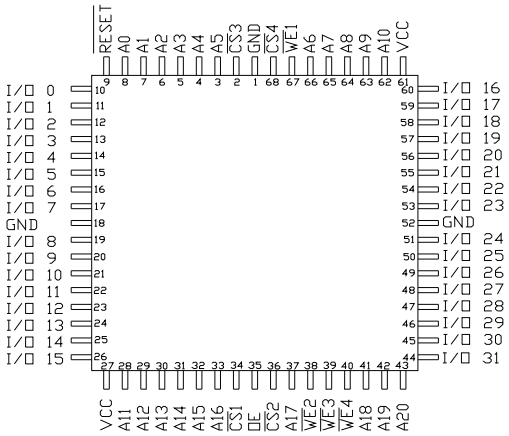
AVAILABLE AS MILITARY SPECIFICATIONS
- Military Processing (MIL-STD-883C para 1.2.2)
- Temperature Range -55C to 125C

FEATURES
- Fast access times of 90ns, 120ns, and 150ns
- 5.0V ±10%, single power supply operation
- Low power consumption(TYP): 4µA CMOS stand-by
  * TYP ICC(active) <120mA for READ/WRITE
- 20 year DATA RETENTION
- Minimum 1,000,000 Program/Erase Cycles per sector guaranteed
- 32 equal sectors of 64 Kbytes each
- Any combination of Sectors can be Erased
- Group Sector Protection
- Supports FULL Chip Erase
- Compatible with JEDEC standards
- Embedded Erase and Program Algorithms
- Data\ Polling and Toggle bits for detection of program or erase cycle completion.
- Erase Suspend/Resume
- Hardware Reset pin (RESET\)
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Separate Power and Ground Planes to improve noise immunity

OPTION	MARKING
• Timing	
90ns	-90
120ns	-120
150ns	-150
• Packages	
Ceramic Quad Flat Pack (0.88" sq)	Q
- MAX height .140"	
- Stand-off Height .035" min	

For more products and information please visit our web site at
www.austinsemiconductor.com

FIGURE 1: PIN ASSIGNMENT
(Top View)



GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8F2M32 is a 64 Mbit, 5.0 volt-only Flash memory. This device is designed to be programmed in-system with the standard system 5.0 volt VCC supply. The AS8F2M32 offers an access time of 90ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable (CE\), write enable (WE\) and output enable (OE\) controls.

The device requires only a single 5.0 volt power supply for both read and write functions. internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the JEDEC single-power-supply FLASH standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-matching that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reaching data out of the device is similar to reading from other FLASH or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically time the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY\ pin, or by reading the DQ7 (DATA\ Polling) and DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

(continued on page 2)

GENERAL DESCRIPTION (cont.)

The Sector Erase Architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

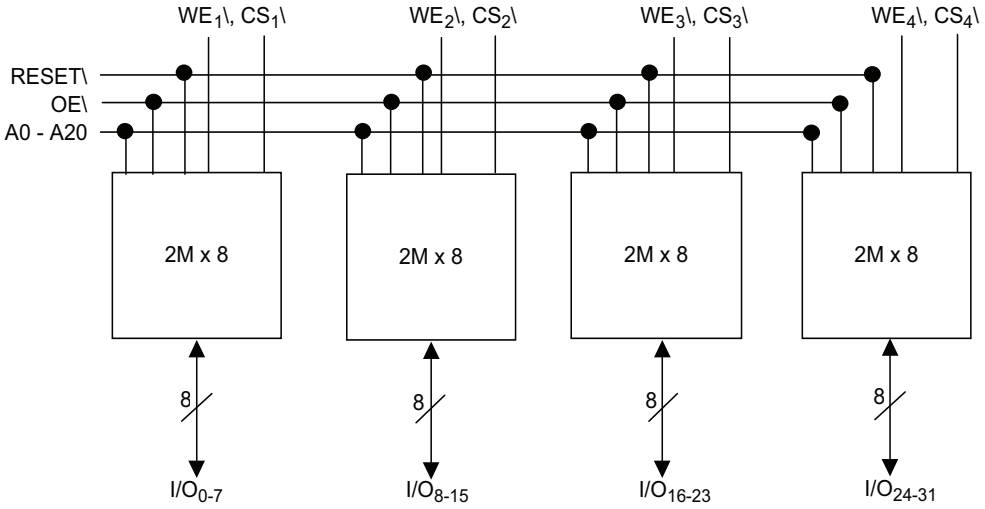
Hardware Data Protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The Hardware Sector Protection feature disables both program and erase operations in any combinations of the sectors of memory. This can be achieved via programming equipment.

The Erase Suspend feature enables the user to put erase on hold for any period of time to read data form, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The Hardware RESET\ pin terminates any operation in progress and resets the internal state machine to reading array data. The RESET\ pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the FLASH memory.

The system can place the device into the standby mode. Power consumption is greatly reduced in this mode.

FIGURE 2: FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

PIN	DESCRIPTION
I/O_{0-31}	Data Inputs/Outputs
A_{0-20}	Address Inputs
$WE\backslash_{1-4}$	Write Enables
$CS\backslash_{1-4}$	Chip Selects
OE\	Output Enable
V_{CC}	Power Supply
GND	Ground
RESET\	Reset

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}, V_T**.....-2.0V to +7.0V
Power Dissipation, P_T.....4W
Storage Temperature, T_{stg}.....-65°C to +125°C
Short Circuit Output Current, I_{OS}(1 output at a time).....100mA
Endurance - Write/Erase Cycles .....100,000 min cycles
Data Retention.....20 years

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(4.5V ≤ VCC ≤ 5.5V , -55°C ≤ T_A ≤ +125°C)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{CC} = 5.5, V_{IN} = GND to V_{CC}	I_{LI}	-10	10	µA
Output Leakage Current	V_{CC} = 5.5, V_{IN} = GND to V_{CC}	I_{LOx32}	-10	10	µA
V_{CC} Active Current for Read	CS\ = V_{IL}, OE\ = V_{IH}	I_{CC1}		160	mA
V_{CC} Active Current for Program or Erase	CS\ = V_{IL}, OE\ = V_{IH}	I_{CC2}		240	mA
V_{CC} CMOS Standby	V_{CC} = 5.5V, All Inputs @ V_{CC} - 0.2V or V_{SS} +0.2V, RESET\ = CS\$_{1-4}$ = V_{CC} -0.2V	I_{SB}		4	mA
V_{CC} Standby Current	V_{CC} = 5.5, CS\ = V_{IH}, RESET\ = V_{CC} ± 0.3V, f=0	I_{CC3}		8	mA
Output Low Voltage	I_{OL} = 12.0 mA, V_{CC} = 4.5	V_{OL}		0.45	V
Output High Voltage	I_{OH} = -2.5 mA, V_{CC} = 4.5	V_{OH}	0.85 x V_{CC}		V
Low V_{CC} Lock-Out Voltage		V_{LKO}	3.2	4.2	V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	---	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	---	+0.8	V

CAPACITANCE (T_A = +25°C)*

PARAMETER	SYM	CONDITIONS	MAX	UNITS
OE\	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
WE\$_{1-4}$	C_{WE}		50	pF
CS\$_{1-4}$	C_{CS}		20	pF
Data I/O	$C_{I/O}$		20	pF
Address input	C_{AD}		50	pF

Parameter is guaranteed, but not tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C)

PARAMETER	SYM		-90		-120		-150		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
WE\ CONTROLLED (WRITE/ERASE/PROGRAM OPERATIONS)									
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Progreamming Operation[1]	t_{WHWH1}			300		300		300	µs
Sector Erase[2]	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time[3]				44		44		44	sec
Chip Erase Time[4]				256		256		256	sec
Output Enable Hold Time[5]		t_{OEH}	10		10		10		ns
RESET\ Pulse Width		t_{RP}	500		500		500		ns
READ-ONLY OPERATIONS									
Read Cycle Time	t_{AVAV}	t_{RC}	90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High[6]	t_{EHQZ}	t_{DF}		20		30		35	ns
Output Enable High to Output High[6]	t_{GHQZ}	t_{DF}		20		30		35	ns
Output Hold from Adresses, CS\ or OE\ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns
RST Low to Read Mode[6]		t_{Ready}		20		20		20	µs
CS\ CONTROLLED (WRITE/ERASE/PROGRAM OPERATIONS)									
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Progreamming Operation[1]	t_{WHWH1}			300		300		300	µs
Sector Erase Time[2]	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time[3]				44		44		44	sec
Chip Erase Time[4]				256		256		256	sec
Output Enable Hold Time[5]		t_{OEH}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1 sec.
3. Typical value for Chip Programming is 14 sec.
4. Typical value for Chip Erase Time is 32 sec.
5. For Toggle an Data Polling.
6. This parameter is guaranteed, but not tested.

AC TEST CONDITIONS

PARAMETER	TYP	UNIT
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

FIGURE 3: AC TEST CURRENT

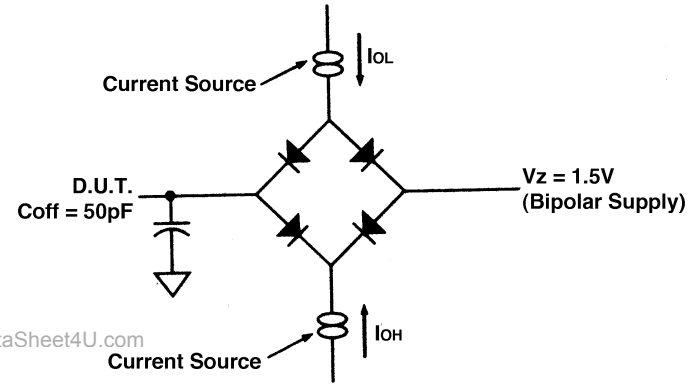


FIGURE 4: RESET Timing Diagram

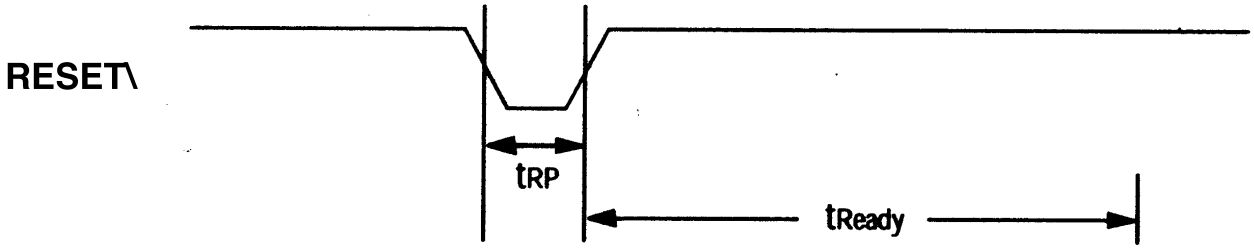


FIGURE 5: AC Waveforms for READ Operations

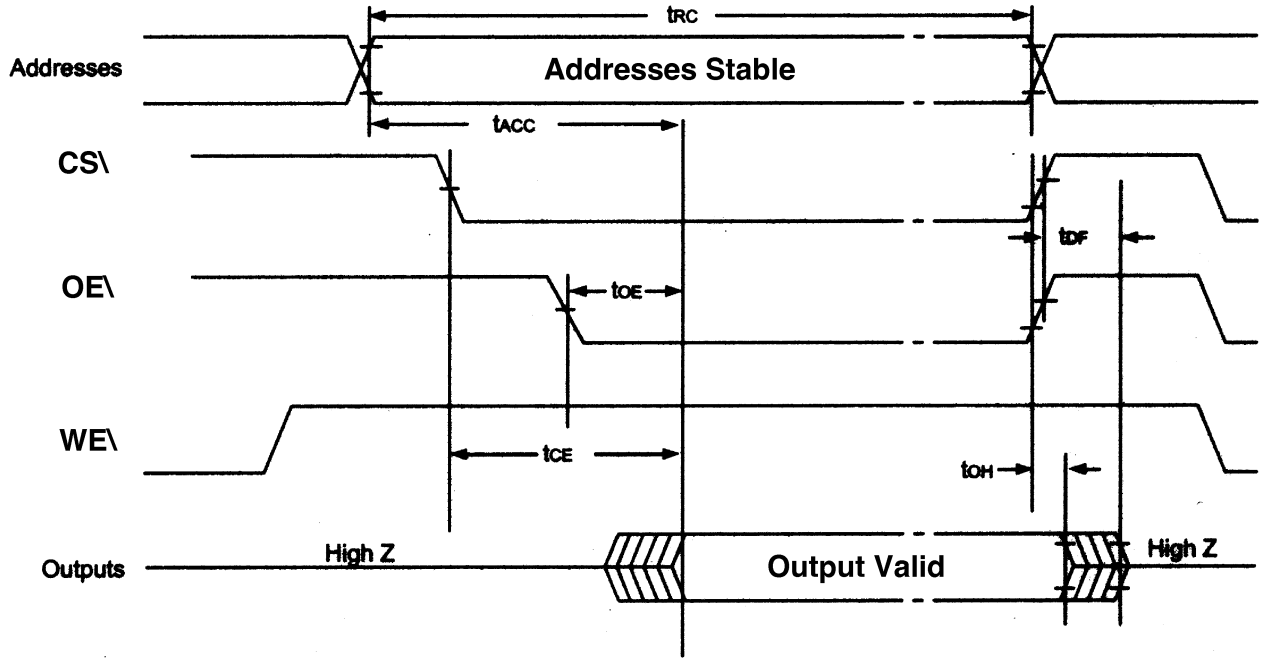
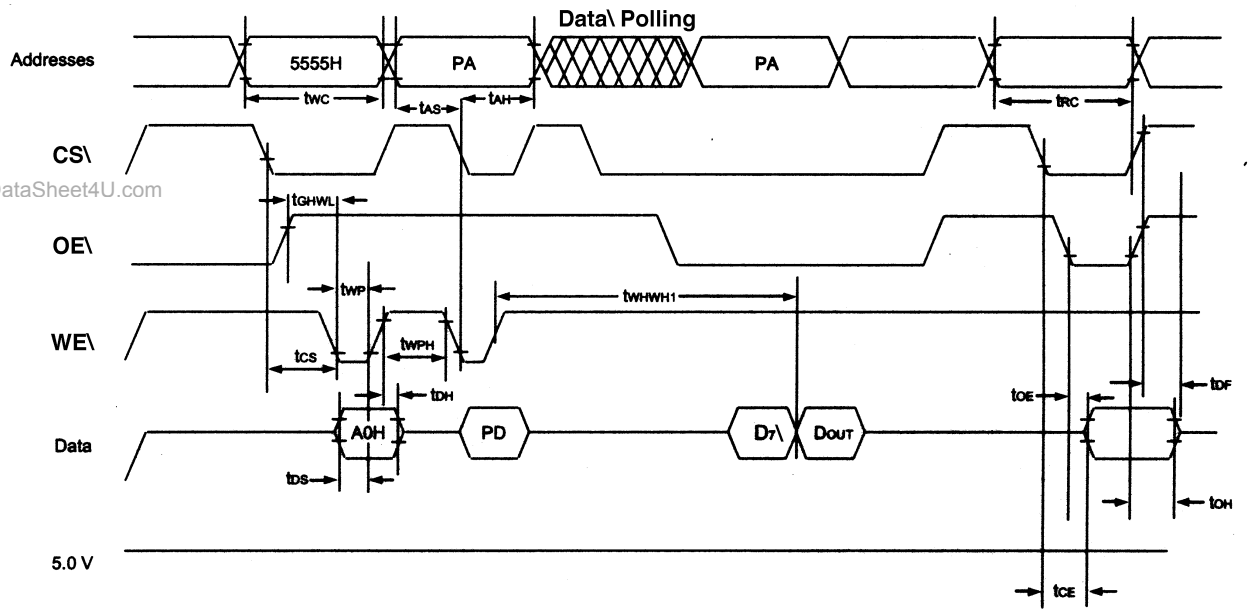


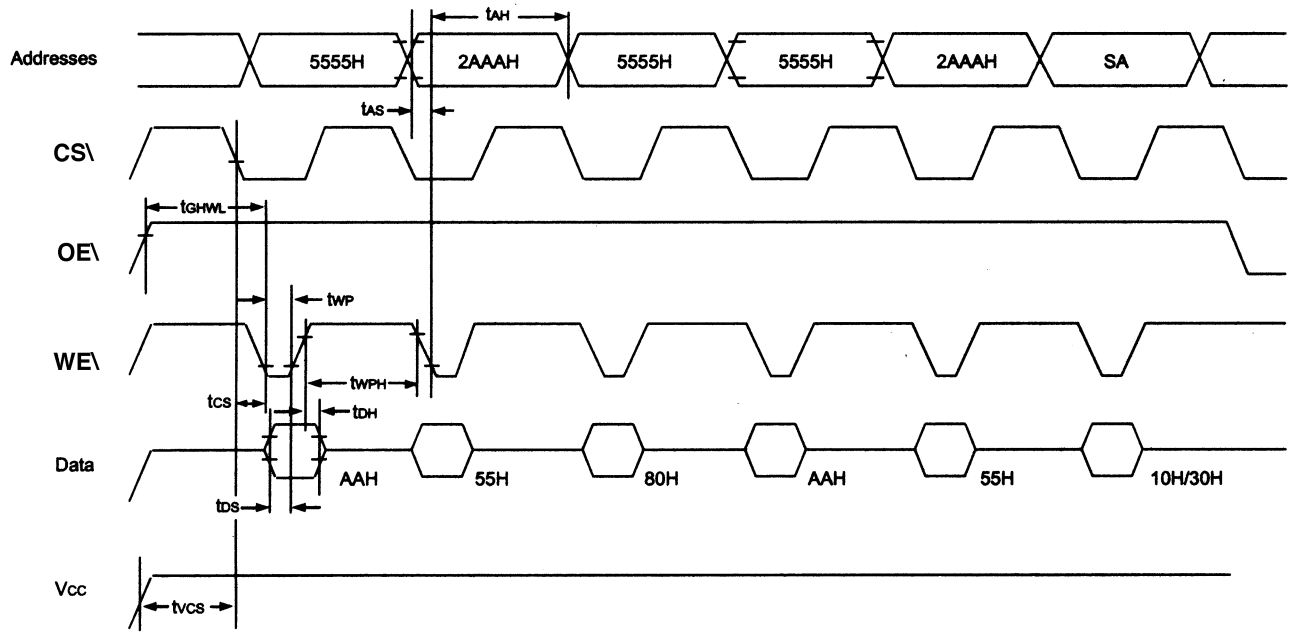
FIGURE 6: WE\ Controlled, WRITE/ERASE/PROGRAM Operation



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D_7\ is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIGURE 7: AC Waveforms Chip/Sector ERASE Operations



NOTES:

1. SA is the sector address for Sector ERASE.

FIGURE 8: AC Waveforms for DATA\ Polling During Embedded Algorithm Operations

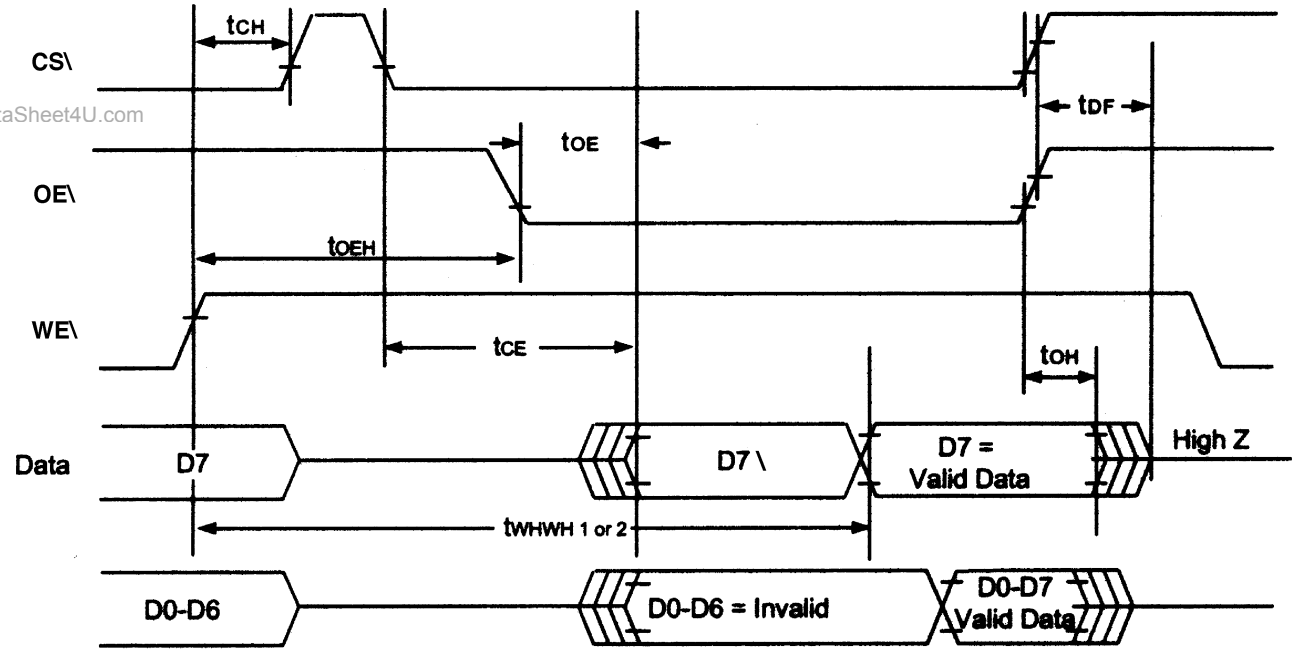
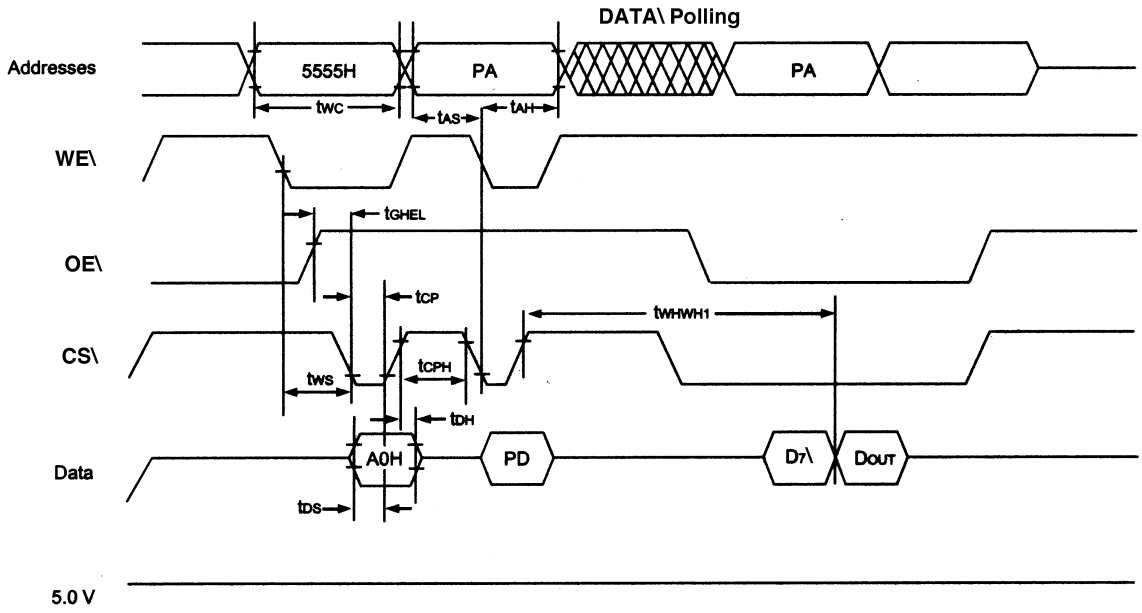


FIGURE 9: Alternate CS\ Controlled Programming Operation Timings

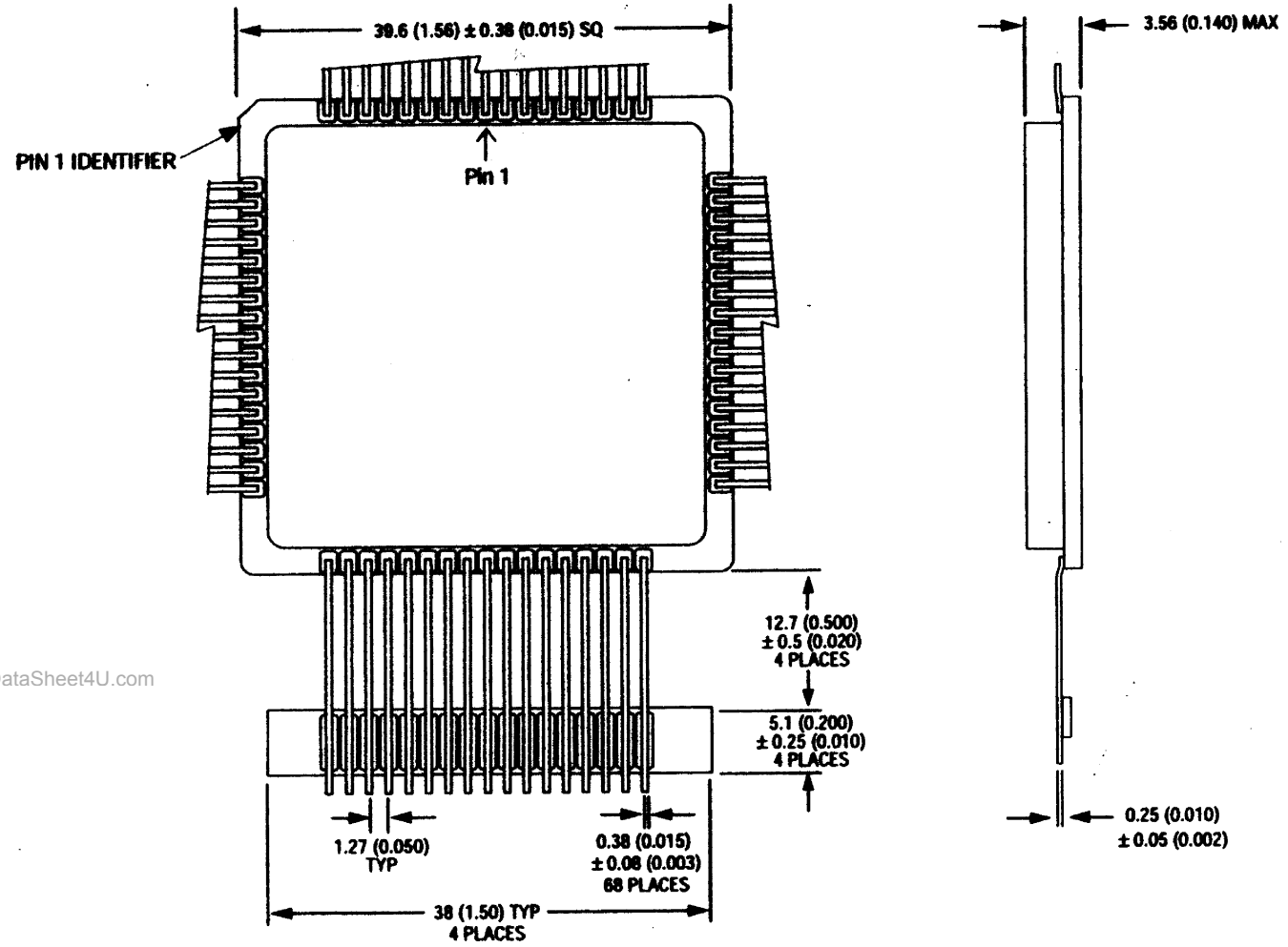


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D_7\ is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

MECHANICAL DEFINITION

ASI Case #703 (Package Designator QW)

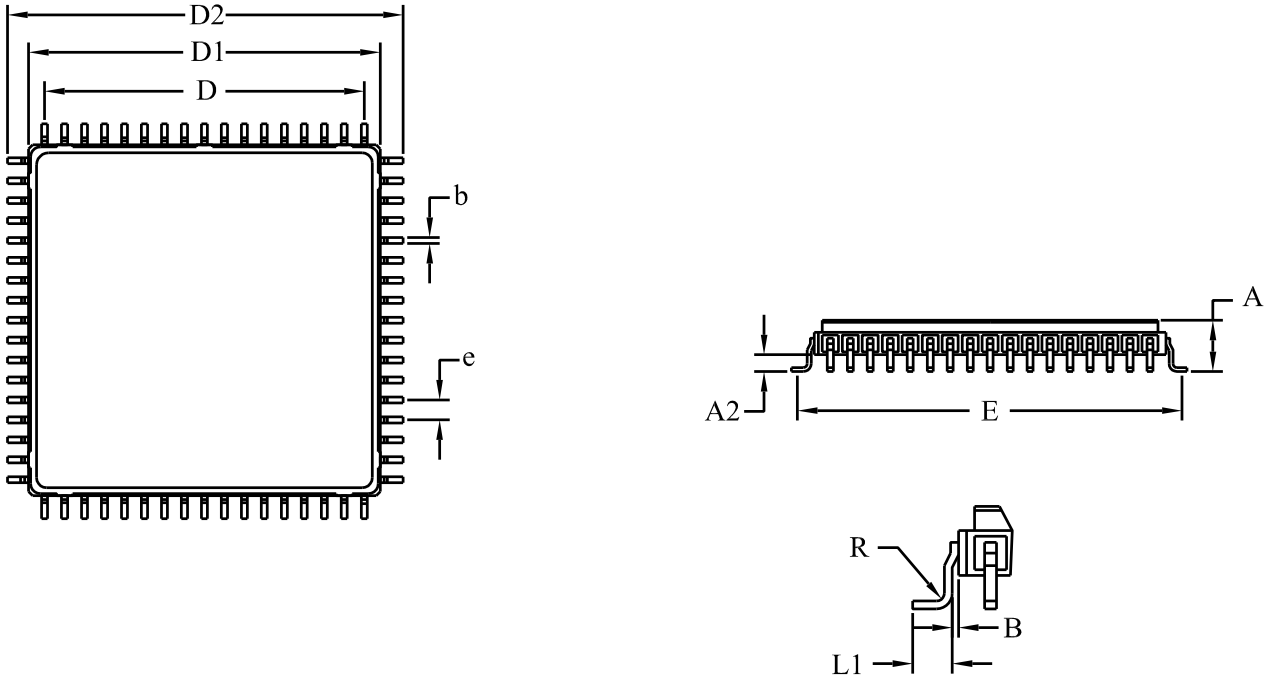


NOTES:

1. Dimensions are shown as millimeters(inches).

MECHANICAL DEFINITIONS*

(Package Designator QT)



ASI PACKAGE SPECIFICATION		
Symbol	Min	Max
A	.120	.140
A2	.035	.049
B	.010 REF	
b	.013	.017
D	.800 BSC	
D1	.870	.890
D2	.980	1.000
E	.936	.956
e	.050 BSC	
R	.010 TYP	
L1	.035	.045
Dimensions in inches		

ORDERING INFORMATION

EXAMPLE: AS8F2M32QW-120/XT

Device Number	Package Type	Speed ns	Process
AS8F2M32	QW	- 90	/*
AS8F2M32	QW	- 120	/*
AS8F2M32	QW	- 150	/*

EXAMPLE: AS8F2M32QT-90/MIL

Device Number	Package Type	Speed ns	Process
AS8F2M32	Q	- 90	/*
AS8F2M32	Q	- 120	/*
AS8F2M32	Q	- 150	/*

*AVAILABLE PROCESSES	Temperature
IT = Industrial Temperature Range	-40°C to +85°C
XT = Extended Temperature Range	-55°C to +125°C
MIL = MIL-STD-883C para 1.2.2 Processing	-55°C to +125°C

NOTE: QW package is planned future offering

DOCUMENT TITLE
64Mb, 2M x 32 Flash Memory Module

REVISION HISTORY

Rev #	History	Release Date	Status
2.5	Updated Order Chart (QT to Q)	May 2009	Release