ALL SHORE INDUSTRIES

ASI-T-370NA2NN/S

Item	Specifications	Unit
Screen size	3.7	inch
Display mode	Transmissive type	-
Active area	48.24(W)×80.4(H)	mm
Display format	480×RGB×800	-
Dot pitch	0.1005(H) X 0.1005(V)	mm
Pixel confinguration	R. G. B. strip	-
Outline Dimensions(typ)	53.54(W)×91.15(H)×1.9(D)	Note 1
View Angle	Full viewing	
Base color Notes	Normaly Black	-
Mass	28.6	g
Driver IC	HX8369	

Note 1: Not include FPCs & Bezel extrude stucture.

RECORDS OF REVISION			

1. Application

This data sheet is to introduce the temporary specification of ASI-T-370NA2NN/S active matrix 16.7M color (**FFS**) TFT LCD module.
Main color LCD module is controlled by Driver IC.
If any problem occurs concerning the items not stated in this temporary specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components, 8 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
Outline: See page 27
Connection: 61 pins;
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Item	Specifications	Unit
Screen size	3.7	inch
Display mode	Transmissive type	-
Active area	48.24(W)×80.4(H)	mm
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Driver IC	HX8369	

Note 1: Not include FPCs & Bezel extrude stucture.

4. Interface signals

Table 2

Pin No.	Symbol	I/0	Description	Remark
1	LED-	P	LED backlight cathode.	
2	LED+	P	LED backlight anode.	
3	YU		NC	
4	XR		NC	
5	YD		NC	
6	XL		NC	
7	VDD2	P	Analog power supply: 2.3V to 4.8V	Notes 4-2
8	VDD1	P	I/O and interface power supply (VDD1): 1.65V to 3.3V	
9	BLU_PWM	O	PWM signal output to control LED driver for LED brightness dimming.	
10	TE	O	Serves TE (Tearing Effect) pin on MPU interface.	
11	BS0	I	Select the MPU interface mode	
12	BS1	I	Select the MPU interface mode	
13	BS2	I	Select the MPU interface mode	
14	BS3	I	Select the MPU interface mode	
15	RESET	I	Reset pin. Setting either pin low initializes the LSI	
16	DB23	I/O	Data bus.	
17	DB22	I/O	Data bus.	
18	DB21	I/O	Data bus.	
19	DB20	I/O	Data bus.	
20	DB19	I/O	Data bus.	
21	DB18	I/O	Data bus.	
22	DB17	I/O	Data bus.	
23	DB16	I/O	Data bus.	
24	DB15	I/O	Data bus.	
25	DB14	I/O	Data bus.	
26	DB13	I/O	Data bus.	
27	DB12	I/O	Data bus.	
28	DB11	I/O	Data bus.	
29	DB10	I/O	Data bus.	
30	DB9	I/O	Data bus.	
31	DB8	I/O	Data bus.	
32	DB7	I/O	Data bus.	
33	DB6	I/O	Data bus.	
34	DB5	I/O	Data bus.	
35	DB4	I/O	Data bus.	
36	DB3	I/O	Data bus.	

37	DB2	I/O	Data bus.	
38	DB1	I/O	Data bus.	
39	DB0	I/O	Data bus.	
40	RDX	I	Read/Write disable, 1: Read / Write enable	
41	WRX_DCX	I	Serves as a write signal and write data at the low level. /0: Read/Write disable, 1: Read / Write enable.	
42	DCX_SCL	I	DBI Type-A/B: Data / Command Selection pin DBI Type-C: it servers as SCL (Serial Clock)	
43	CSX	I	Chip select signal.	
44	SDI	I	Serial data input pin in serial interface operation.	
45	SDO	O	Serial data output. Let it to open in MPU interface mode.	
46	VSYNC	I	Line synchronizing signal.	
47	HSYNC	I	Serves VS signal pin on RGB interface. (Input pad).	
48	DE	I	A data enable signal in RGB I/F mode. Has to be fixed to VSSD level in MPU interface mode.	
49	PCLK	I	Dot clock signal.	
50	DSI_LDO_ENB	I	DSI I/F:Control signal of DSI_LDO. The default setting of DSI_LDO_ENB is Low .	
51	DSI_VSS	P	MIPI DSI analogy ground	
52	DSI_D0N	I	MIPI-DSI Data differential signal input pins.	
53	DSI_D0P	I	MIPI-DSI Data differential signal input pins.	
54	DSI_VSS	P	MIPI DSI analogy ground	
55	DSI_D1N	I	MIPI-DSI Data differential signal input pins.	
56	DSI_D1P	I	MIPI-DSI Data differential signal input pins.	
57	DSI_VSS	P	MIPI DSI analogy ground	
58	DSI_CLKN	I	MIPI-DSI CLOCK differential signal input pins.	
59	DSI_CLKP	I	MIPI-DSI CLOCK differential signal input pins.	
60	DSI_VSS	P	MIPI DSI analogy ground	
61	VDD3	P	Logic power supply (VDD3): 2.3V to 4.8V	Notes 4-2

Notes: The direction is named with respect to the display module, I = from host to module, O = from module to host. The input must be connected to VSSD or VDD1 if not used.

[Notes 4-1**]: FPC Connector Type**

Table 4

Assembled on	Item	Description
Phone PWB	Connector Type	FPC Connection
	Pin Amount	61
	Manufacturer	HRS
	Part Number	FH26-61S-0.3SHW(0.5)

[Notes 4-2**]:**VDD2 input level should be same as VDD3 input level to avoid the level-mismatching at internal level shifter circuit.

5. Absolute Maximum Ratings

(5-1) Electrical absolute maximum ratings

Table 5

Parameter(requirement)	Symbol	Rating	Unit
Analog power supply	VDD2	-0.3 to +4.4	
I/O and interface power supply	VDD1	-0.3 to +3.3	V
Logic power supply	VDD3	-0.3 to +4.4	V
Logic Signal Input Voltage	V_I	-0.3 to VDD3+0.5	V
Logic Signal Output Voltage	V_O	-0.3 to VDD3+0.5	V

(5-2) Environment Conditions

Table 6

Item	Top		Tstg		Remark
	Min	Max	Min	Max	
Ambient temperature	-20℃	+70℃	-30℃	+80℃	Note 2
Humdity	Note 1		Note 2		No condensation

(**Note1**) Ta ≤ 40 ° C.....95 % RH Max

(**Note2**) Ta > 40 ℃.....Absolute humidity shall be less than Ta=40 ℃ /95 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ℃ a nd it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

6. Electrical Specifications

(6-1) Electrical characteristics

Table 7

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Driver IC(Analog) Power Supply Voltage	VDD2	2.3	2.8	3.3	V	[Note6-1]
Driver IC(Digital) Power Supply Voltage	VDD3	2.3	2.8	3.3	V	[Note6-1]
I/O and interface power supply	VDD1	1.7	1.8	3.3		
Input Voltage(Low)	V_{IL}	0	-	0.3VDD1	V	[Note6-1]
Input Voltage(High)	V_{IH}	0.7VDD1	-	VDD1	V	[Note6-1]
Input Current(Low)	I_{IL}	-10	-	-	uA	
Input Curent(High)	I_{IH}	-	-	10	uA	
Output Voltage(Low)	V_{OL}	0	-	0.2VDD1	V	I_{OL}=+0.1mA
Output Voltage(High)	V_{Oh}	0.8VDD1	-	VDD1	V	I_{OH}=-0.1mA
Power Consumption	P_{norm}	-	85	-	mW	[Note6-1]
	P_{SLEEP}	-	10	-	mW	[Note6-1]

	$P_{Deepsleep}$	-	1.0	-	mW	[Note6-1]

[Note6-1]:

1. Conditions : Ta = 25℃, VDD 2=VDD3= 2.8V, VDD1= 1.8V,Refresh rate=60Hz.
   Ambient temperature,Ta = -20℃ to +70℃ operational
   Measurement Point

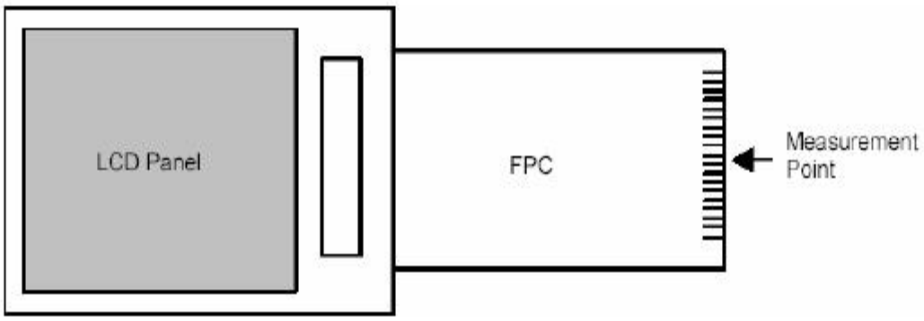


Fig.2

(6-2) LED back light

At main panel the back light uses 8 pcs edge light type white LED.

Table 8

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Voltage	VLED	-	25.6	27.2	V	[Note 5-2]
LED Current	ILED	-	20	30	mA	
Power Consumption	WLED	-	512	816	mW	[Note 5-2]
Number of LED components		8			PCS	
Connection Type (Serial/Parallel/Other)		8 LEDs in Serial				

Note:

*8 pcs of LED

*Please consider Allowable Forward Current on used temperature
(refer to Ambient Temperature vs. Allowable Forward Current curve Fig.3)

■ Ambient Temperature vs.
Allowable Forward Current

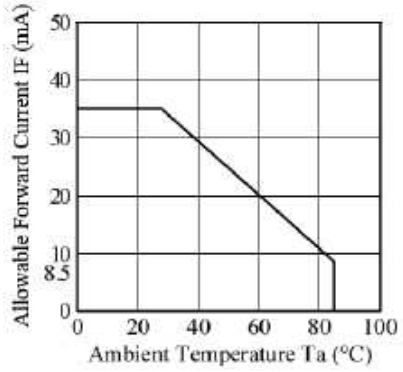


Fig.3

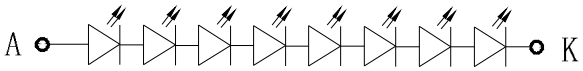


Fig.4*Schematics drawing of lighting (Fig.4)

(6-3) 80-System Interface (MPU Interface) Timing Diagrams

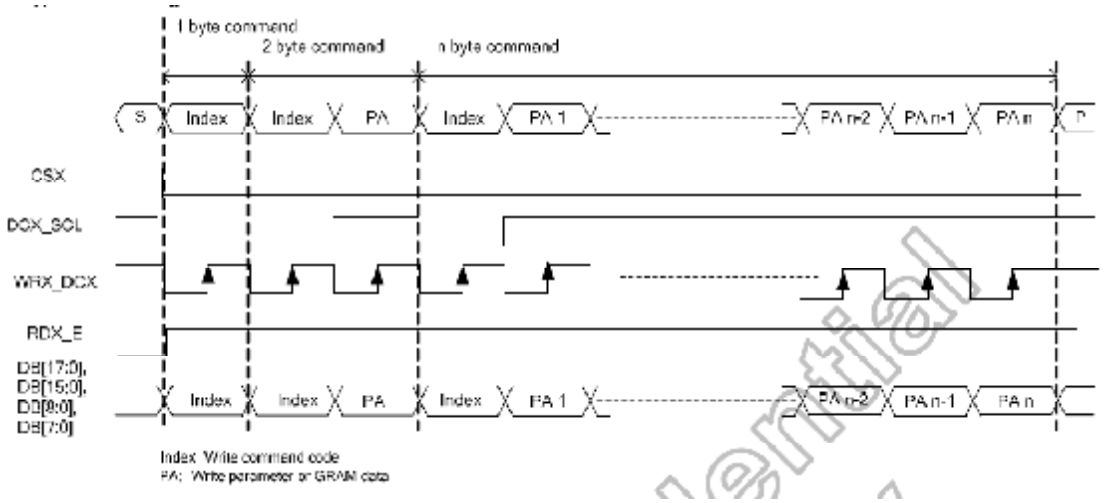


Fig.5 80-System system interface protocol, write to register or GRAM

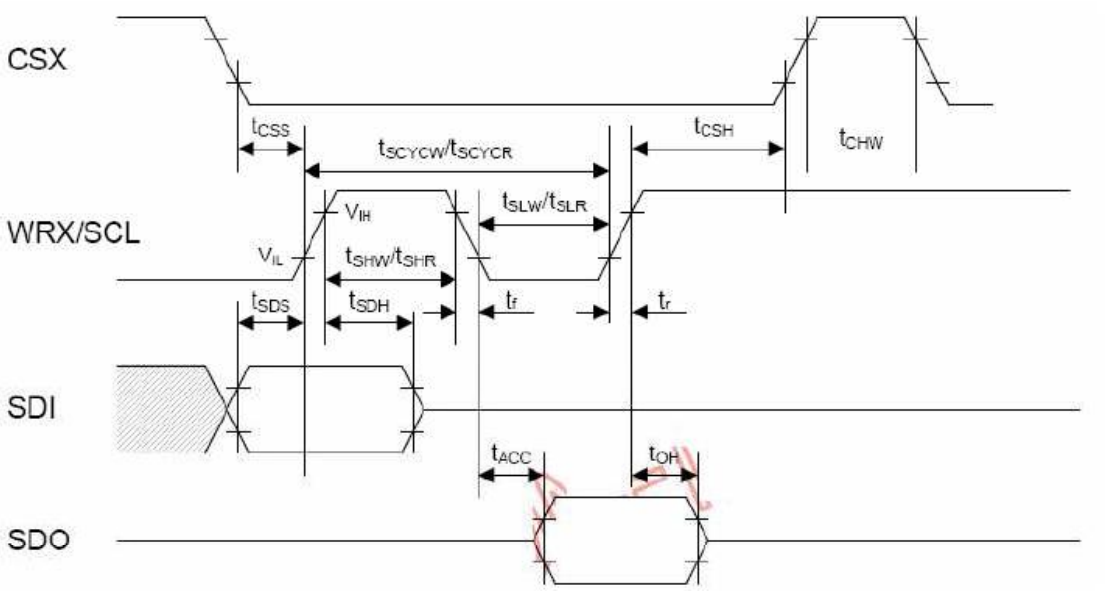
Table 9

Item	Symbol	Timing Diagram	Min	Typ	Max	Unit
Write cycle time	tWC	Figure.110	66	-	-	ns
Read cycle time	tRC	Figure.110	160	-	-	ns
Write control pulse "Low" duration	tWRL	Figure.110	33	-	-	ns
Read control pulse "Low" duration	tRDL	Figure.110	45	-	-	ns
Write control pulse "High" duration	tWRH	Figure.110	33	-	-	ns
Read control pulse "High" duration	tRDH	Figure.110	90	-	-	ns
Write setup time (DCX to CSX, WRX)	tAST	Figure.110	0	-	-	ns
Read setup time (DCX to CSX, RDX)	tAST	Figure.110	10		-	ns
Address hold time	tAHT	Figure.110	2	-	-	ns
Write data setup time	tDST	Figure.110	15	-	-	ns
Write data hold time	tDHT	Figure.110	10	-	-	ns
Read data access time	tRAT	Figure.110	-	-	40	ns
Read data hold time	tODH	Figure.110	5	-	-	ns

Note: Logic high and low levels are specified as 30% and 70% of VDD3 for Input signals.

Note: Ta = -30 to 70 ℃, VDD3=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

(6-4) 3-wire 9bit Serial Interface Timing Diagrams



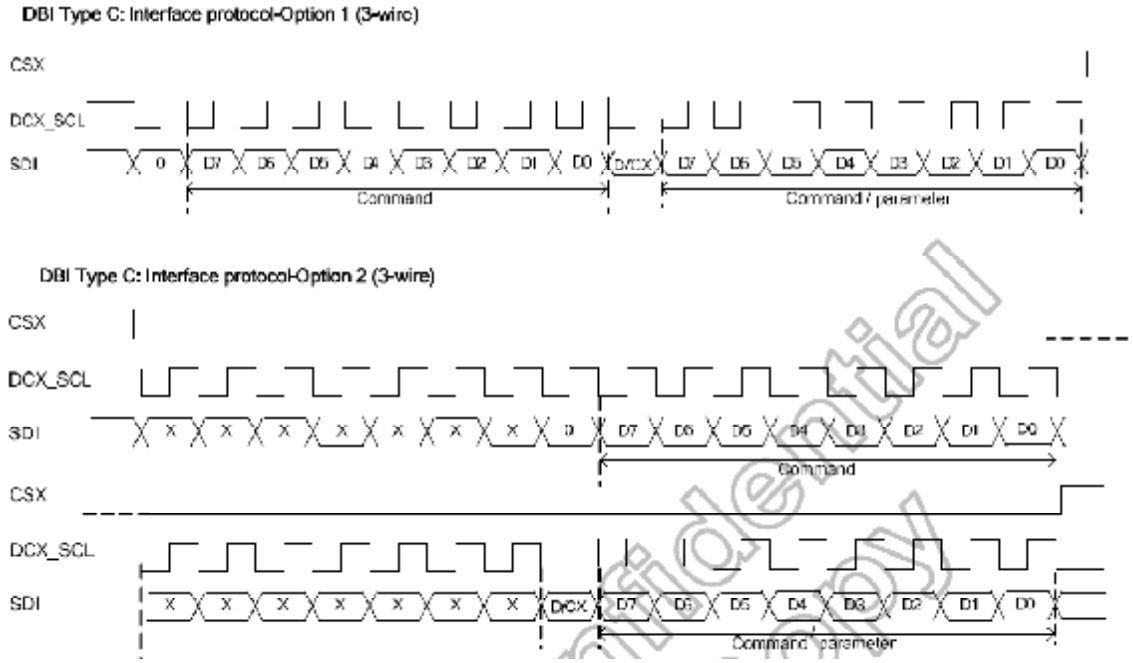
VDD3=1.65~3.3V, VDD=2.5~3.3V, TA=25℃

Fig.6

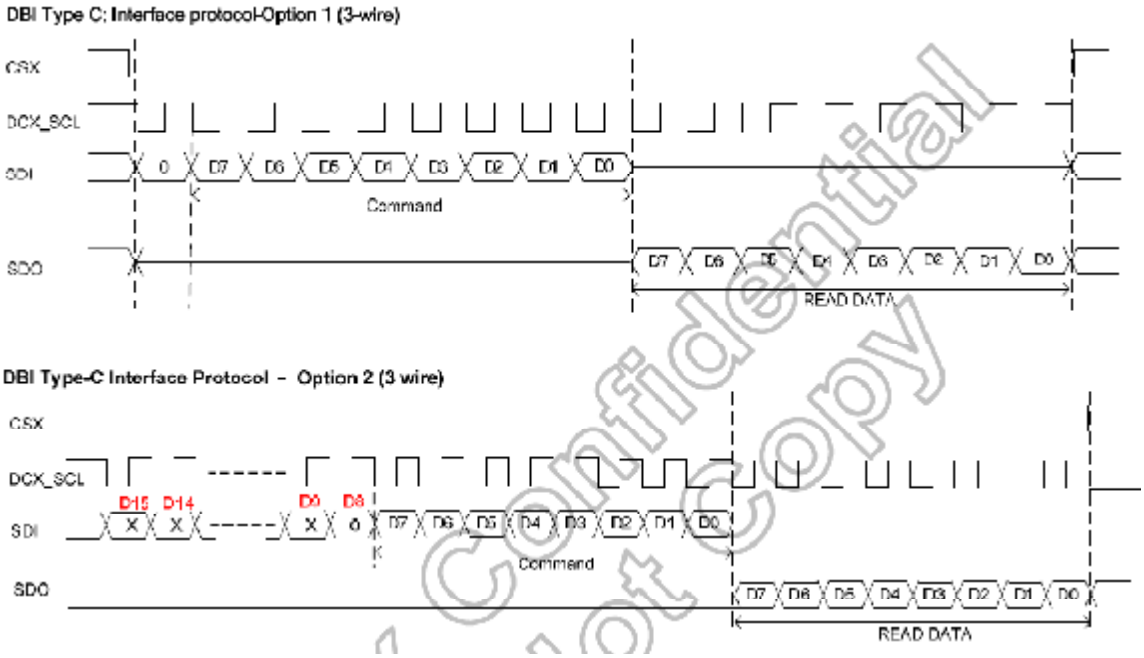
Table 10

Signal	Symbol	Patameter	Min	Max	Unit	Description
CSX	t_{css}	Chip select setup time (Write)	40		ns	
	t_{csh}	Chip select hold time (Write)	40		ns	
D/CX	t_{as}	Address setup time	10		ns	
	t_{ah}	Address hold time(Write/Read)	10		ns	
WRX/SCL (Wrilte)	t_{wc}	Write cycle	100		ns	
	t_{wrh}	SCL High duration (Write)	40		ns	
	t_{wrl}	SCL Low duration(Wtite)	40		ns	
WRX/SCL (Read)	t_{rc}	Read cycle	300		ns	
	t_{rdh}	SCL High duration(Read)	120		ns	
	t_{rdl}	SCL Low duration(Read)	120		ns	
DIN/SDA (Driver IC)	t_{ds}	Data setup time	30		ns	
	t_{dh}	Data hold time	30		ns	
DOUT (Driver IC)	t_{acc}	Access time	-	110	ns	
	t_{od}	Output disable time	10		ns	

(6-5) 3-wire Serial Interface Write Mode/Read Mode



Serial bus protocol, register write mode



Serial bus protocol, register read mode

(6-6) General Timing Diagram for RGB

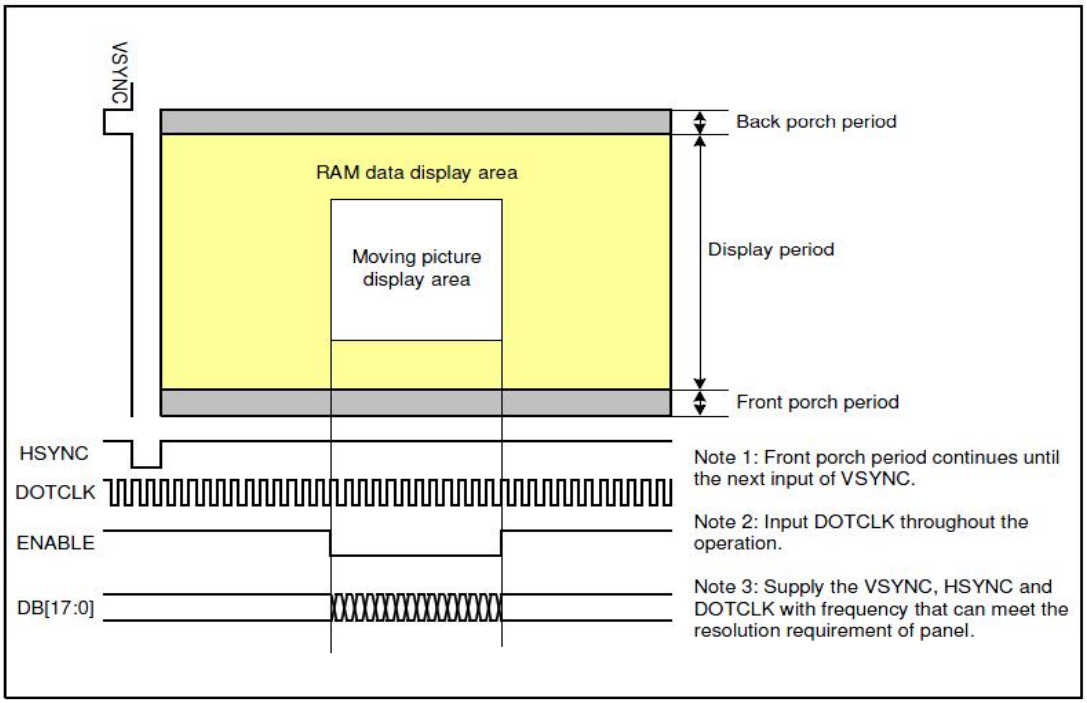


Fig.7

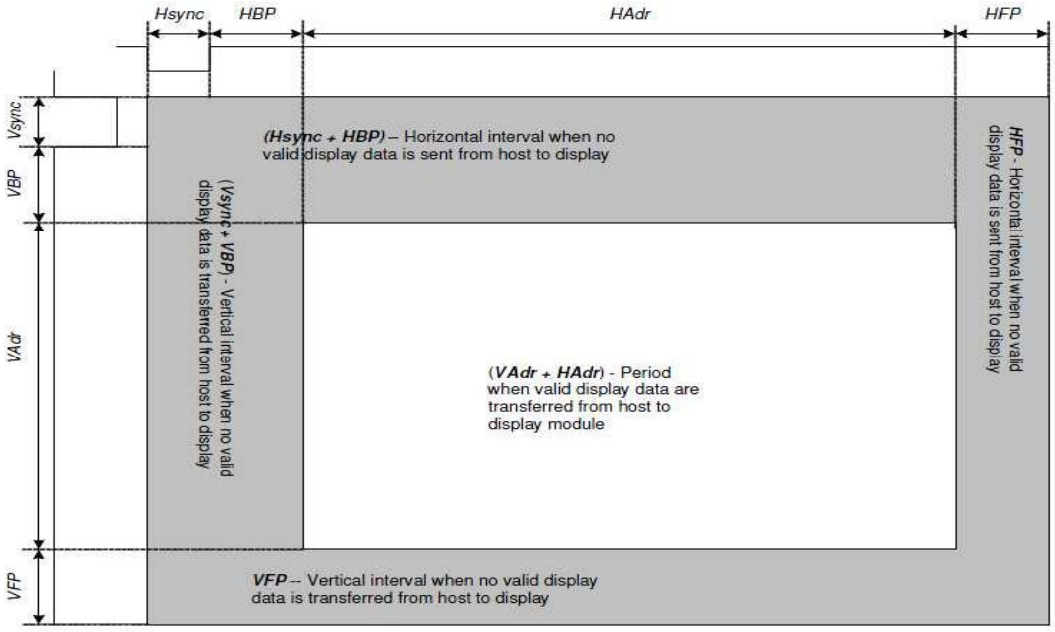


Fig.8

Table 11

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
PCLK Cycle	$PCLK_{CYC}$		-	49.8	-	ns
Horizontal Synchronization	Hsync		5	9	-	PCLK
Horizontal Back Porch	HBP		5	30	-	PCLK
Horizontal Address	Hadr		480	480	-	PCLK
Horizontal Front Porch	HFP		5	16	-	PCLK
Vertical Synchronization	Vsync		2	5	-	Line
Vertical Back Porch	VBP		2	3	-	Line
Vertical Address	Vadr		800	800	-	Line
Vertical Front Porch	VFP		2	3	-	Line
Vsync setup time	VSST		10		-	Hz
Vsync hold time	VSHT		10		-	Hz
Hsync setup time	HSST		10		-	Hz
Hsync hold time	HSHT		10		-	Hz
Data setup time	DST		10		-	Hz
Data hold time	DHT		10		-	Hz
Vertical Frequency(*)			55	60	70	Hz
Horizontal Frequency(*)			-	-	-	KHz
PCLK Frequency(*)			22	23.5	34	MHz

(6-7) Detailed Timing for RGB

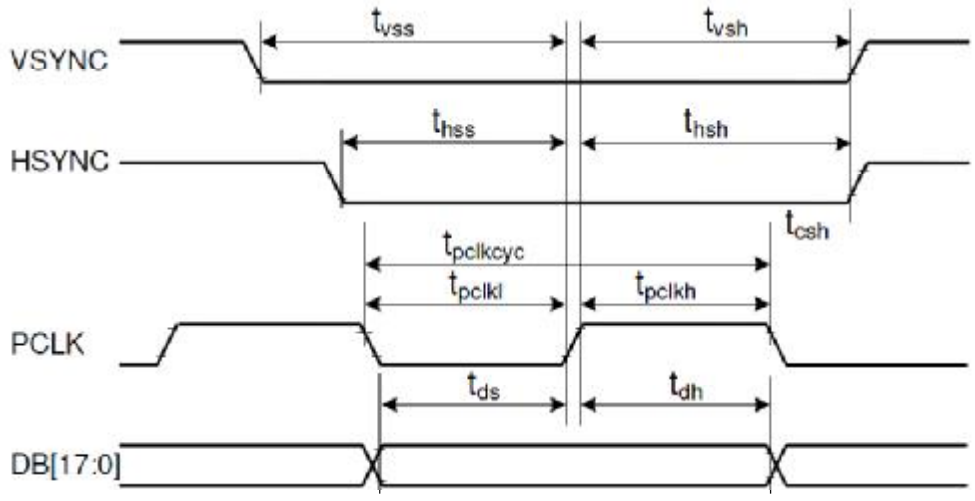


Fig.9

Table 12

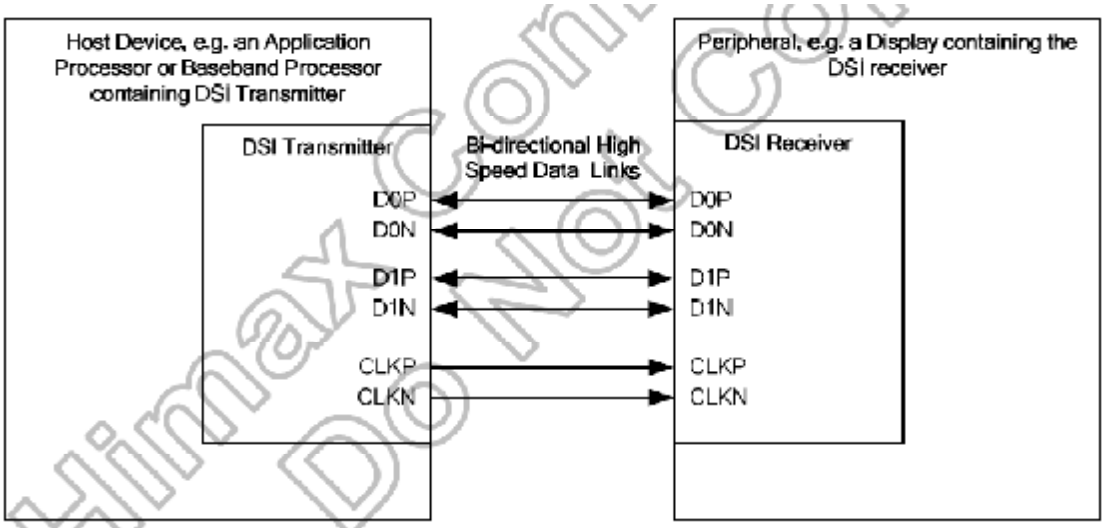
Parameter	Symbol	Condition	Min.	Max.	Unit
Vsync setup Time	t_{vss}		15		ns
Vsync hold Time	t_{vsh}		15		ns
Hsync setup Time	t_{hss}		15		ns
Hsync hold Time	t_{hsh}		15		ns
Pixel Clock Duty Cycle	$t_{pclkcyc}$		35	67	%
Pixel Clock Low Duration	t_{pclkl}		15		ns
Pixel Clock High Duration	t_{pclkh}		15		ns
Data setup Time	t_{ds}		15		ns
Data Hold Time	t_{dh}		15		ns

(6-8) DSI system interface

The selection of interface is by BS(3-0) =”1000 “ or “1100”, the DSI specifies the interface between a host processor and a peripheral such as a display module.

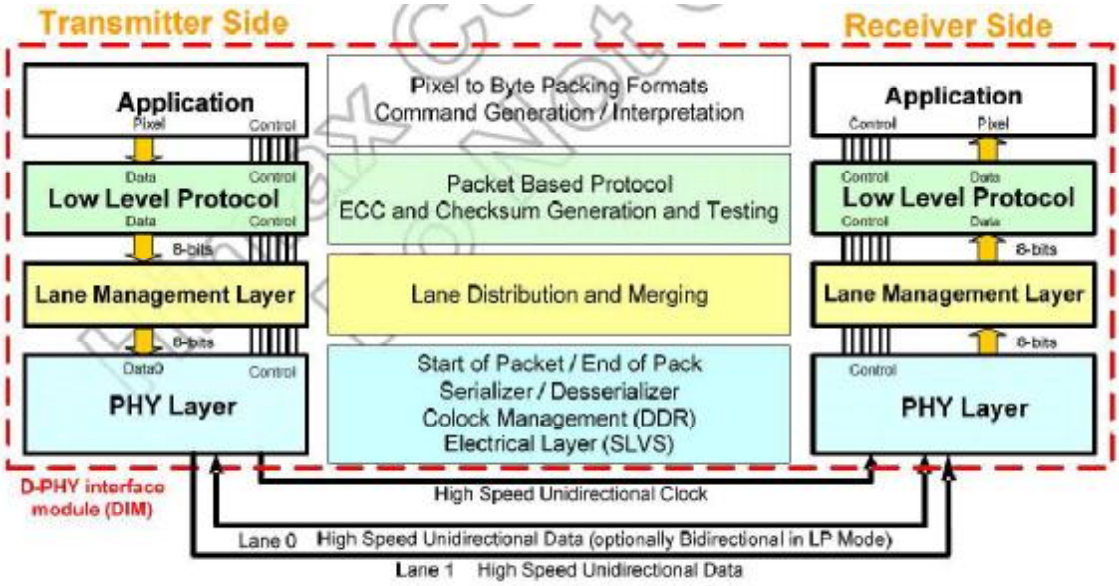
As to basic specification of driver IC refer to the IC specification and handbook.

(6-8-1) Schematic of DSI system interface system



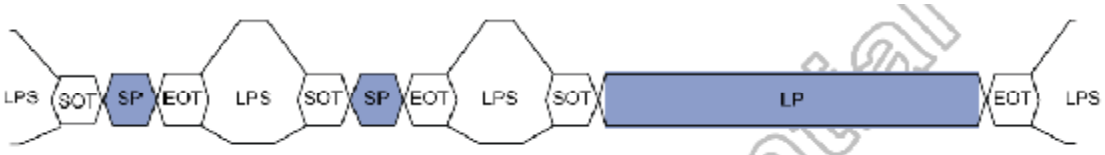
(6-8-2) DSI layer definitions

According DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer



(6-8-3)DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup.



LPS : Low power state
SOT : Start of Transmission
SP : Short Packet
LP : Long Packet
EOT : End of Transmission

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the

number of parameters depending on the command type.

As to basic specification of driver IC refer to the IC specification and handbook.

(6-8-3) Processor to peripheral direction packets data types

The set of transaction types sent from the host processor to a peripheral.

such as a display module, are shown in DATASHEET OF DRIVER IC (HX8369) Data Types for Processor-sourced Packets.

(6-8-4) Peripheral to processor (reverse direction)

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets may use ECC and Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

As to basic specification of driver IC refer to the IC specification and handbook.

(6-9) /Reset Input Timing

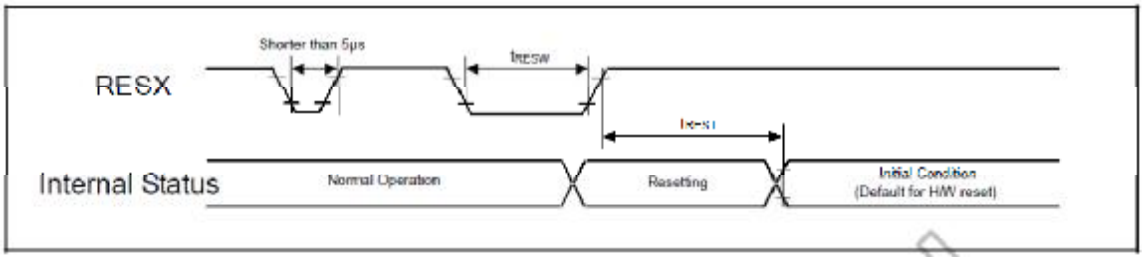


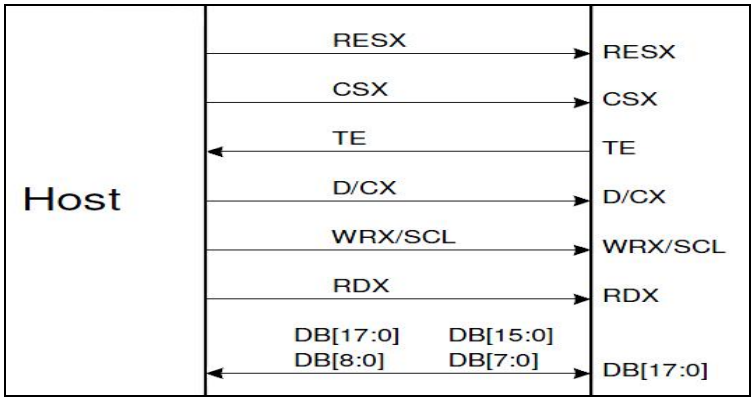
Fig.10

Table 13

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
t_{RESW}	Reset low pulse width	30	-	-	us	-
t_{REST}	Reset complete time	-	-	120	ms	-

(6-10) Schematic of LCD MPU Interface system （）

Fig.11



(6-11) Power On/Off Characteristics

Recommended Power On / Off Sequence

The LCD adopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:

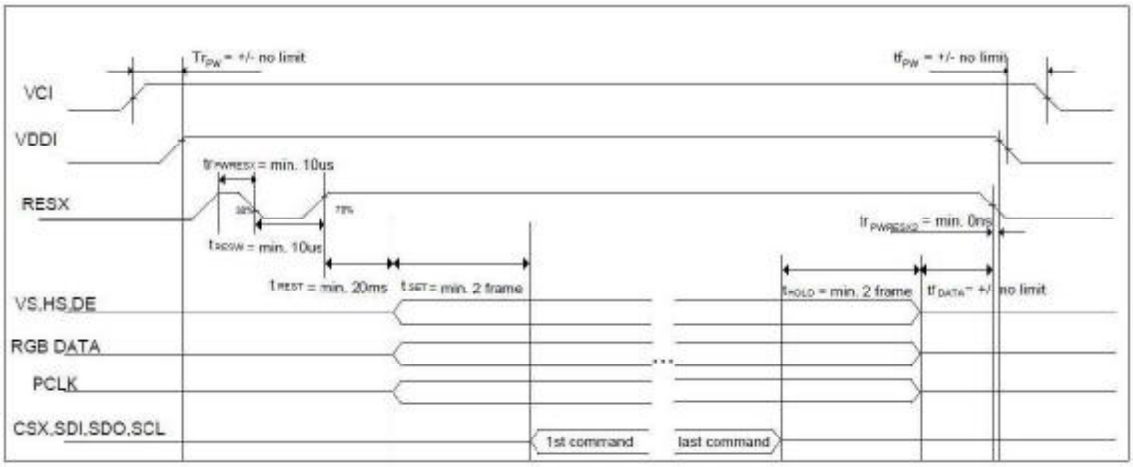


Fig.11

7. Optical Characteristics

Table 14

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	Tr	θ=0°	-	(10)	35	ms	Note 4
	Fall	Tf		-	(15)	35	ms	

Brightness		Br	θ=0°	240	300	-	Cd/m^2	Note 1,2
Contrast ratio		CR	θ=0°	600	800	-	-	Note 1,2,3
Viewing angle(with Polarizer)	Top		CR≥10	80	85	-	degree	Note 1
	Bottom			80	85	-		
	Left			80	85	-		
	Right			80	85	-		
White Chromaticity		X	CIE	0.270	0.310	0.350	-	-
		Y		0.280	0.336	0.370	-	-
NTSC			-	-	60	-	%	-

***VDD=2.8V,Ta=25℃**

Note 1) Definition of range of visual angle

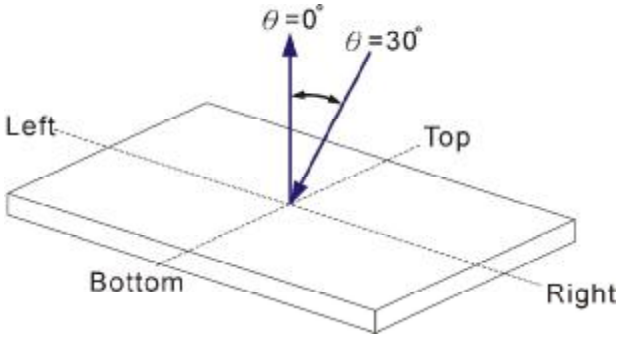


Fig.12

(Note 2) To be measured at the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7, after 10 minutes operation (module).

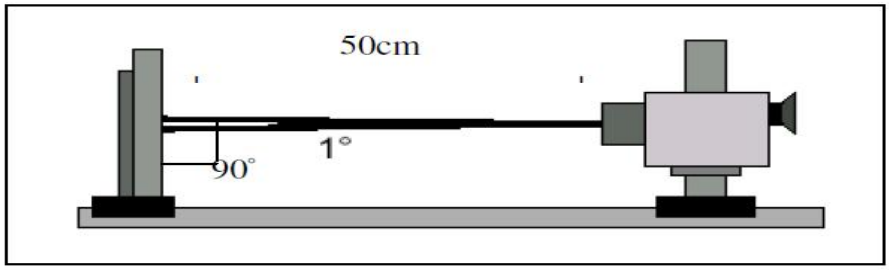


Fig. 13

Note 3) Contrast ratio is defined as follows:

$$\text{Contrast ratio(CR)} = \frac{\text{Photodetector output with all pixels white (GS63)}}{\text{Photodetector output with all pixels black (GS0)}}$$

Note 4) Response time is defined as follows:

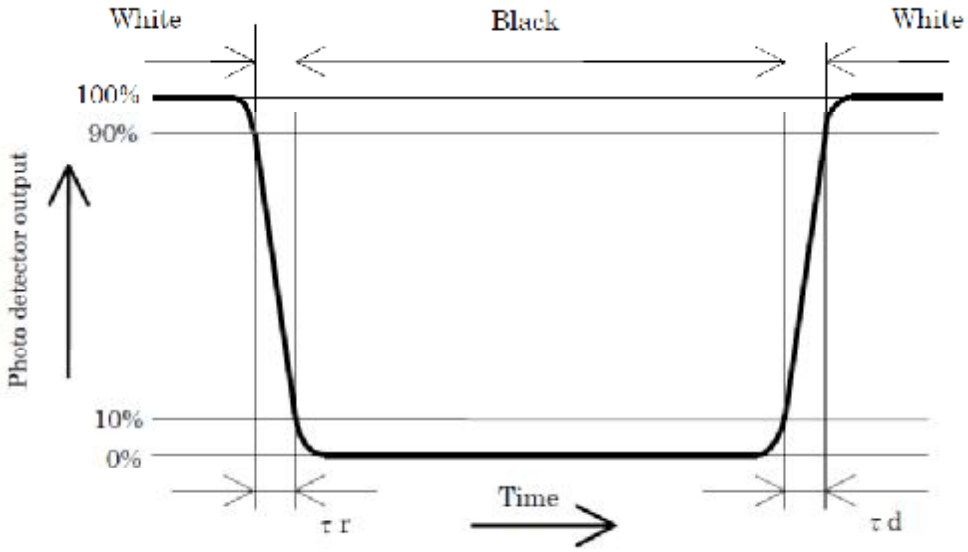


Fig. 14

8. Initial Code

（8-1）Recommended Power On Register Setting（TBD）

Table 15

ITEM	Register Address	Register Data list	REMARK
VDD3(1.8V),VDD(2.8V) ON (anytime VDD3O≦VCI),RESX=H			
WAIT until power stable			
RESX=L			
Delay 50ms(This delay time is necessary)			
RESX=H(Reset release)			
Delay 100 ms			
SET password	*0xB9*	*0xFF*	
		0x83	
		0x69	
SET Display 480x800	*0xB2*	*0x00*	
		0x23	
		0X03	
		0X03	
		0X70	
		0X00	
		0XFF	
		0X00	
		0X00	
		0X00	
		0X00	
		0X03	
		0X03	
		0X00	
		0X01	
SET Display waveform	*0xB4*	*0x00*	

		0X18	
		0X80	
		0X06	
		0X02	
SET VCOM	0XB6	0X42	
		0X42	
SET GIP	*0xD5*	0X00	
		0X04	
		0X03	
		0X00	
		0X01	
		0X05	
		0X28	
		0X70	
		0X01	
		0X03	
		0X00	
		0X00	
		0X40	
		0X06	
		0X51	
		0X07	
		0X00	
		0X00	
		0X41	
		0X06	
		0X50	
		0X07	
		0X07	
		0X0F	
		0X04	
		0X00	
Set Power	0XB1	0X85	
		0X00	
		0X34	
		0X07	
		0X00	
		0X0F	
		0X0F	
		0X2A	
		0X32	
		0X3F	
		0X3F	
		0X01	
		0XE6	
		0XE6	
		0XE6	

		0XE6	
		0XE6	
SET GAMMA 2.2	0XE0	0X00	
		0X13	
		0X19	
		0X38	
		0X3D	
		0X3F	
		0X28	
		0X46	
		0X07	
		0X0D	
		0X0E	
		0X12	
		0X15	
		0X12	
		0X14	
			14
		0X0F	
		0X17	
		0X00	
		0X13	
		0X19	
		0X38	
		0X3D	
		0X3F	
		0X28	
		0X46	
		0X07	
		0X0D	
		0X0E	
		0X12	
		0X15	
		0X12	
		0X14	
		0X0F	
		0X17	
SET DGC	0XC1	0X01	
		0X04	
		0X0A	
		0X13	
		0X1A	
		0X21	
		0X29	
		0X31	
		0X37	
		0X3E	
		0X47	

		0X4F	
		0X56	
		0X5E	
		0X65	
		0X6E	
		0X78	
		0X80	
		0X88	
		0X8F	
		0X98	
		0XA0	
		0XA8	
		0XA8	
		0XB1	
		0XBA	
		0XC3	
		0XCB	
		0XD3	
		0XDB	
		0XE4	
		0XEB	
		0XF3	
		0XFA	
		0XFF	
		0X20	
		0X35	
		0XE6	
		0X2D	
		0X8C	
		0X29	
		0XE3	
		0X2F	
		0XC0	
		0X04	
		0X0A	
		0X13	
		0X1A	
		0X21	
		0X29	
		0X31	
		0X37	
		0X3E	
		0X47	
		0X4F	
		0X56	
		0X5E	
		0X65	

		0X6E	
		0X78	
		0X80	
		0X88	
		0X8F	
		0X98	
		0XA0	
		0XA8	
		0XB1	
		0XBA	
		0XC3	
		0XCB	
		0XD3	
		0XDB	
		0XE4	
		0XEB	
		0XF3	
		0XFA	
		0XFF	
		0X20	
		0X35	
		0XE6	
		0X2D	
		0X8C	
		0X29	
		0XE3	
		0X2F	
		0XC0	
		0X04	
		0X0A	
		0X13	
		0X1A	
		0X21	
		0X29	
		0X31	
		0X37	
		0X3E	
		0X47	
		0X4F	
		0X56	
		0X5E	
		0X65	
		0X6E	
		0X78	
		0X80	
		0X88	
		0X8F	

		0X98	
		0XA0	
		0XA8	
		0XB1	
		0XBA	
		0XC3	
		0XCB	
		0XD3	
		0XDB	
		0XE4	
		0XEB	
		0XF3	
		0XFA	
		0XFF	
		0X20	
		0X35	
		0XE6	
		0X2D	
		0X8C	
		0X29	
		0XE3	
		0X2F	
		0XC0	
SET pixel format 24-bit	*0x3A*	**0X77**	
sleep out command	*0x11*	**-----**	
Delay 120 ms			
display on command	*0x29*	**------**	
Wait for more than 120ms (Delay Time : Typ. 120ms , Min.50ms)			
Backlight On			

Notes:

1. Undefined commands are treated as NOP (00h) command.
2. C=command, W=write, R=read, +=number of following parameters, (in Bytes), d=dummy clock cycle.

(8-2) Recommended Power Off Register Setting

Table 16

ITEM	Register Address	Register Data list	REMARK
SET_ DISPLAY_ OFF	**28H**	**----**	
Set ENT_ SLEEP_ MODE	**10H**	**---**	
Delay 100 ms			
Power Off	**VDD3(1.8V),VDD(2.8V) ON (anytime VDD3O≦VCI)**		

9. Initial Sequence

During power on, 'RESX' must be applied for a minimum of 10us after both VDD and VDD3 have been applied. 'RESX' can be undefined during power-on but must be applied subsequently to ensure correct LCD controller operation. VDD3 and VDD can be applied in any order.

During power-off, if the LCD controller is in 'Sleep Out' mode, VDD and VDD3 must be powered down a minimum of 120ms after RESX has been released. If the LCD controller is in 'Sleep In' mode, VDD3 and VDD can be powered down a minimum of 0ms after 'RESX' has been released. VDD3 and VDD can be powered down in any order.

'CSX' can be applied at any time. 'RESX' has priority over 'CSX'.

(9-1) Case 1 - RESX line is held high or unstable by host at power-on

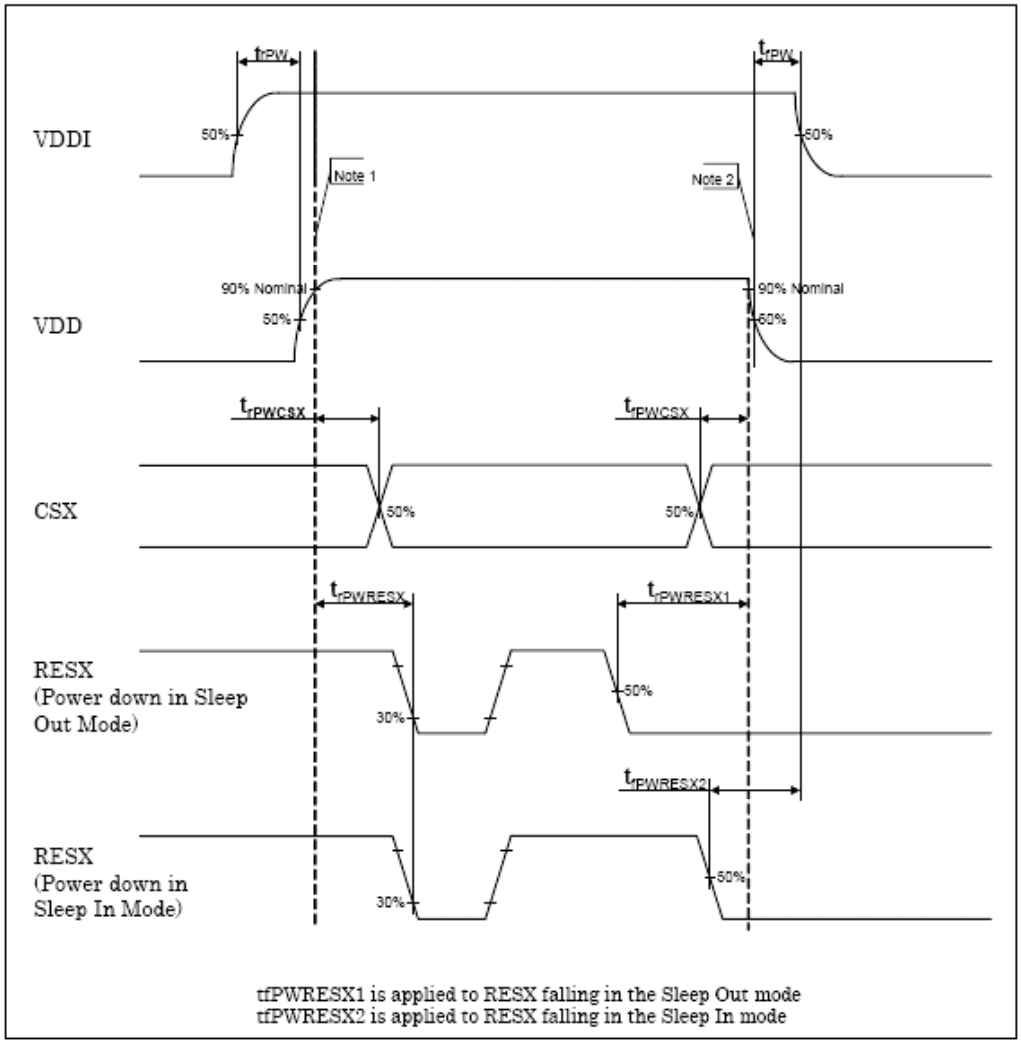


Fig.18

Note 1. Time when the latter signal rises up to 90% of its typical value, e.g. when VDD comes later. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Note 2. Time when the former signal falls down to 90% of its typical value, e.g. when VDD falls earlier. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Table 17

Parameter	Value
trPW	+/- no limit
tfPW	+/- no limit
trPWCSX	+/- no limit
tfPWCSX	+/- no limit
trPWRESX	+ no limit
tfPWRESX1	min 120mS
tfPWRESX2	+ no limit

(9-2) Case 2 - RESX line is held low by host at power-on

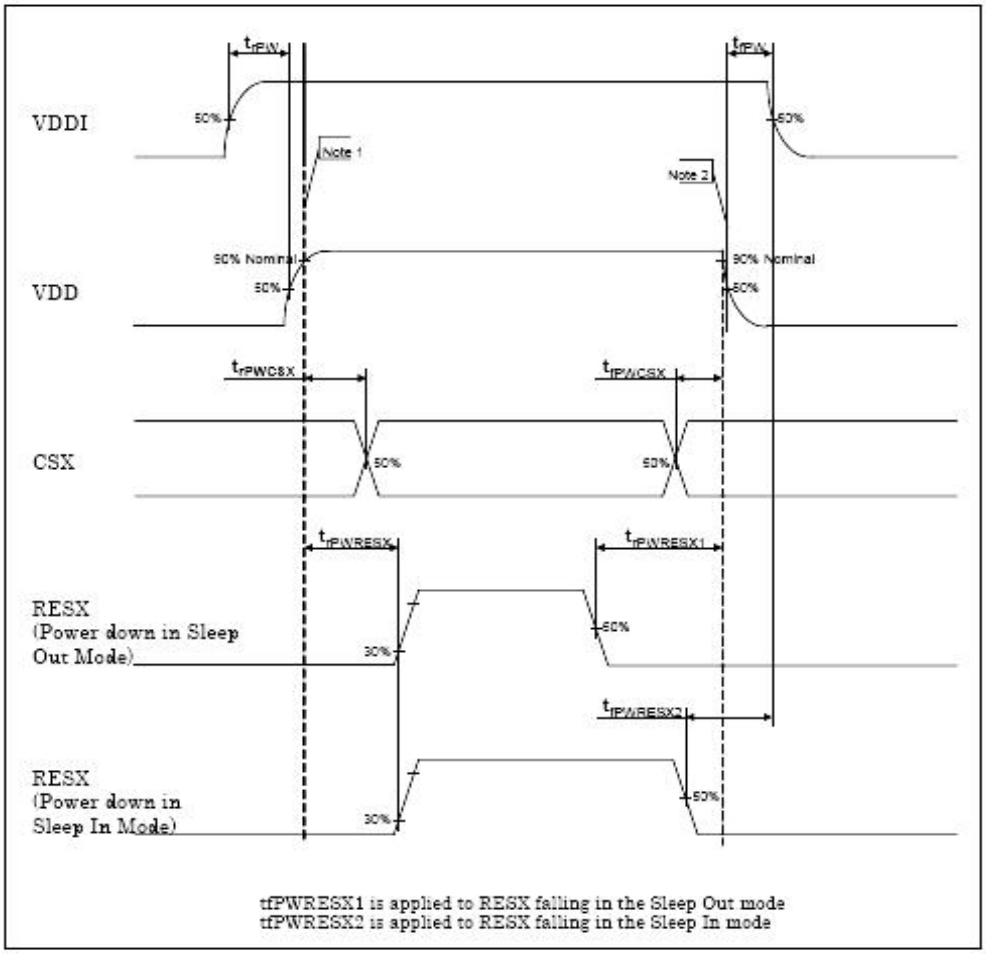


Fig.15

Note 1. Time when the latter signal rises up to 90% of its typical value, e.g. when VDD comes later. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Note 2. Time when the former signal falls down to 90% of its typical value, e.g. when VDD falls earlier.

This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Table 17

Parameter	Value
trPW	+/- no limit
tfPW	+/- no limit
trPWCSX	+/- no limit
tfPWCSX	+/- no limit
trPWRESX	min 10 us
tfPWRESX1	min 120mS
tfPWRESX2	min 0mS

Notes:

There will be no damage to the display module if the above power sequences are not met.

There will be no abnormal visible effects on the display panel during the sequence.

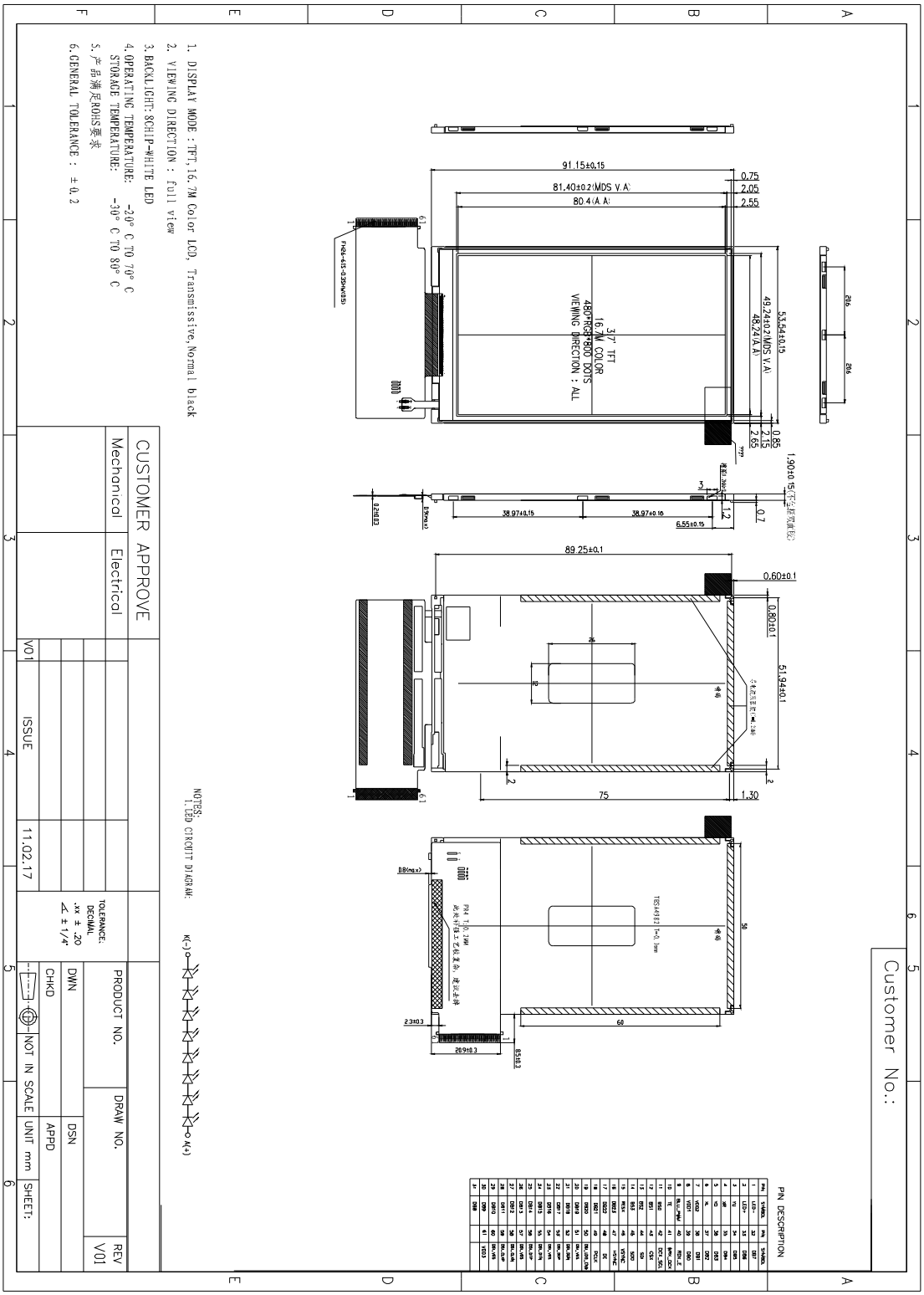
There will be no abnormal visible effects on the display between the end of power on sequence and before entering Sleep Out mode. Also between entering Sleep In mode and power off sequence.

There are no limits for RESX timings during power on sequence. (e.g. from the undefined level to high or low, when the first RESX low pulse after VDD and VDD3 are powered-on, etc.)

(9-3) Uncontrolled power-off

Uncontrolled power-off (e.g. the battery is removed without following the proper power-off sequence), will not damage the LCD module or cause the LCD module to inflict any damage on the host.

There will not be any abnormal visible effects left on the display after a period of 5 seconds following an uncontrolled power-off. The display will remain blank until the power on sequence is initiated.


1. DISPLAY MODE : TFT, 16.7M Color LCD, Transmissive, Normal black
2. VIEWING DIRECTION : full view
3. BACKLIGHT: SCHIP-WHITE LED
4. OPERATING TEMPERATURE: -20° C TO 70° C
STORAGE TEMPERATURE: -30° C TO 80° C
5. 产品满足ROHS要求
6. GENERAL TOLERANCE : ± 0.2
3.7" TFT
16.7M COLOR
480RGB*800 DOTS
VIEWING DIRECTION : ALL
91.15±0.15
81.40±0.2(MDS V.A)
80.4(A.A)
53.54±0.15
49.24±0.2(MDS V.A)
48.24(A.A)
89.25±0.1
51.94±0.1
0.60±0.1
0.80±0.1
75
1.30
60
50
CUSTOMER APPROVE
Mechanical
Electrical
V01
ISSUE
11.02.17
PRODUCT NO.
DRAW NO.
REV
V01
DWN
DSN
CHKD
APPD
NOT IN SCALE
UNIT mm
SHEET:
TOLERANCE:
DECIMAL
.XX ± .20
∠ ± 1/4°
NOTES:
1. LED CIRCUIT DIAGRAM:
K(-)
A(+)
PIN DESCRIPTION
Customer No.: