ALL SHORE INDUSTRIES

Specification

For

LCD Module

ASI-T-400NA3MN/S

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2012.1.11

RECORDS OF REVISION

REV	DATE	CHANGE DETAIL	ORIGINATOR	REMARKS
1	2012.1.11	FIRST issue	*luojiaoping*	

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• Description

This is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit ,back-light unit. The resolution of a 3.97" TFT-LCD contains 480(RGB) x 800 pixels, and can display up to 16.7M colors.

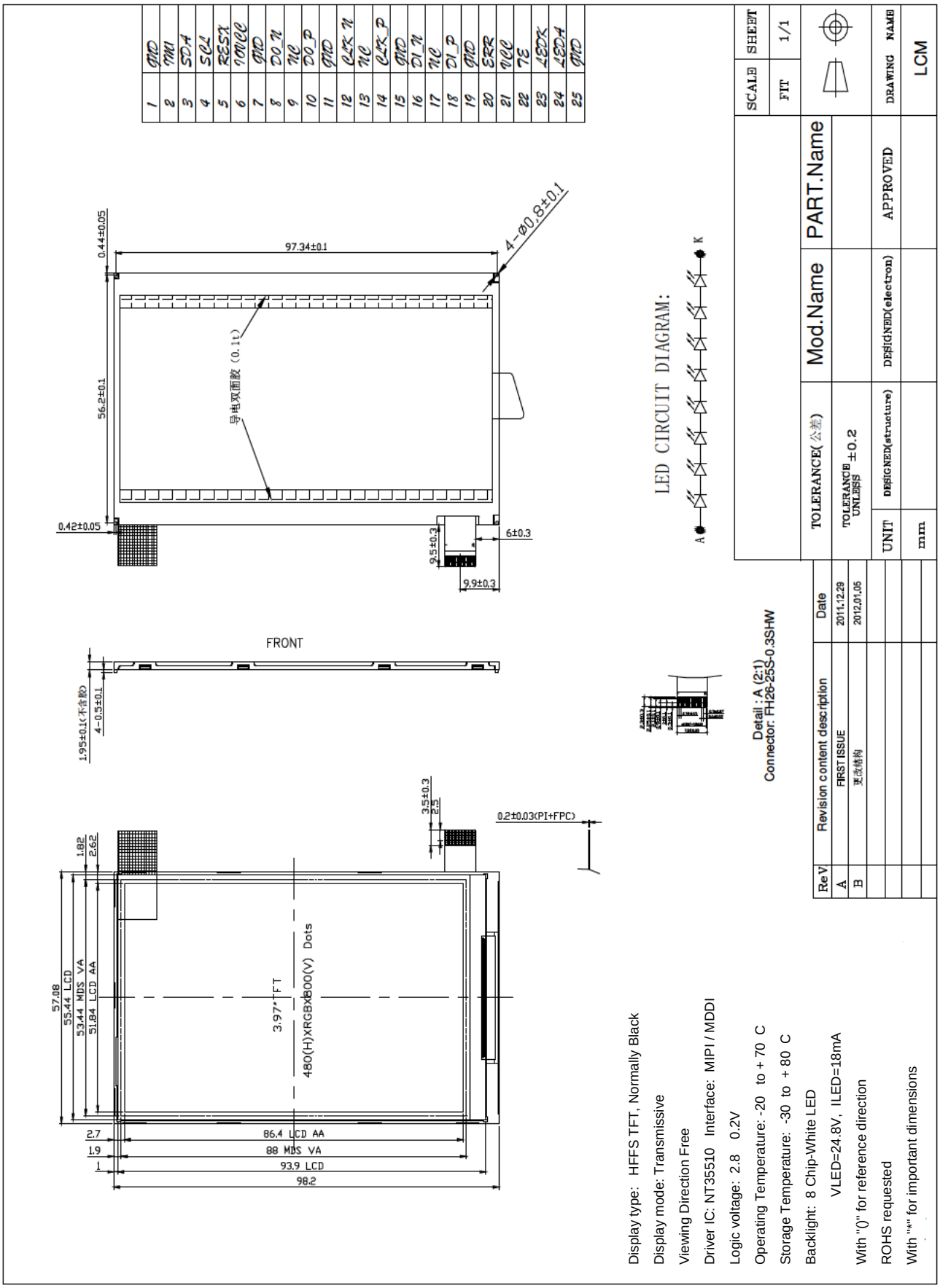
• Features

- Display Mode**:** HFFS TFT, Transmissive/ Normally Black
- Active screen size: 3.97″ Diagonal TFT.
- Display Colors of TFT LCD : 16.7M Colors
- Number of Dots : 480(RGB)X800
- Pixel Pitch (mm): 0.108 (H) x 0.108(V)
- Viewing Direction: Free
- Input Voltage : 2.5V~ 3.3V
- Control IC: NT35510
- Interface Type : MIPI/MDDI
- Operating Temperature: -20°C - 70°C
- Storage Temperature:-30°C - 80°C
- Backlight Color : White

• Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	57.08	-	mm	±0.2
	Vertical(V)	--	98.2	-	mm	±0.2
	Depth(D)	-	1.95	--	mm	±0.1
Weight		--	---	--	g	

1. OUTLINE DIMENSION



Display type: HFFS TFT, Normally Black
Display mode: Transmissive
Viewing Direction Free
Driver IC: NT35510 Interface: MIPI / MDDI
Logic voltage: 2.8 0.2V
Operating Temperature: -20 to + 70 C
Storage Temperature: -30 to + 80 C
Backlight: 8 Chip-White LED
VLED=24.8V, ILED=18mA
With "()" for reference direction
ROHS requested
With "*" for important dimensions

2. INPUT TERMINAL PIN ASSIGNMEN

Pin NO.	Symbol	Level	Function
1	GND	L	Power Ground
2	IM1	H/L	IM1=0：MIPI DSI， IM1=1：MDDI
3	SDA	H/L	IIC_SDA for MDDI
4	SCL	H/L	IIC_SCL for MDDI
5	RESX	H/L	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
6	IOVCC	H	A supply voltage to the digital circuit. (1.8V/2.8V)
7	GND	L	Power Ground
8	D0_N	H/L	This pin is DSI D0- differential data signals if MIPI interface is used. This pin is MDDI_DATA0_M differential strobe signals if MDDI interface is used
9	NC	/	No Connect
10	D0_P		This pin is DSI D0+ differential data signals if MIPI interface is used. This pin is MDDI_DATA0_P differential strobe signals if MDDI interface is used.
11	GND	L	Power Ground
12	CLK_N	H/L	This pin is DSI CLK- differential clock signals if MIPI interface is used. This pin is MDDI_STB_M differential strobe signals if MDDI interface is used.
13	NC	/	No Connect
14	CLK_P	H/L	This pin is DSI CLK+ differential clock signals if MIPI interface is used. This pin is MDDI_STB_P differential strobe signals if MDDI interface is used.

15	GND	L	Power Ground
16	D1_N	H/L	This pin is DSI D1- differential data signals if MIPI interface is used. This pin is MDDI_DATA1_M differential strobe signals if MDDI interface is used.
17	NC	/	No Connect
18	D1_P	H/L	This pin is DSI-D1+ differential data signals if MIPI interface is used. This pin is MDDI_DATA1_P differential strobe signals if MDDI interface is used.
19	GND	L	Power Ground
20	ERR	H/L	CRC and ECC error output pin for MIPI interface. This pin is output low when it is notactivated. When this pin is activated, it output high if CRC/ECC error found.
21	VCC	H	A supply voltage to the analog circuit. (2.8V type)
22	TE	H/L	Tearing effect output pin to synchronize MCU to frame writing, activated by S/Wcommand. When this pin is not activated, this pin is output low. If not used, please open this pin.
23	LEDK	L	Backlight Cathode
24	LEDA	H	Backlight Anode
25	GND	L	Power Ground

3. LCD OPTICAL CHARACRERISTICS

3.1 Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold Voltage		Vsat					V	Fig.1
		Vth					V	
Viewing Angle	Horiz-ontal	Θ3	CR>10		85		Deg.	Note 1
		Θ9			85		Deg.	
	Vertical	Θ12			85		Deg.	
		Θ6			85		Deg.	
Contrast Ratio		CR	Θ= 0°	700	900			Note 2
Transmittance		T(%)	Θ= 0°		5.2%			Note 3 Base on C light With APF
Reprod-uction of color	Red	Rx	Θ= 0°	0.620	0.640	0.660		Note 4 *Color Filter Glass (with ITO) Based on C light
		Ry		0.315	0.335	0.355		
	Green	Gx		0.295	0.325	0.345		
		Gy		0.576	0.606	0.626		
	Blue	Bx		0.128	0.148	0.168		
		By		0.025	0.045	0.065		
White		Wx	Θ= 0°	0.268	0.288	0.308		
		Wy		0.299	0.319	0.339		
Response Time		Tr+Tf	Ta= 25° C Θ= 0°		35		ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 2) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value with Polarizer.
4. The color chromaticity coordinates specified in Table1 shall be calculated from The spectral data measured with all pixels first in red, green, blue and white.
   Measurements shall be made at the center of the C/F.
   Measurement condition is C - light source & Halogen Lamp
5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF.
   The times needed for the luminance to change from 10% to 90% is Tf, and 90% to 10% is Tr.

Figure 1. The definition of Vth & Vsat

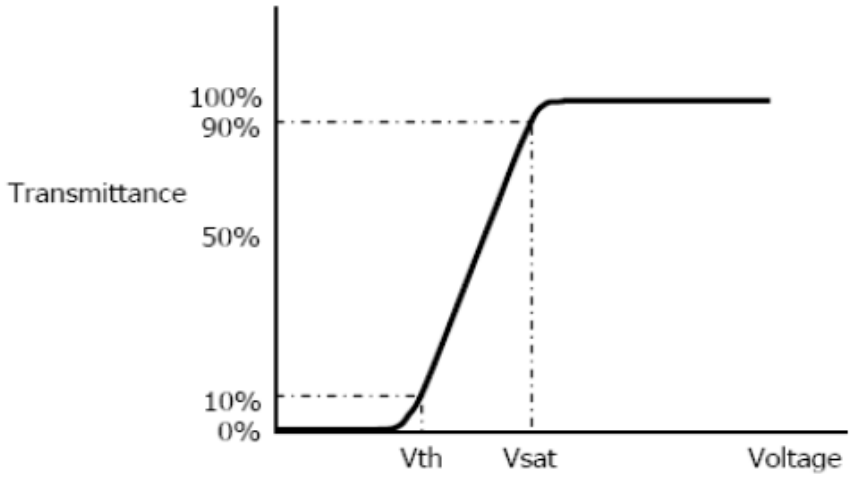


Figure 2. Measurement Set Up

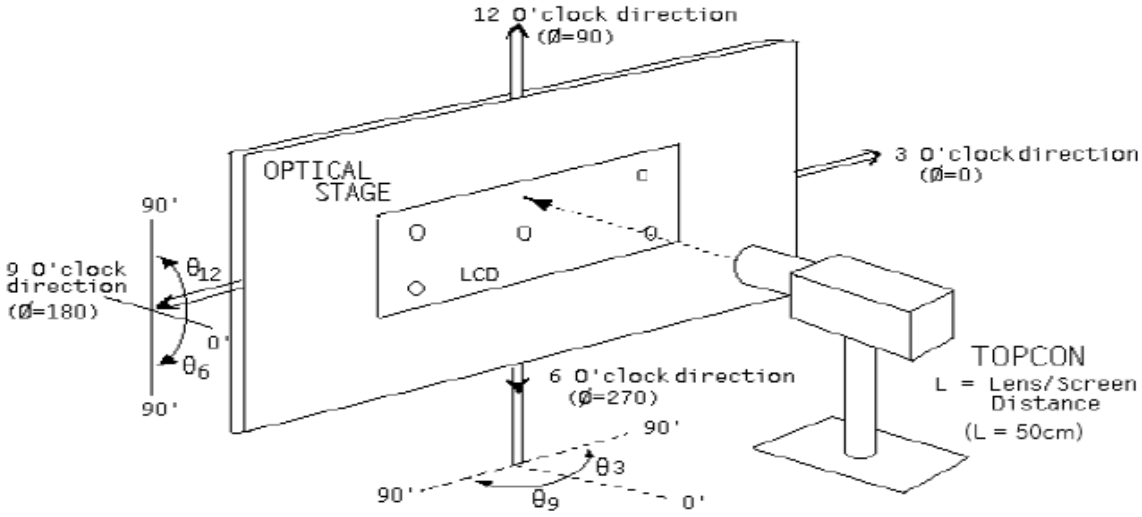
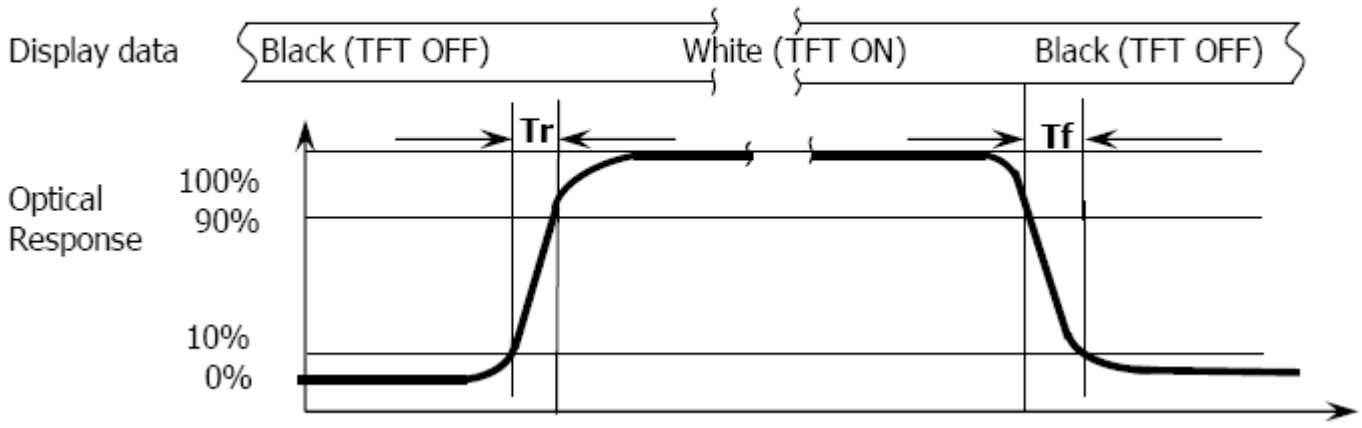


Figure 3. Response Time Testing



4. ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Rating (VSS=0V)

No	Item	Symbol	Min.	Max.	Unit
1	**Supply Voltage For Analog**	VCI	-0.3	5.5	V
2	**Supply Voltage For Logic**	IOVDD	-0.3	5.5	V
3	**Input Voltage**	V_{In}	GND-0.3	VCI+0.3	V

4.2 DC Characteristics

No	Item	Symbol	Min.	Typ.	Max.	Unit	Notes
1	Supply Voltage for Analog	VCI –G_{ND}	2.3	2.8	4.8	V	*
2	Supply Voltage for Digital	IOVDD-Gnd	1.65	1.8/2.8	3.3	V	
2	Supply Current for LCM	I_{DD}	-	35	-	mA	
4	TFT Gate ON Voltage	VGH *1)	13	15	17	V	
5	TFT Gate OFF Voltage	VGL *2)	-13	-10	-9	V	
7	Input High Voltage	V_{IH}	0.7xVCI	-	VCI	V	
8	Input Low Voltage	V_{IL}	0	-	0.2xVCI	V	
9	Output High Voltage	V_{OH}	0.8xVCI	-	VCI	V	
10	Output Low Voltage	V_{OL}	0	-	0.2xVCI	V	

Notes:

*1) VGH is TFT Gate Operating Voltage.

*2) VGL is TFT Gate Operating Voltage.

4.3 LED Backlight Characteristics

The back−light system is edge−lighting type with 8chips White LED in Series.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	18	--	mA	--
Forward Voltage	V_F	--	24.8		V	-
Luminance	L_V	280	330	--	cd/m2	I_F=18mA
Uniformity	A_{Vg}	---	--	--	%	--

4.4 AC Timing Diagram

MIPI DSI Timing Characteristics

4.4.1 HIGH SPEED MODE

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	-	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

Note) Dn = D0 and D1.

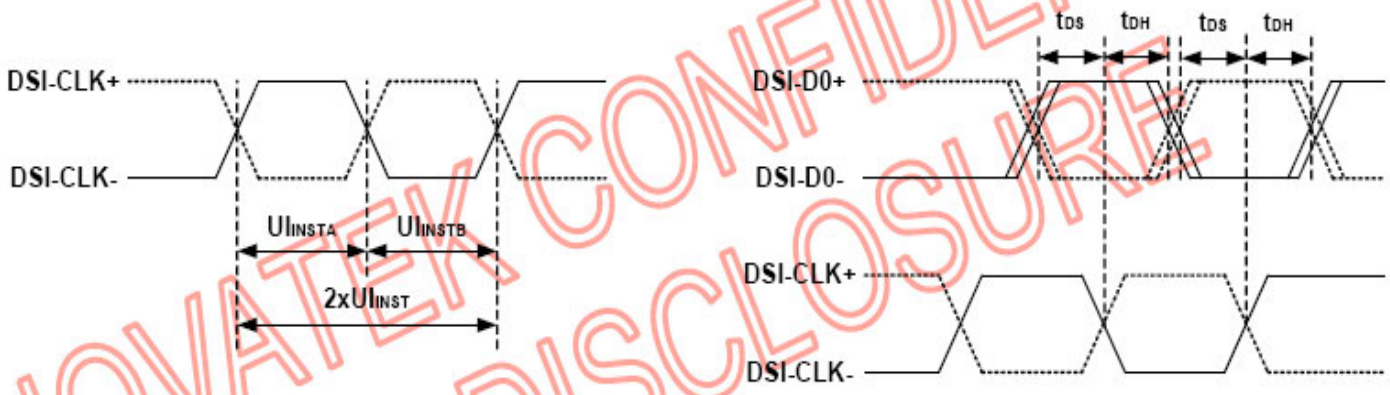


Fig. 7.6.4 DSI clock channel timing

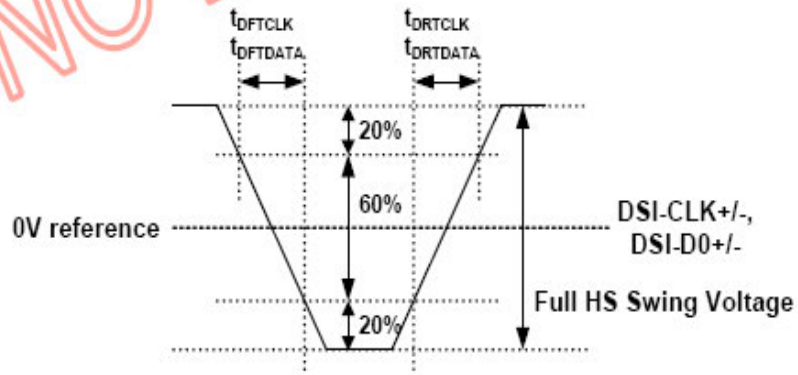


Fig. 7.6.5 Rising and fall time on clock and data channel

4.4.2 LOW POWER MODE

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output

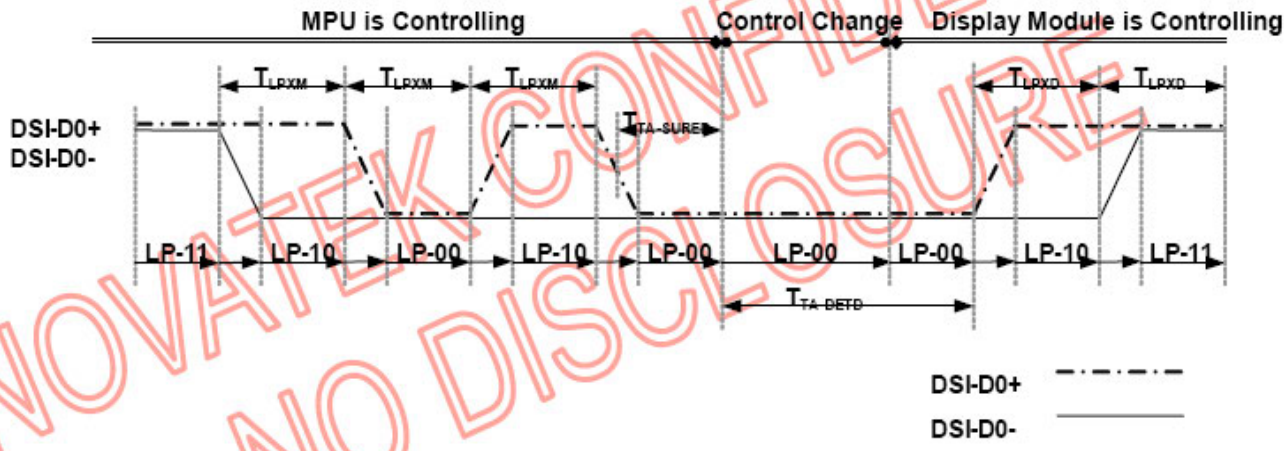


Fig. 7.6.6 Bus Turnaround (BAT) from MPU to display module Timing

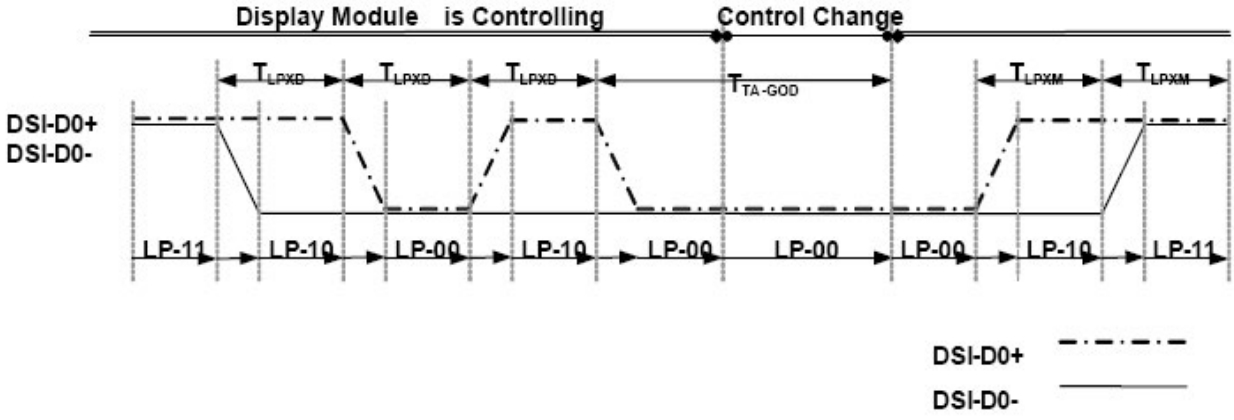


Fig. 7.6.7 Bus Turnaround (BAT) from display module to MPU Timing

4.4.3 MDDI Timing Characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
MDDI_STB_P/M MDDI_DATA_P/M	1/Tbit	Data transfer rate	-	384	450	Mbps	
MDDI_STB_P/M MDDI_DATA_P/M	|Tskew-pair|	Differential transfer input skew	-	-	0.05	ns	
MDDI_STB_P/M MDDI_DATA_P/M	|Tskew-data|	Data/Strobe input skew	-	-	0.3	ns	

Note) MDDI_DATA_P/M = MDDI_DATA0_P/M and MDDI_DATA1_P/M.

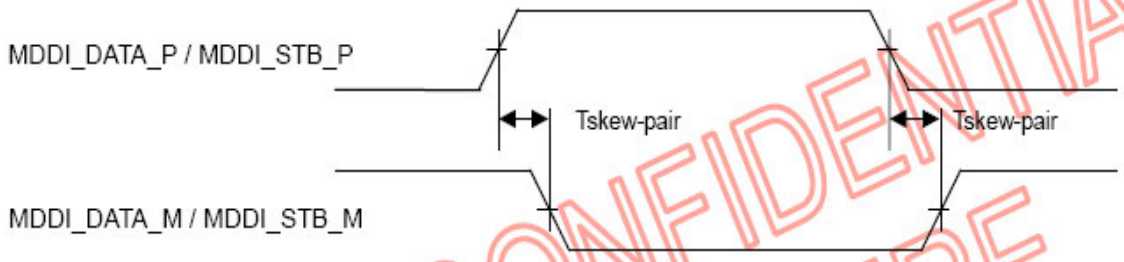


Fig. 7.6.10 Skew between MDDI positive and negative signal pair

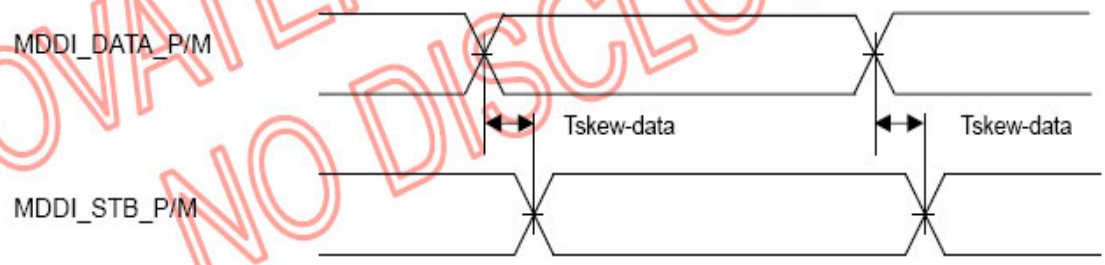


Fig. 7.6.11 Skew between MDDI_DATA_P/M and MDDI_STB_P/M

4.4.4 Reset Input Timing

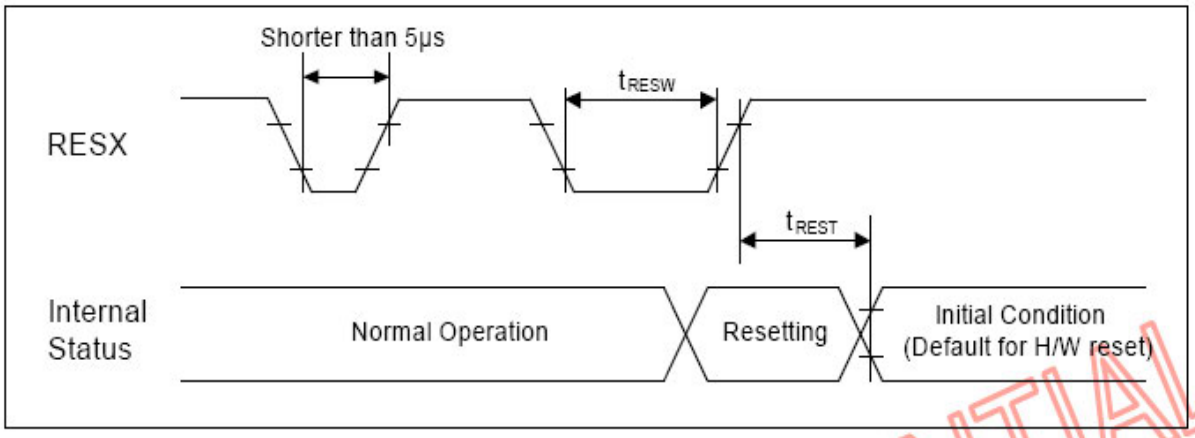


Fig. 7.6.12 Reset input timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

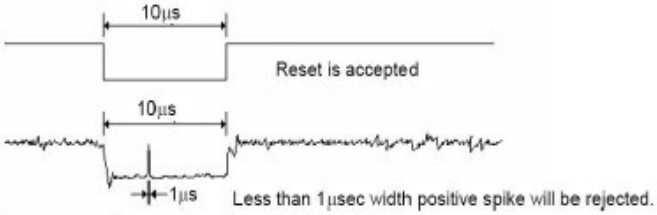
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

6 . OPERATING PRINCIPLE & METHODS

Please refer to NT35510 datasheet for more details.

7. CAUTIONS AND HANDLING PRECAURIONS

7.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage,

this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch

the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl

chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or

mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly

with soap.

(8) Protect the module from static, it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection

and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 5.1 Power On Sequence &5.2 Power Off Sequence

7.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

8. Reliability

Test Item	Test Condition
High Temperature Operation	70℃ for 96 hours
Low Temperature Operation	-20℃ for 96 hours
High Temperature Storage	80℃ for 96 hours
Low Temperature Storage	-30℃ for 96 hours
High Temperature Operation Humidity Operation	60℃, 90%RH for 96 hours
Thermal Shock	-30℃(30min) ~+25℃(5min)~ +80℃(30min) for 100 cycles
Vibration Test (No Operation)	Frequency: 10~55Hz Amplitude:1.0mmSweep Time: 11min Test Period: 6 Cycles for each direction of X, Y, Z

10. Packing

TBD