

ASM1142 Data Sheet

PCI Express to 2 ports USB3.1
xHCI Host Controller

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	September 16, 2013	Initial Release
0.2	September 26, 2013	Correct the typo of pin19, 36 and 37
0.3	June 23, 2014	Update the feature description Remove the feature of 48MHz clock input
0.4	October 15, 2014	Update the strapping table Add the timing spec Update the core power spec and ESD capability
0.5	Nov. 18, 2014	Add the spec of Tcase and Power consumption

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1. General Description

ASM1142 is an ASMedia first Universal Serial Bus 3.1 host controller, compliant with Intel eXtensible Hot Controller Interface specification revision 1.1, bridging PCI Express interface to two ports of USB3.1, up to 10Gbps high speed bandwidth, backward compatible with legacy USB function and devices. It can configure PCI Express as Gen2 x2 or Gen3 x1, compliant with USB Attach SCSI Protocol revision 1.0, supporting the function of debugport.

ASM1142 integrates ASMedia self-designed PCI Express/USB3.1 PHY, and it also integrates two internal regulators to supply normal core power and suspend core power, supporting the driver on Windows 7, Windows 8.0, Windows 8.1 and various Linux kernels. The application of ASM1142 includes Motherboard, Desktop PC, Notebooks, Workstations, Servers, Add-in cards, PCI Express based embedded platform.

2. Features

General Feature

- ◇ Bridge PCI Express to USB3.1
- ◇ Upload firmware through BIOS or external SPI ROM
- ◇ External 20MHz differential crystal
- ◇ Overclock capability on PCI Express bus under asynchronous mode
- ◇ Integrate Spread Spectrum Controller for PCI Express and USB3.1 interface
- ◇ Integrate two regulators for normal core power supply and suspend core power supply
- ◇ Support driver on Windows7, Windows8, and Windows 8.1
- ◇ Support various Linux kernels

PCI Express Feature

- ◇ Support PCI Express Gen2 x2 or Gen3 x1
- ◇ Up to 10 Gbps bandwidth performance with low latency
- ◇ Support PCI Express Link power management
- ◇ Compliant with PCI Express Base 3.0 Specification
- ◇ Compliant with PCI Express Card Electromechanical 2.0 specification
- ◇ Compliant with PCI Express Mini Card Electromechanical 1.2 specification
- ◇ Compliant with ExpressCard Standard Revision 2.0
- ◇ Compliant with PCI Bus Power Management Interface Specification Revision 1.2
- ◇ Compliant with PCI Local Bus Specification Revision 3.0
- ◇ Support overclocking capability on PCI Express Interface

USB Feature

- ◇ Support two ports of USB3.1
- ◇ Compliant with Universal Serial Bus 3.1 Specification Revision 1.0
- ◇ Compliant with Universal Serial Bus Specification Revision 2.0
- ◇ Compliant with eXtensible Host Controller Interface specification Revision 1.1
- ◇ Compliant with USB Attached SCSI Protocol Revision 1.0
- ◇ Support USB3.1 and USB2.0 Link Power Management
- ◇ Support Control, Bulk, Stream, Interrupt, Isochronous transfer type
- ◇ Support independent port power control
- ◇ Support over current detection
- ◇ Support Remote/Wakeup event
- ◇ Backward compatible with Legacy USB function and device
- ◇ Support the Debugport

Package Type

- ◇ Green Package 9x9 QFN64 (Pb-free) - RoHS Compliance

3. Functional Diagram

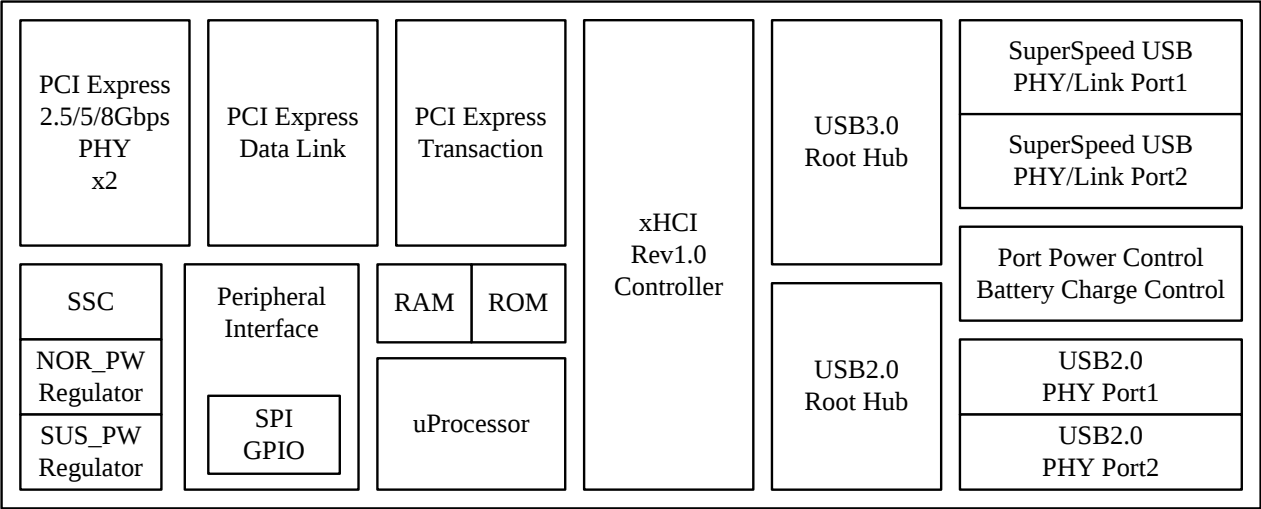


Figure 1: Functional Diagram of ASM1142

4. Pinout Diagrams

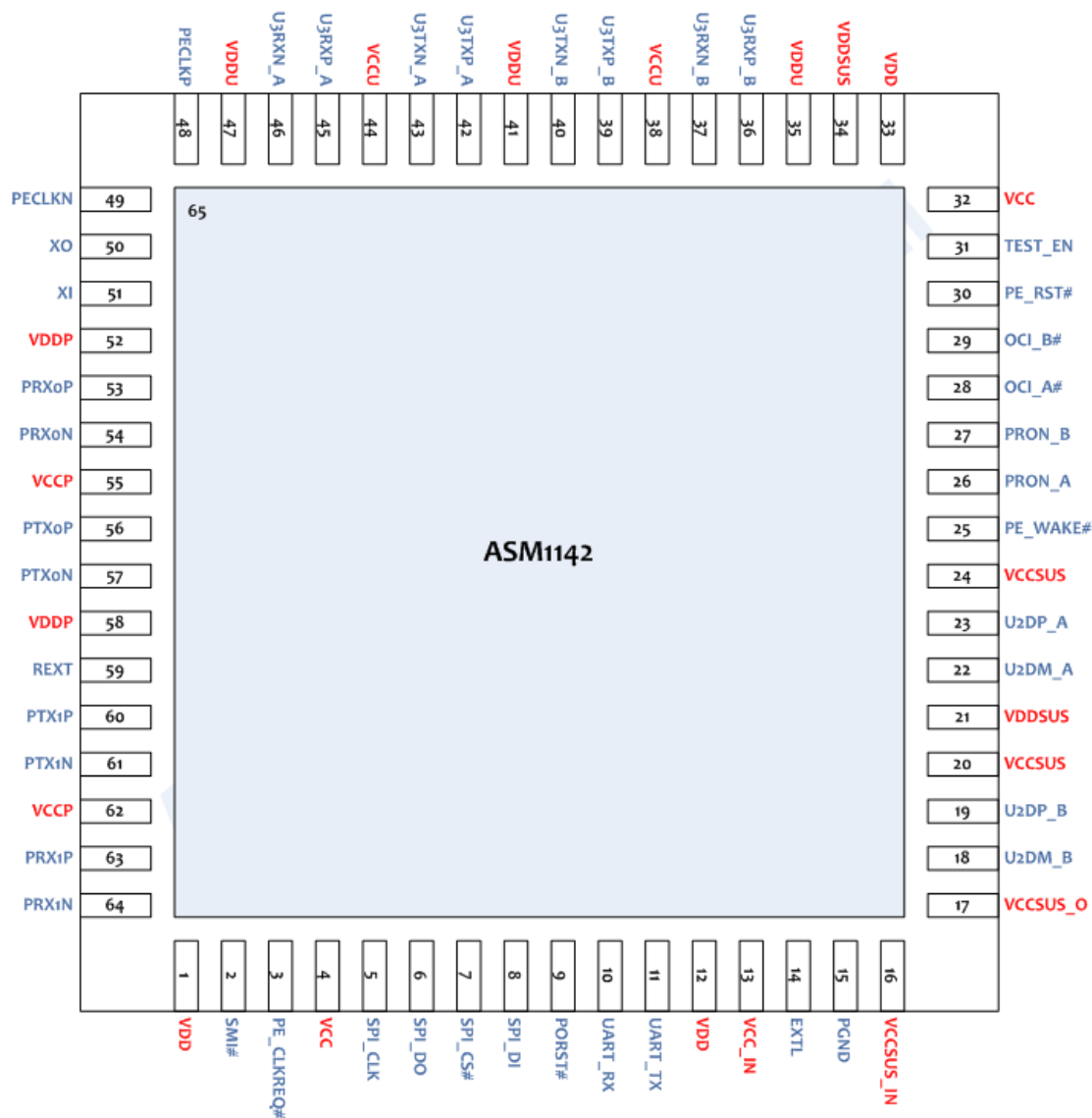


Figure 2: ASM1142 QFN64 pinout

5. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain

PCI Express Interface

QFN64	Name	PWR	TYPE	Descriptions
53	PRX0P	PCIE	DiI	PCI Express Differential Receive Signal +
54	PRX0N	PCIE	DiI	PCI Express Differential Receive Signal -
56	PTX0P	PCIE	DiO	PCI Express Differential Transmit Signal +
57	PTX0N	PCIE	DiO	PCI Express Differential Transmit Signal -
63	PRX1P	PCIE	DiI	PCI Express Differential Receive Signal +
64	PRX1N	PCIE	DiI	PCI Express Differential Receive Signal -
60	PTX1P	PCIE	DiO	PCI Express Differential Transmit Signal +
61	PTX1N	PCIE	DiO	PCI Express Differential Transmit Signal -
48	PE_CLKP	VCC	DiI	PCI Express Differential Clock Signal+
49	PE_CLKN	VCC	DiI	PCI Express Differential Clock Signal-
25	PE_WAKE#	VCC_SUS	O	PCI Express Remote/Wakeup Internal pull up resistor
30	PE_RST#	VCC_SUS	I	PCI Express Reset
3	PE_CLKREQ#	VCC	O	PCI Express Clock Request

USB Interface

QFN64	Name	PWR	TYPE	Descriptions
18	U2DM_B	VCC_SUS	DiB	USB2.0 Differential Signal- for Port B
19	U2DP_B	VCC_SUS	DiB	USB2.0 Differential Signal+ for Port B
22	U2DM_A	VCC_SUS	DiB	USB2.0 Differential Signal- for Port A
23	U2DP_A	VCC_SUS	DiB	USB2.0 Differential Signal+ for Port A
36	U3RXP_B	VCC_SUS	DiI	USB3.0 Differential Receive Signal + for Port B
37	U3RXN_B	VCC_SUS	DiI	USB3.0 Differential Receive Signal - for Port B
39	U3TXP_B	VCC_SUS	DiO	USB3.0 Differential Transmit Signal + for Port B
40	U3TXN_B	VCC_SUS	DiO	USB3.0 Differential Transmit Signal - for Port B
42	U3TXP_A	VCC_SUS	DiO	USB3.0 Differential Transmit Signal + for Port A
43	U3TXN_A	VCC_SUS	DiO	USB3.0 Differential Transmit Signal - for Port A
45	U3RXP_A	VCC_SUS	DiI	USB3.0 Differential Receive Signal + for Port A
46	U3RXN_A	VCC_SUS	DiI	USB3.0 Differential Receive Signal - for Port A
26	PRON_A	VCC_SUS	O	Port Power Control for Port A
27	PRON_B	VCC_SUS	O	Port Power Control for Port B
28	OCI_A#	VCC_SUS	I	Overcurrent Signal for Port A Internal pull up resistor
29	OCI_B#	VCC_SUS	I	Overcurrent Signal for Port B Internal pull up resistor

SPI Interface

QFN64	Name	PWR	TYPE	Descriptions
5	SPI_CLK	VCC	O	Clock of Serial Peripheral Interface Internal pull up resistor
6	SPI_DO	VCC	O	Data Output of Serial Peripheral Interface Internal pull up resistor
7	SPI_CS#	VCC	O	Chip Select of Serial Peripheral Interface Internal pull up resistor
8	SPI_DI	VCC	I	Data Input of Serial Peripheral Interface Internal pull up resistor

System Interface

QFN64	Name		TYPE	Descriptions
10	UART_RX	VCC	I	UART Rx Signal Internal pull up resistor
11	UART_TX	VCC	O	UART Tx Signal Internal pull up resistor
9	PORST#	VCC	I	Power On Rest
59	REXT	VCC	I	External Reference 12.1Kohm+/-1% Resistor to GND
31	TEST_EN	VCC_SUS	I	Test Mode Enable Internal pull down resistor
2	SMI#	VCC	O	System management Interrupt Internal pull up resistor IO type is configurable as open-drain or push-pull mode by firmware
14	EXTL	VCC	O	Connect to external Inductor
50	XO	VCC	B	20MHz Crystal Output or 48MHz clock input
51	XI	VCC	I	20MHz Crystal Input

Regulator

QFN64	Name	TYPE	Descriptions
15	PGND	G	Analog Ground for switching regulator
13	VCC_IN	P	Switching Regulator VCC Input
16	VCCSUS_IN	P	Linear Regulator VCCSUS Input
17	VCCSUS_O	P	Linear Regulator VCCSUS output for VDDSUS

Power and Ground

QFN64	Name	TYPE	Descriptions
4, 32	VCC	P	IO Power
1, 12, 33	VDD	P	Core Power
38, 44	VCCU	P	IO Power for USB
35, 41, 47	VDDU	P	Core Power for USB
55, 62	VCCP	P	IO Power for PCI Express
52, 58	VDDP	P	Core Analog Power for PCI Express
20, 24	VCCSUS	P	Suspend IO Power
21, 34	VDDSUS	P	Suspend Core Power
65	GND	G	Common Ground

Strapping Table

	Function	Description
SPI_CLK	D3cold enable	1: D3cold (Default) 0: D3Hot
UART[RX:TX]	Clock Select	11: Asynchronous mode with External 20MHz Crystal (Default) Rest : Reserved for Test mode

6 Register Table

The ASM1142 integrates an eXtended Host Controller (xHCI) handling USB3.1 and USB2.0 device connected to root hub port on ASM1142. The following section shows PCI configuration space and xHCI Host Controller register information.

6.1 Register Attribute

Register Attribute	Definition
RO	Read-only register: Register bits are read-only and cannot be altered by software.
RW	Read-Write register: Register bits are read-write and may be either set or cleared by software to the desired state.
HwInit	Hardware Initialized: Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. Bits are read-only after initialization and can only be reset (for write-once by firmware) with Fundamental Reset.
RW1C	Read-only status, Write-1-to-clear status register: Register bits indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1C bits has no effect.
ROS	Sticky – Read-only register: Registers are read-only and cannot be altered by software. Registers are not initialized or modified by hot reset.
RWS	Sticky – Read-Write register: Registers are read-write and may be either set or cleared by software to the desired state. Bits are not initialized or modified by hot reset.
RW1CS	Sticky – Read-only status, Write-1-to-clear status register: Registers indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1CS bits has no effect. Bits are not initialized or modified by hot reset.
RWO	Read-Write Once: Register can only be written once
Rsvd	Reserved: Reserved for future RW

6.2 PCI Configuration Space Register

6.2.1 Type 0 Configuration Header Registers

Type 0 Configuration Header Register						
31:24	23:16	15:8	7:0	Byte Offset		
Device ID		Vendor ID		00h		
Status		Command		04h		
Class Code			Revision ID	08h		
BIST	Header Type	Latency Timer	Cache Line size	0Ch		
Base Address 0				10h		
Base Address 1				14h		
Reserved				18h-28h		
Subsystem ID		System Vender ID		2Ch		
				30h		
				Capabilities PTR	34h	
					38h	
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch		
Reserved for Device-Specific and PCI Capability Registers				40h-5Fh		
				FLADJ	SBRN	60h
						64h-FCh

Register Name: Vendor ID Register

Address: 00h

Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Vendor ID (VID)	16'h 1B21

Register Name: Device ID Register

Address: 02h

Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Device ID (DID)	16'h 1242

Register Name: Command Register

Address: 04h

Size: 16 bits

Bit	Attrib	Description	Default
0	RO	I/O Space Enable	1'h 0
1	RW	Memory Space Enable	1'h 0
2	RW	Bus Master Enable	1'h 0
3	RO	Special Cycle Enable	1'h 0
4	RO	Memory Write and Invalidate	1'h 0
5	RO	VGA Palette Snoop	1'h 0
6	RW	Parity Error Response	1'h 0
8	Rw	SERR# Enable	1'h 0
9	RO	Fast Back-to-Back Transaction Enable	1'h 0
10	RW	Interrupt Disable	1'h 0
15:11		Reserved	

Register Name: Status Register

Address: 06h

Size: 16 bits

Bit	Attrib	Description	Default
2:0		Reserved	
3	RO	Interrupt Status	1'h 0
4	RO	Capabilities List	1'h 1
6		Reserved	
8	RW1C	Master Data Parity Error	1'h 0
11	RW1C	Signaled Target-Abort	1'h 0
12	RW1C	Received Target-Abort	1'h 0
13	RW1C	Received Master-Abort	1'h 0
14	RW1C	Signaled System Error	1'h 0
15	RW1C	Detected Parity Error	1'h 0

Register Name: Revision ID Register

Address: 08h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Revision ID	8'h 00

Register Name: Class Code Register

Address: 09h

Size: 24 bits

Bit	Attrib	Description	Default
7:0	RO	Programming Interface (PI)	8'h 30
15:8	RO	Sub-Class Code (SSC)	8'h 03
23:16	RO	Base Class Code (BASEC)	16'h 000C

Register Name: Cache Line Size Register

Address: 0Ch

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Cache Line Size	8'h 00

Register Name: Header Type Register

Address: 0Eh

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Header Type	8'h 00

Register Name: BIST Register

Address: 0Fh

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	BIST	8'h 00

Register Name: Base Address 0 Register

Address: 10h

Size: 32 bits

Bit	Attrib	Description	Default
0	RO	Memory Space Indicator	1'h 0
2:3	RO	Type	2'h 2
3	RO	Prefetchable	1'h 0
12:4	RO	Base Address (LSB)	9'h 00
31:13	RW	Base Address (MSB)	18'h 0 0000

Register Name: Base Address 1 Register

Address: 14h

Size: 32 bits

Bit	Attrib	Description	Default
31:0	RO	Base Address 1	32'h 0000 0000

Register Name: Subsystem Vender ID

Address: 2Ch

Size: 32 bits

Bit	Attrib	Description	Default
15:0	HWinit	System Vender ID	16'h 1B21

Register Name: Subsystem ID

Address: 2Eh

Size: 32 bits

Bit	Attrib	Description	Default
15:0	HWinit	Subsystem ID	16'h 1242

Register Name: Capabilities Pointer Register

Address: 34h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capabilities Pointer	8'h 50

Register Name: Interrupt Line Register

Address: 3Ch

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RW	Interrupt Line	8'h 00

Register Name: Interrupt Pin Register

Address: 3Dh

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Interrupt Pin	8'h 01

Register Name: Serial Bus Release Number Register (SBRN)

Address: 60h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Serial Bus Release Number (SBRN)	8'h 30

Register Name: Frame Length Adjustment Register

Address: 61h

Size: 8 bits

Bit	Attrib	Description	Default
5:0	RWS	Frame Length Adjustment (FLADJ)	6'h 20
7:6		Reserved	

6.2.2 Message Signal Interrupts (MSI & MSI-X) Capability Registers

MSI & MSI-X Capability Register				
31:24	23:16	15:8	7:0	Byte Offset
MSI Message Control		Next Pointer	Capabilities ID	050h
Message Address				054h
Message Upper Address				058h
Reserved		Message Data		05Ch

MSI-X Message Control		Next Pointer	Capabilities ID	068h
Table Offset				06Ch

PBA Offset

070h

Register Name: MSI Capability ID

Address: 50h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	MSI Capability ID	8'h 05

Register Name: MSI Next Capability Pointer Register

Address: 51h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	MSI Next Capability Pointer	8'h 68

Register Name: MSI Message Control Register

Address: 52h

Size: 16 bits

Bit	Attrib	Description	Default
0	RW	MSI Enable	1'b 0
3:1	RO	Multiple Message Capable	3'b 011
6:4	RW	Multiple Message Enable	3'b 000
7	RO	64-bit Address Capable	1'b 0
8	RO	Per-vector masking capable	1'b 0
15:9		Reserved	

Register Name: MSI Message Address Register

Address: 54h

Size: 32 bits

Bit	Attrib	Description	Default
1:0		Reserved	
31:2	RW	MSI Message Address	30'h 0000 0000

Register Name: MSI Message Upper Address Register

Address: 58h

Size: 32 bits

Bit	Attrib	Description	Default
31:0	RW	MSI Message Upper Address	32'h 0000 0000

Register Name: MSI Message Data Register

Address: 5Ch

Size: 16 bits

Bit	Attrib	Description	Default
15:0	RW	MSI Message Data	16'h 0000

Register Name: MSI-X Capability ID

Address: 68h

Size: 8 bits

Bit	Attrib	Description	Default
-----	--------	-------------	---------

7:0	RO	MSI-X Capability ID	8'h 11
-----	----	---------------------	--------

Register Name: MSI-X Next Capability Pointer Register

Address: 69h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	MSI-X Next Capability Pointer	8'h 78

Register Name: MSI-X Message Control Register

Address: 6Ah

Size: 16 bits

Bit	Attrib	Description	Default
10:0	RO	Table Size	11'h 007
13:11		Reserved	
14	RW	Function Mask	1'b 0
15	RW	MSI-X Enable	1'b 0

Register Name: MSI-X Table Offset Register

Address: 6Ch

Size: 32 bits

Bit	Attrib	Description	Default
31:0	RO	Table Offset	32'h 2000

Register Name: MSI-X PBA Offset Register

Address: 70h

Size: 8 bits

Bit	Attrib	Description	Default
31:0	RO	MSI-X PBA Offset Register	32'h 2080

6.2.3 Power Management Capability Registers

Power Management Capability Register					
31:24	23:16	15:8	7:3	2:0	Byte Offset
PMC		Next Pointer	Capabilities ID		078h
Data	PMCSR BSE	PMCSR			07Ch

Register Name: Capabilities ID

Address: 78h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capability ID	8'h 01

Register Name: Next Capability Pointer Register (Next_Ptr)

Address: 79h

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Next Capability Pointer	8'h 80

Register Name: Power Management Capabilities Register (PMC)

Address: 7Ah

Size: 16 bits

Bit	Attrib	Description	Default
2:0	RO	Version	3'h 11
3	RO	PME Clock	1'h 0
4		Reserved	
5	RO	DSI	1'h 0
8:6	HWinit	Aux Current	3'h 0
9	RO	D1 Support	1'h 0
10	RO	D2 Support	1'h 0
15:11	HWinit	PME Support	5'b X1001

Register Name: Power Management Control/Status Register (PMCSR)

Address: 7Ch

Size: 16 bits

Bit	Attrib	Description	Default
1:0	RW	Power State	2'h 00
2		Reserved	
3	RO	No Soft Reset	1'b 0
7:4		Reserved	
8	RWS	PME Enable	1'b 0
12:9	RO	Data Select	1'b 0
14:13	RO	Data Scale	1'b 0
15	RW1CS	PME Status	1'b 0

6.3 Host Controller Capability Register

eXtensible Host Controller Capability Register				
31:24	23:16	15:8	7:0	Byte Offset
HCVERSION		Reserved	CAPLENGTH	00h
HCSPARAMS 1				04h
HCSPARAMs 2				08h
HCSPARAMS 3				0Ch
HCCPARAMS				10h
Doorbell Offset (DBOFF)				14h
Runtime Register Space Offset				18h
Reserved				1Ch

Register Name: Capability Register Length (CAPLENGTH)

Address: Base + (00h)

Size: 8 bits

Bit	Attrib	Description	Default
7:0	RO	Capability Register Length	8'h 20

Register Name: Host Controller Interface Version Number (HCVERSION)

Address: Base + (02h)

Size: 16 bits

Bit	Attrib	Description	Default
15:0	RO	Host Controller Interface Version Number	16'h 0096

Register Name: Structural Parameters 1 (HCSPARAM 1)

Address: Base + (04h)

Size: 32 bits

Bit	Attrib	Description	Default
7:0	RO	Number of Device Slots (MaxSlots)	8'h 20
18:8	RO	Number of Interrupts (MaxIntrs)	11'h 008
23:19		Reserved	
31:24	RO	Number of Ports (MaxPorts)	8'h 04

Register Name: Structural Parameters 2 (HCSPARAM 2)

Address: Base + (08h)

Size: 32 bits

Bit	Attrib	Description	Default
3:0	RO	Isochronous Scheduling Threshold (IST)	4'h 1
7:4	RO	Event Ring Segment Table Max (ERST Max)	4'h F
12:8	RO	IOC Interval	5'h 17
25:13		Reserved	
26	RO	Scratchpad Restore (SPR)	1'b 0
31:27	RO	Max Scratchpad Buffers (Max Scratchpad Bufs)	5'h 00

Register Name: Structural Parameters 3 (HCSPARAM 3)

Address: Base + (0Ch)

Size: 32 bits

Bit	Attrib	Description	Default														
7:0	RO	U1 Device Exit Latency <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>00h</td><td>Zero</td></tr><tr><td>01h</td><td>Less than 1us</td></tr><tr><td>02h</td><td>Less than 2us</td></tr><tr><td>---</td><td></td></tr><tr><td>0Ah</td><td>Less than 10us</td></tr><tr><td>0Bh-FFh</td><td>Reserved</td></tr></tbody></table>	Value	Description	00h	Zero	01h	Less than 1us	02h	Less than 2us	---		0Ah	Less than 10us	0Bh-FFh	Reserved	8'h 00
Value	Description																
00h	Zero																
01h	Less than 1us																
02h	Less than 2us																

0Ah	Less than 10us																
0Bh-FFh	Reserved																
15:8		Reserved															
31:16	RO	U2 Device Exit Latency <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0000h</td><td>Zero</td></tr><tr><td>0001h</td><td>Less than 1us</td></tr><tr><td>0002h</td><td>Less than 2us</td></tr><tr><td>---</td><td></td></tr><tr><td>07FFh</td><td>Less than 2047us</td></tr><tr><td>0800h-FFFFh</td><td>Reserved</td></tr></tbody></table>	Value	Description	0000h	Zero	0001h	Less than 1us	0002h	Less than 2us	---		07FFh	Less than 2047us	0800h-FFFFh	Reserved	16'h 0000
Value	Description																
0000h	Zero																
0001h	Less than 1us																
0002h	Less than 2us																

07FFh	Less than 2047us																
0800h-FFFFh	Reserved																

Register Name: Capability Parameters (HCCPARAMS)

Address: Base + (10h)

Size: 32 bits

Bit	Attrib	Description	Default
0	RO	64-bit Addressing Capability (AC64)	1'b 0
1	RO	BW Negotiation Capability (BNC)	1'b 0
2	RO	Context Size (CSZ)	1'b 0
3	RO	Port Power Control (PPC)	1'b 0
4	RO	Port Indicators (PIND)	1'b 0
5	RO	Light HC Reset Capability (LHRC)	1'b 0
6	RO	Latency Tolerance Messaging Capability (LTC)	1'b 0
7	RO	No Secondary SID Support (NSS)	1'b 1

8	RO	Force Stopped Event (FSE)	1'b 1
9	RO	Secondary Bandwidth Domain Reporting (SBD)	1'b 0
11:10		Reserved	
15:12	RO	Maximum Primary Stream Array Size (MaxPSASize)	4'h F
31:16	RO	xHCI Extended Capabilities Pointer (xECP)	16'h 0200

Register Name: Doorbell Offset

Address: Base + (14h)

Size: 32 bits

Bit	Attrib	Description	Default
1:0		Reserved	
31:2	RO	Doorbell Array Offset	30'h 0600

Register Name: Runtime Register Space Offset

Address: Base + (18h)

Size: 32 bits

Bit	Attrib	Description	Default
4:0		Reserved	
31:5	RO	Runtime Register Space Offset	28'h 080

6.4 Host Controller Operational Register

eXtensible Host Controller Operational Register				
31:24	23:16	15:8	7:0	Byte Offset
USB Command				00h
USB Status				04h
Page Size				08h
Reserved				0Ch-13h
Device Notification Control				14h
Command Ring Control				18h
Reserved				20h-2Fh
Device Context Base Address Array Pointer				30h
Configure				38h
Reserved				3Ch-3FFh
Port Register Set 1-4 (Refer to the table as below)				400-13FFh

Host Controller Port Register				
31:24	23:16	15:8	7:0	Byte Offset
Port Status and Control				00h
Port Power Management Status and Control				04h
Port Link Info				08h
Reserved				0Ch

Register Name: USB Command Register (USBCMD)

Address: OP Base + (00h)

Size: 32 bits

Bit	Attrib	Description	Default
0	RW	Run/Stop (R/S)	1'b 0
1	RWS	Host Controller Reset (HCRST)	1'b 0
2	RW	Interrupter Enable (INTE)	1'b 0
3	RW	Host System Error Enable (HSEE)	1'b 0
6:4		Reserved	

7	RW	Light Host Controller Reset (LHCRST)	1'b 0
8	RWS	Controller Save State (CSS)	1'b 0
9	RWS	Controller Restore State (CRS)	1'b 0
10	RW	Enable Wrap Event (EWE)	1'b 0
11	RW	Enable U3 MFINDEX Stop	1'b 0
31:12		Reserved	

Register Name: USB Status Register (USBSTS)

Address: OP Base + (04h)

Size: 32 bits

Bit	Attrib	Description	Default
0	RO	HCHalted (HCH)	1'b 1
1		Reserved	
2	RWS	Host System Error (HSE)	1'b 0
3	RWS	Event Interrupt (EINT)	1'b 0
4	RWS	Port Change Detect (PCD)	1'b 0
7:5		Reserved	
8	RO	Save State Status (SSS)	1'b 0
9	RO	Restore Status (RSS)	1'b 0
10	RWS	Save/Restore Error (SRE)	1'b 0
11	RO	Controller Not Ready (CNR)	1'b 1
12	RO	Host Controller Error (HCE)	1'b 0
31:13		Reserved	

Register Name: Page Size Register (PAGESIZE)

Address: OP Base + (08h)

Size: 32 bits

Bit	Attrib	Description	Default
3:0	RO	Page Size	4'h 1
31:4		Reserved	

Register Name: Device Notification Control Register (DNCTRL)

Address: OP Base + (14h)

Size: 32 bits

Bit	Attrib	Description	Default
15:0	RW	Notification Enable (No-N15)	16'h 0000
31:16		Reserved	

Register Name: Command Ring Control Register (CRCR)

Address: OP Base + (18h)

Size: 64 bits

Bit	Attrib	Description	Default
0	RWS	Ring Cycle State (RCS)	1'h 0
1	RWS	Command Stop (CS)	1'h 0
2	RWS	Command Abort (CA)	1'h 0
3	RO	Command Ring Running (CRR)	1'h 0
5:4		Reserved	
63:6	RWS	Command Ring Pointer	58'h 000

Register Name: Device Context Base Address Array Pointer Register (DCBAAP)

Address: OP Base + (30h)

Size: 64 bits

Bit	Attrib	Description	Default
5:0		Reserved	
63:16	RW	Device Context Base Address Array Pointer	16'h 0000 000

Register Name: Configure Register (CONFIG)

Address: OP Base + (38h)

Size: 32 bits

Bit	Attrib	Description	Default
7:0	RW	Max Device Slots Enabled (MaxSlotsEn)	8'h 00
31:8		Reserved	

Register Name: Port Status and Control Register (PORTSC)

Address: OP Base + (400h + (10h*(n-1))

Size: 32 bits

Bit	Attrib	Description	Default
0	RO	Current Connect Status (CCS)	1'b 0
1	RWS	Port Enable/Disable (PED)	1'b 0
2		Reserved	
3	RO	Over-Current Active (OCA)	1'b 0
4	RWS	Port Reset (PR)	1'b 0
7:5		Reserved	
8:5	RWS	Port Link State (PLS)	4'h 0
9	RWS	Port Power (PP)	1'b 0
13:10	RO	Port Speed	4'h 0
15:14	RWS	Port Indicator Control (PIC)	2'h 0
16	RWS	Port Link State Write Strobe (LWS)	1'b 0
17	RWS	Connect Status Change (CSC)	1'b 0
18	RWS	Port Enable/Disable Change (PEC)	1'b 0
19	RWS	Warm Port Reset Change (WRC)	1'b 0
20	RWS	Over-Current Change (OCC)	1'b 0
21	RWS	Port Reset Change (PRC)	1'b 0
22	RWS	Port Link State Change (PLC)	1'b 0
23	RWS	Port Config Error Change (CEC)	1'b 0
24		Reserved	
25	RWS	Wake on Connect Enable (WCE)	1'b 0
26	RWS	Wake on Disconnect Enable (WDE)	1'b 0
27	RWS	Wake on Over-Current Enable (WOE)	1'b 0
29:28		Reserved	
30	RO	Device Removable (DR)	1'b 0
31	RWS	Warm Port Reset (WPR)	1'b 0

Register Name: Port Power Management Status and Control Register (PORTPMSC)
(Under USB3.0 mode)

Address: OP Base + (404h + (10'h*(n-1))

Size: 32 bits

Bit	Attrib	Description	Default								
7:0	RWS	U1 Timeout <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>00h</td><td>Zero (default)</td></tr><tr><td>01h</td><td>1 us</td></tr><tr><td>02h</td><td>2 us</td></tr></tbody></table>	Value	Description	00h	Zero (default)	01h	1 us	02h	2 us	8'h 00
Value	Description										
00h	Zero (default)										
01h	1 us										
02h	2 us										

		7Fh	127us	
		80h-FEh	Reserved	
		FFh	Infinite	
15:8	RWS	U2 Timeout		8'h 00
		Value	Description	
		00h	Zero (default)	
		01h	256 us	
		02h	512 us	

		FEh	65.024 ms	
		FFh	Infinite	
16	RWS	Force Link PM Accept (FLA)		1'b 0
31:17		Reserved		

Register Name: Port Power Management Status and Control Register (PORTPMSC)

(Under USB2.0 mode)

Address: OP Base + (404h + (10'h*(n-1))

Size: 32 bits

Bit	Attrib	Description	Default
2:0	RO	L1 Status	3'b 000
		Value Description	
		0 Invalid	
		1 Success	
		2 Not Yet	
		3 Not Support	
		4 Timeout/Error	
		5-7 Reserved	
3	RW	Remote Wake Enable (RWE)	1'b 0
7:4	RW	Host Initiated Resume Duration (HIRD)	4'h 0
15:8	RW	L1 Device Slot	8'h 00
27:16		Reserved	1'b 0
31:28	RW	Port Test Control	4'h 0

Register Name: Port Link Info Register (PORTLI)

(under USB3.0 mode, for USB2.0 mode, this register is reserved.)

Address: OP Base + (408h + (10h*(n-1)))

Size: 32 bits

Bit	Attrib	Description	Default
15:0	RO	Link Error Count	16'h 0000
31:16		Reserved	

6.5 Host Controller Runtime Register

Host Controller Runtime Register				
31:24	23:16	15:8	7:0	Byte Offset
Microframe Index				0000h
Reserved				0004h-0020h
Interrupter Register Set 0				0020h
---				---
Interrupter Register Set 8				003Ch

Register Name: Microframe Index Register (MFINDEX)

Address: RT Base + (00h)

Size: 32 bits

Bit	Attrib	Description	Default
13:0	RO	Microframe Index	14'h 0000
31:14		Reserved	

Interrupter Register Set							
31:24	23:16	15:8	7:0		Byte Offset		
Reserved					IE	IP	00h
Interrupter Moderation Counter		Interrupter Moderation Interval				04h	
Reserved		Event Ring Segment Table Size				08h	
Reserved					0Ch		
Event Ring Segment Table Base Address Lo				Reserved		10h	
Event Ring Segment Table Base Address Hi					14h		
Event Ring Dequeue Pointer Lo				Reserved		18h	
Event Ring Dequeue Pointer Hi					1Ch		

Register Name: Interrupter Management Register (IMAN)

Address: RT Base + 020h + (32*Interrupter)

Size: 32 bits

Bit	Attrib	Description	Default
0	RWS	Interrupt Pending (IP)	1'b 0
1	RW	Interrupt Enable (IE)	1'b 0
31:2		Reserved	

Register Name: Interrupter Moderation Register (IMOD)

Address: RT Base + 024h + (32*Interrupter)

Size: 32 bits

Bit	Attrib	Description	Default
15:0	RW	Interrupt Moderation Interval (IMODI)	16'h 0FA0
31:16	RWS	Interrupt Moderation Counter (IMODC)	16'h 0000

Register Name: Event Ring Registers (ERSTSZ)

Address: RT Base + 028h + (32*Interrupter)

Size: 32 bits

Bit	Attrib	Description	Default
15:0	RW	Event Ring Segment Table Size	16'h 0000
31:16		Reserved	

Register Name: Event Ring Segment Table Base Address Registers (ERSTBA)

Address: RT Base + 030h + (32*Interrupter)

Size: 64 bits

Bit	Attrib	Description	Default
3:0		Reserved	
63:4	RWS	Event Ring Segment Table Base Address Register	60'h 0000 000

Register Name: Event Ring Dequeue Pointer Register (ERDP)

Address: RT Base + 038h + (32*Interrupter)

Size: 64 bits

Bit	Attrib	Description	Default
2:0	RW	Dequeue ERST Segment Index (DESI)	3'h 0
3	RWS	Event Handle Busy (EHB)	1'b 0

63:4	RWS	Event Ring Dequeue Pointer	61'h 0000 000
------	-----	----------------------------	---------------

6.6 Doorbell Registers

Doorbell Registers				
31:24	23:16	15:8	7:0	Byte Offset
DB Stream ID		Reserved	DB Target	0000h

Address: it is a Dword aligned calculated by adding the value in the DBOFF register to "Base"

Size: 32 bits

Bit	Attrib	Description	Default
7:0	RW	DB Target Device Context Doorbell (1-255)	8'h 00
15:8		Reserved	
31:16	RW	DB Stream ID	16'h 0000

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

The below stress value parameter shows absolute maximum rating which may cause the device to have permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over those parameter in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply for VCC	-0.5 ~ VCC+0.5	V
Power Supply for VDD	-0.5 ~ VDD+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

7.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
VCC, VCCU, VCCP	Normal Power Supply for IO and PHY	3.0	3.3	3.6	V	
VDD, VDDU, VDDP	Normal Power Supply for Core Logic	1.14	1.2	1.26	V	
VCC_SUS	Suspend Power Supply for PHY	3.0	3.3	3.6	V	
VDD_SUS	Suspend Power Supply for Logic	1.14	1.2	1.26	V	
T _J	Operating Junction Temperature	0	25	120	°C	
T _C	Operating Case Temperature			85	°C	
HBM ESD	Human Body Mode ESD capability		2		KV	
MM ESD	Machine mode ESD capability		200		V	

Chip Temperature (T_J, T_C) Calculation

Symbols	Parameter	How to get?
T _A	Ambient temperature	Measure temperature around chip
T _J	Operating junction temperature	$T_J = \Theta_{JA} * Power + T_A$
T _C	Operating case temperature	$T_C = T_J - \Psi_{JT} * Power$
Θ_{JA}	Junction to Ambient thermal resistance	23.8 (data from package vender)
Ψ_{JT}	Junction to top thermal characterization	0.08 (data from package vender)
Power	Chip power consumption	Measure chip power consumption

- Thermal test board condition, please refer to JEDEC JESD51-5
- Thermal test method environmental conditions refer to JESD51-2
- Example: If chip power consumption is 0.9W; T_A=40°C
 $T_J = 23.8 * 1.5 + 40 = 75.7^{\circ}\text{C}$
 $T_C = 75.7 - 0.08 * 1.5 = 75.58^{\circ}\text{C}$

7.3 AC/DC Characteristics

Digital Pin Specification

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
V _{IH}	Input High Level	2.0		VCC	V	
V _{IL}	Input Low Level	-0.5		0.8	V	

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
I _{LEAK}	Input Leakage Level			10	uA	
V _{OH}	Output High Level	2.4		VCC	V	
V _{OL}	Output Low Level	-0.5		0.5	V	

PCI Express Electrical Specification

(Refer to PCI Express Base Specification Rev. 3.0)

USB3.1 Electrical Specification

(Refer to Universal Serial Bus 3.1 Specification Rev. 1.0)

USB2.0 Electrical Specification

(Refer to Universal Serial Bus Specification Rev. 2.0)

PCI Express Differential Reference Clock Input Ranges

Symbols	Parameter	Min	Typ	Max	Unit	Remark
F _{IN-DIFF}	The input frequency is 100 MHz + 300 ppm and max. – 5000 including SSC-dictated variations Differential input frequency		100		MHz	
	Rising Edge Rate	0.6		4.0	V/ns	
	Falling Edge Rate	0.6		4.0	V/ns	
V _{IH}	Differential Input High Voltage	150			mV	
V _{IL}	Differential Input Low Voltage			-150	mV	
V _{CROSS}	Absolute crossing point voltage	250		550	mV	
V _{CROSS-DELTA}	Variation of V _{CROSS} over all rising clock edges			140	mV	
V _{RB}	Ring-back Voltage Margin	-100		100	mV	
T _{STABLE}	Time before V _{RB} is allowed	500			ps	
T _{PERIOD-AVG}	Average Clock Period Accuracy	-300		2800	ppm	
T _{PERIOD-ABS}	Absolute Period (including Jitter and Spread Spectrum)	9.847		10.203	ns	
T _{CC-JITTER}	Cycle to Cycle Jitter			150	ps	
V _{MAX}	Absolute Max input voltage			1.15	V	
V _{MIN}	Absolute Min input voltage			-0.3	V	
	Duty Cycle	40		60	%	
R/F Matching	Rising edge rate (REFCLK+) to Falling edge rate (REFCLK-) matching			20	%	
Z _{C-DC}	Clock source DC impedance	40		60	Ω	

20MHz Crystal Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f _{XTAL}	Frequency		20		MHz
Δf _{XTAL}	Long Term Stability (at 250C)	-30		30	ppm
T _C	Temperature Stability	-30		30	ppm
F _A	Aging	-5		5	ppm
C _L	Load Capacitance (Single-end mode)		16		pF

Symbol	Parameter	Min.	Typ	Max.	Unit
C ₀	Shunt Capacitance	1	3	7	pF

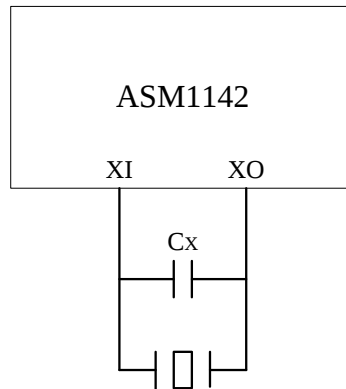


Figure 3: Differential Crystal Design

20MHz Clock input Electrical Specification (from 20MHz crystal)

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f _{CLK}	Frequency		20		MHz
Δf _{CLK}	Long Term Stability (all condition)	-150		150	ppm
C _x	External Load Capacitance (Differential mode)		C _{TOTAL} -C ₀		pf
C _{TOTAL}	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R _{TOTAL}	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

Power Consumption

Symbol	Parameter	Power	Min.	Typ	Max.	Unit
Idle	Enter idle state with attached devices	3.3V normal	225	250	275	mA
		3.3V suspend		1	5	mA
		1.2V normal	495	550	605	mA
		1.2V suspend		1	5	mA
S3/S4	Enter system S3/S4 state	3.3V normal		1	5	mA
		3.3V suspend		1	5	mA
		1.2V normal		1	5	mA
		1.2V suspend		1	5	mA
Burn in	two USB3.1 Gen-II devices running burn in testing simultaneously	3.3V normal	225	250	275	mA
		3.3V suspend		1	5	mA
		1.2V normal	575	640	705	mA
		1.2V suspend		1	5	mA

8. Timing Diagram

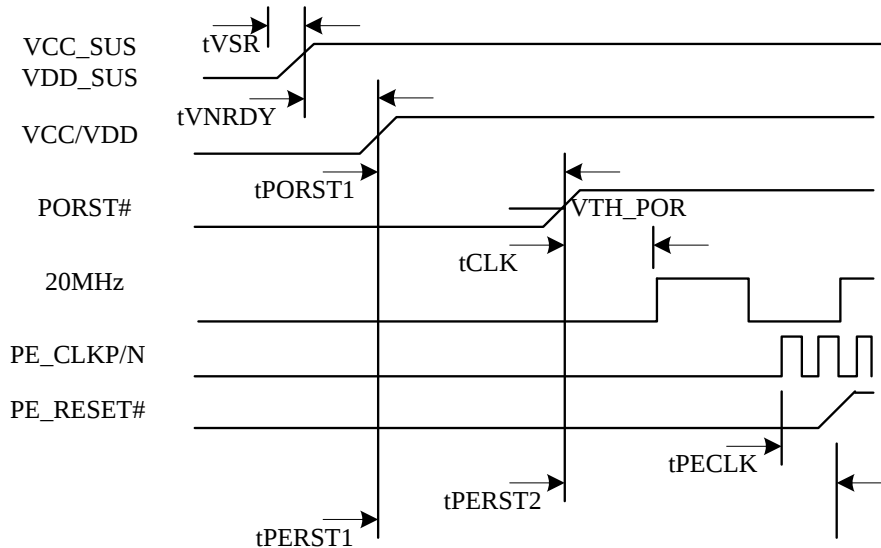


Figure 4: Power On Sequence for Asynchronous mode

Power On Sequence Timing Specification for Asynchronous mode

Symbols	Parameter	Min	Typ	Max	Unit	Remark
V _{TH_POR}	Threshold voltage for PORST# pins	1.38	1.6	1.8	V	
t _{VSR}	Rising time for Suspend Power Ready			10	ms	
t _{VNRDY}	Timing for Normal Power Ready	50			ms	
t _{PORST1}	Timing for 1.2V/3.3V Normal Power Ready to Power On Reset	2		80	ms	
t _{PECLK}	Timing for PE_CLK Ready to PE_RST#	100			μs	
t _{CLK}	Timing for 20MHz Crystals Clock Ready to Power On Reset (relate to max value of V_{TH_POR})			2	ms	
t _{PERST1}	Timing for PE_RST# delay after Normal Power Ready (D3Cold)	210			ms	
	Timing for PE_RST# delay after Normal Power Ready (D3Hot)	250			ms	
t _{PERST2}	Timing for PE_RST# delay after PORST# comes up	200			ms	

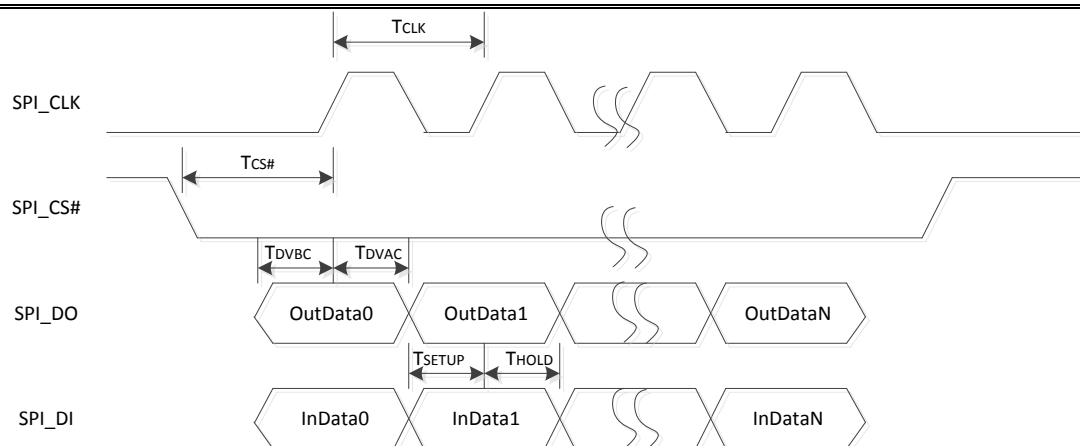


Figure 5: SPI Type Serial ROM Signal Interface

SPI Interface Timing Specification

Symbols	Parameter	Min	Typ	Max	Unit	Remark
T_{CLK}	SPI_CLK Clock Period	102	112	122	ns	
$T_{CS\#}$	SP_CS# Active to the 1 st clock rising edge	100	112	124	ns	
T_{DVBC}	SPI_DO data valid before clock	48	56	64	ns	
T_{DVAC}	SPI_DO data valid after clock	48	56	64	ns	
T_{SETUP}	SPI_DI setup time	20			ns	
T_{HOLD}	SPI_DI hold time	1			ns	

9. PCB Design Guide under Thermal Pad

To improve the thermal efficiency and signal integrity, it is recommended to place the thermal-via under or near to thermal pad. To avoid process issues, please make sure the thermal-via is completely filled with solder paste covered by solder mask. It is recommended to follow up the pattern on PCB as Figure 7 or Figure 8.

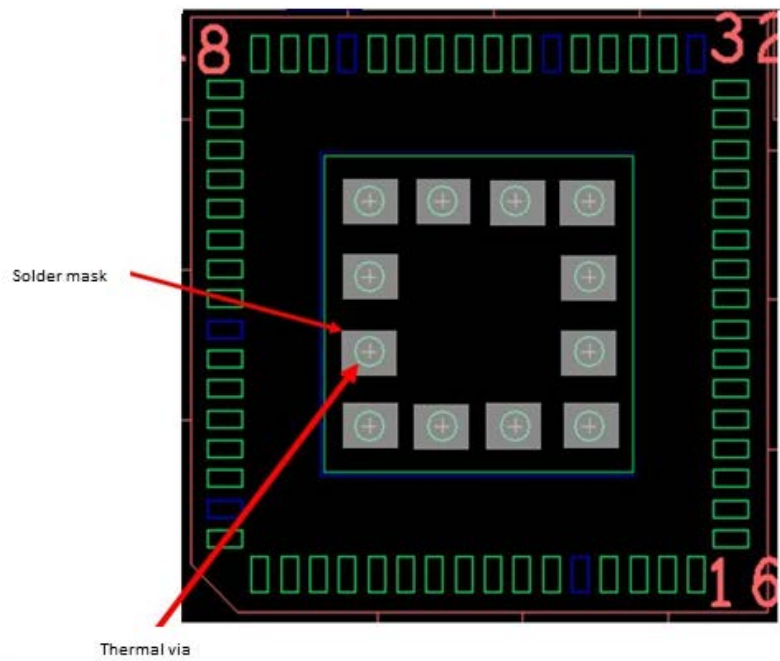


Figure 6: Symbol 1 for via design rule under Thermal pad

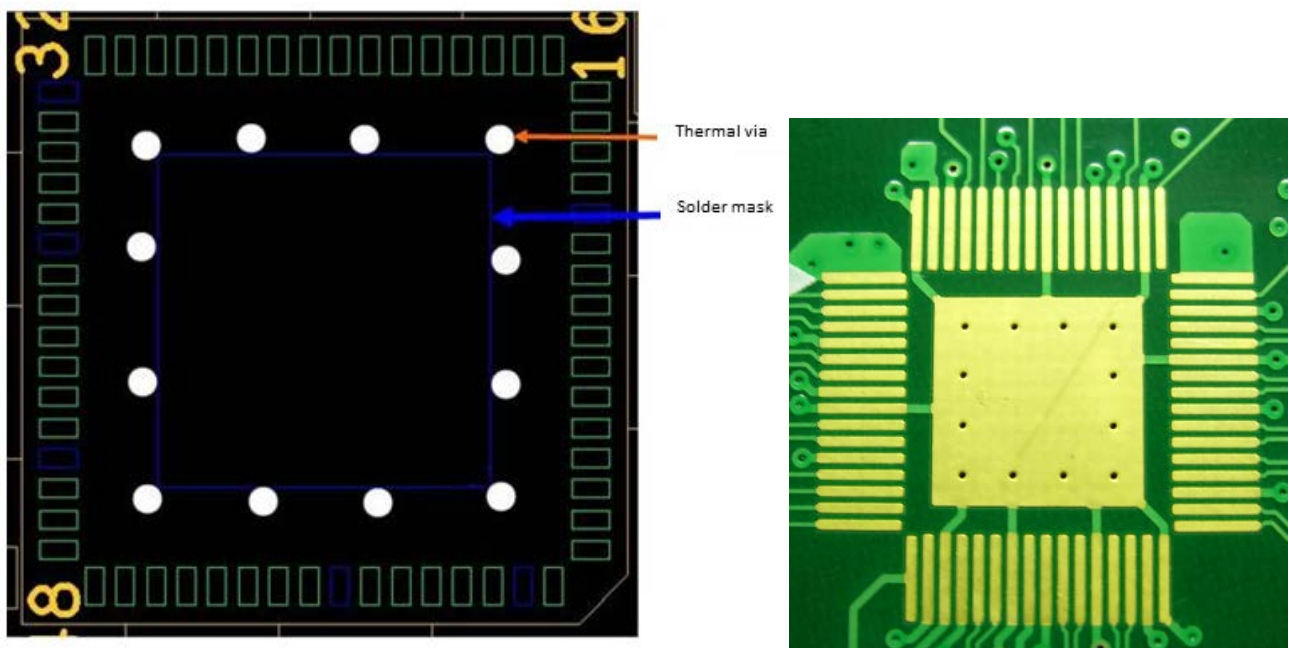


Figure 7: Symbol 2 for via design rule under Thermal pad

*CONTROLLING DIMENSION : MM						
SYMBOL	MILLMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.30	0.008	0.010	0.012
D/E	9.00 bsc			0.354 bsc		
D1/E1	8.75 bsc			0.344 bsc		
D2/E2	5.007	5.207	5.407	0.197	0.205	0.213
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.10	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure 8: Mechanical Specification – QFN 64