ASMEDIA TECHNOLOGY INC



# ASM235CM Datasheet

## USB Type-C USB 3.1 Gen 2/Gen 1 to SATA Bridge Controller

# 1. General Description

Engaged in Universal Serial Bus I/O solutions and storage application developments, ASMedia Technology is committed on expanding product portfolio with introducing a new generation of USB 3.1 to SATA 6Gbps bridge solution for USB Type-C storage application.

ASM235CM is the latest generation of ASMedia's single chip solution, bridging the USB3.1 to Serial ATA host interface with highly integrated SuperSpeedPlus, SuperSpeed, High Speed, SATA 1.5/3.0/6.0 Gbps ASMedia self-designed PHYs as well as built-in CC logic circuit enabling reversible USB cable orientation and direction. Along with excellent compatibility with USB3.1 hosts and SATA devices, ASM235CM utilizes advanced process technology to optimize the chip power consumption.

Customers can easily enhance their storage device performance with ASM235CM since it also integrates an 8-bit micro-processor and embedded RAM to provide a cutting edge solution in USB to SATA device enclosure market.

# 2. Features

- ◇ Compliant with USB3.1 Specification Revision 1.0
- ◇ Compliant with Type-C Specification Revision 1.1
- ◇ Compliant with USB Specification Revision 2.0
- ◇ Support USB Super-Speed Plus, USB Super-Speed, High-Speed and Full-Speed Operation
- ◇ Support USB Mass Storage Class, Bulk-Only Transport Specification Revision 1.3
- ◇ Support USB Attached SCSI Protocol Specification Revision 1.0
- ◇ Compliant with Serial ATA Specification Revision 3.2
- ◇ Serial ATA bus up to 6Gbps Signal bandwidth
- ◇ Support Spread Spectrum Control of USB3.0 and SATA interface to improve the EMI performance
- ◇ Support ATA/ATAPI Packet Command Set
- ◇ Support ATA/ATAPI LBA48 addressing mode(28-bit LBA SATA devices are not supported due to OS limitations)
- ◇ Integrated 8-bit micro-processor with embedded program RAM and ROM
- ◇ Support SPI NVRAM for Vender Specific Application of USB Device Controller
- ◇ Support multi-GPIO pins
- ◇ Support programmable PWMs
- ◇ Support 25 MHz with external crystal mode
- ◇ Integrated two internal voltage regulator for IO power and Core

# 3. Package Type

◇ Green Package 6x6 QFN 48L (Pb-free)

# 4. Functional Diagram

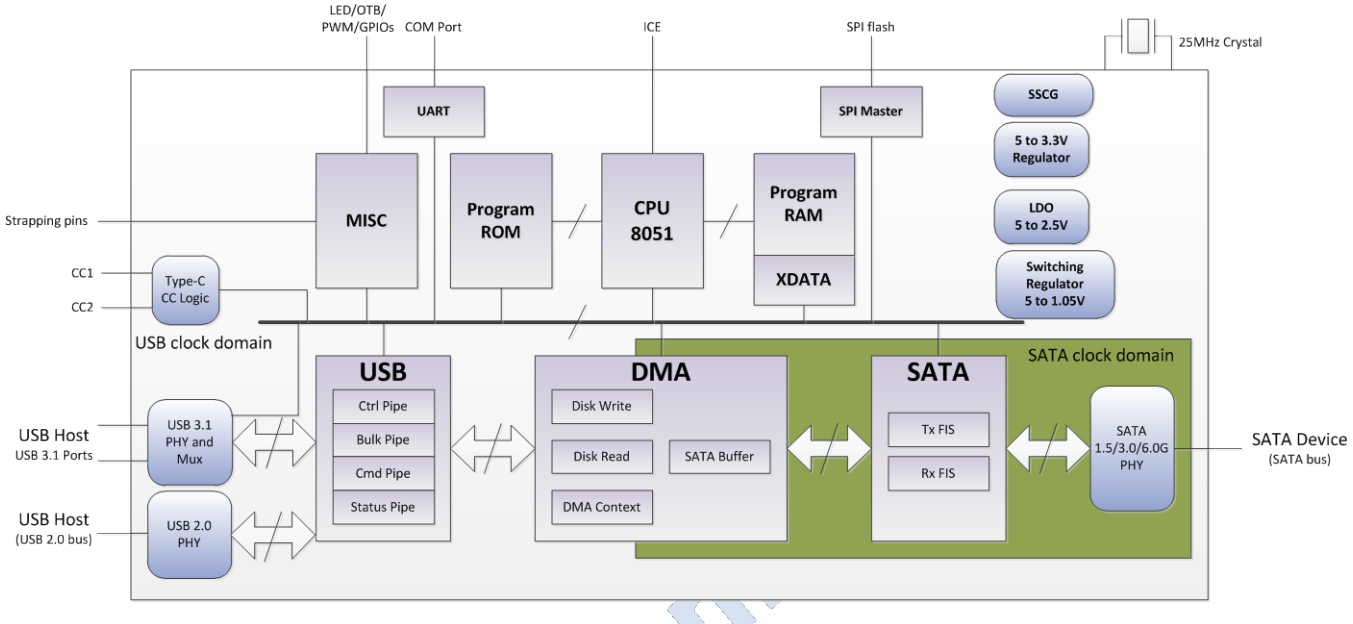



**Figure 1: Functional Diagram of ASM235CM**

# 5. Pinout Diagrams

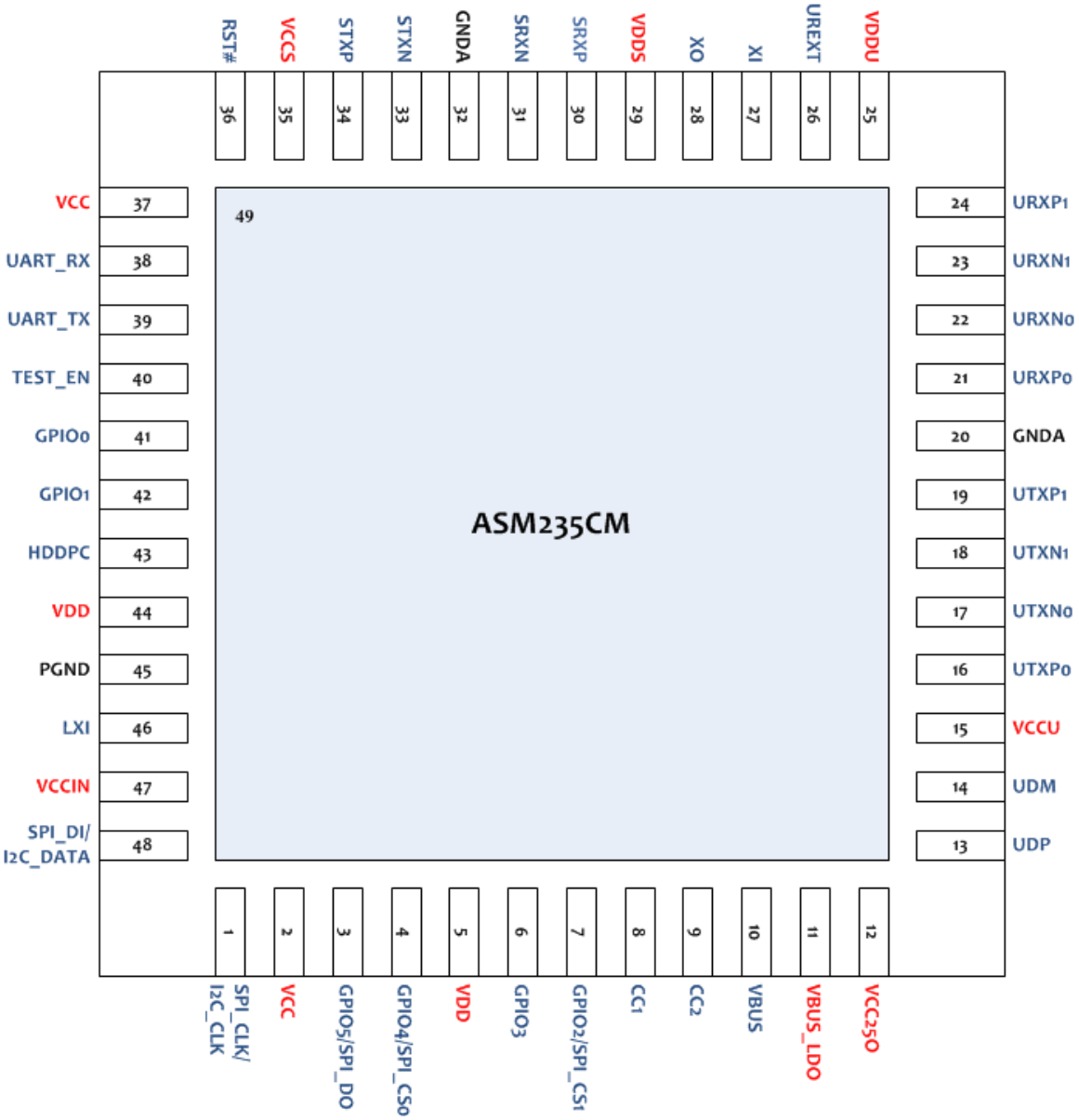



**Figure 2: ASM235CM Pinout**

# 6. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

| I/O Type | Definition |
|---|---|
| I | Input pin |
| O | Output pin |
| B | Bi-directional pin |
| P | Power pin |
| G | Ground pin |
| OD | Open Drain |

| Pin No. | Name | TYPE | Descriptions |
|---|---|---|---|
| USB interface | | | |
| 14 | UDM | B | USB2.0 negative Data Signal |
| 13 | UDP | B | USB2.0 positive Data Signal |
| 17 | UTXN0 | O | SuperSpeedPlus USB negative Transmitter Signal for port0 |
| 16 | UTXP0 | O | SuperSpeedPlus USB positive Transmitter Signal for port0 |
| 22 | URXN0 | I | SuperSpeedPlus USB negative Receiver Signal for port0 |
| 21 | URXP0 | I | SuperSpeedPlus USB positive Receiver Signal for port0 |
| 18 | UTXN1 | O | SuperSpeedPlus USB negative Transmitter Signal for port1 |
| 19 | UTXP1 | O | SuperSpeedPlus USB positive Transmitter Signal for port1 |
| 23 | URXN1 | I | SuperSpeedPlus USB negative Receiver Signal for port1 |
| 24 | URXP1 | I | SuperSpeedPlus USB positive Receiver Signal for port1 |
| SATA interface | | | |
| 30 | SRXP | I | SATA positive Receiver Signal |
| 31 | SRXN | I | SATA negative Receiver Signal |
| 33 | STXN | O | SATA negative Transmitter Signal |
| 34 | STXP | O | SATA positive Transmitter Signal |
| System Signals | | | |
| 40 | TEST_EN | I | Test Enable Signal, with internal pull-down resistor<br>0: Normal Mode (Default)<br>1: Test Mode Enable |
| 48 | I2C_DATA | B | Used as I2C_DATA signal or SPI_DI signal. Used as General Purpose IO after power on. Integrated pull-up resistor. |
| 1 | I2C_CLK | B | Used as I2C_CLK signal or SPI_CLK signal. Used as General Purpose IO after power on. Integrated pull-up resistor. |
| 3 | GPIO5 | B | General Purpose IO, used as SPI_DO, with internal pull-up resistor. |
| 4 | GPIO4 | B | General Purpose IO, used as SPI_CS0, with internal pull-up resistor. |
| 6 | GPIO3 | B | General Purpose IO. Integrated pull-up resistor. |
| 7 | GPIO2 | B | General Purpose IO, used as SPI_CS1 or LED2, with internal pull-up resistor. |
| 38 | UART_RX | B | URAT_RX while debug mode. Used as General Purpose IO after power on. Integrated pull-up resistor. |
| 39 | UART_TX | B | UART_TX while debug mode. Used as General Purpose IO after power on. Integrated pull-up resistor. |
| 41 | GPIO0 | B | General Purpose IO. Integrated pull-up resistor. |
| 42 | GPIO1 | B | General Purpose IO. Used as LED1. Integrated pull-up resistor. |
| 43 | HDDPC | B | HDD power control pin, use as General Purpose IO. Integrated pull-up resistor.<br>0: Hard Drive Power Off<br>1: Hard Drive Power On<br>**Note: It is strongly recommended to implement HDDPC control circuitry. To avoid power surge caused by some SATA drives, particularly SSDs, during power-up, proper RC delay or slew rate control is required in HDDPC circuitry. Please refer to reference design schematic and FAE for details.** |
| 10 | VBUS | I | USB Cable Power Detector |

| Pin No. | Name | TYPE | Descriptions |
|---|---|---|---|
| 26 | REXT | **P** | External Reference Resistor with 12.1Kohm +/-1% |
| 36 | RST# | I | Power Reset pin |
| Clock Interface | | | |
| 27 | XI | I | Crystal input or Clock input pin |
| 28 | XO | O | Crystal output or Clock output pin |
| Type-C Interface | | | |
| 8 | CC1 | B | Type-C Configuration Channel 1 for USB SuperSpeedPlus port0 |
| 9 | CC2 | B | Type-C Configuration Channel 2 for USB SuperSpeedPlus port1 |
| Voltage Regulator | | | |
| 11 | VBUS_LDO | **P** | Linear regulator input<br>**Please always keep 5V input on this pin even if external 5V to 2.5V power solution is used.** |
| 12 | VCC25O | **P** | Linear regulator output |
| 47 | VCCIN | **P** | Switching regulator input |
| 46 | LXI | **P** | Connect with external inductor |
| 45 | PGND | **G** | Ground for voltage regulator |
| Power and Ground | | | |
| 15 | VCCU | **P** | USB high power pin |
| 35 | VCCS | **P** | SATA high power pin |
| 25 | VDDU | **P** | USB low power pin |
| 29 | VDDS | **P** | SATA low power pin |
| 5, 44 | VDD | **P** | Core power |
| 2, 37 | VCC | **P** | IO power |
| 20, 32 | GNDA | **G** | Analog Ground |
| 49 | GND | **G** | the exposed pad connected to common ground on PCB |

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings

Stressing the below parameters listed over the absolute maximum rating may cause the device permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over these parameters in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal exhibit voltage spikes while power is switched on or off.

| Parameter | Range | Unit |
|---|---|---|
| **Power Supply for VCC** | -0.5 ~ VCC+0.5 | V |
| **Power Supply for VDD** | -0.5 ~ VDD+0.5 | |
| **DC Input Voltage** | -0.5 ~ VCC+0.5 | V |
| **Output Voltage** | -0.5 ~ VCC+0.5 | V |
| **Storage Temperature** | JEDEC J-STD-033B MSL 3 | |

## 7.2 Recommended Operating Conditions

| Symbols | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **$V_{CC}$** | IO Power Supply | 2.25 | 2.5/3.3 | 3.6 | V |
| **$V_{CCU}$** | USB Analog High Power Supply | 2.25 | 2.5 | 2.75 | V |
| **$V_{CCS}$** | SATA Analog High Power Supply | 2.25 | 2.5 | 2.75 | V |
| **$V_{DD}$** | Core Power Supply | 0.945 | 1.05 | 1.1025 | V |
| **$V_{DDU}$** | USB Analog Low Power Supply | 0.945 | 1.05 | 1.1025 | V |
| **$V_{DDS}$** | SATA Analog Low Power Supply | 0.945 | 1.05 | 1.1025 | V |
| **$T_C$** | Operating Case Temperature | | | 85 | $^0$C |
| **$T_J$** | Operating Junction Temperature | 0 | 25 | 120 | $^0$C |
| **HBM** | Human Body mode ESD | | 2.5 | | KV |
| **MM** | Machine Mode ESD | | 150 | | V |

### Chip Temperature (Ta, Tj) Calculation

| Symbols | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **$T_a$** | Ambient Temperature | Measure Temperature Around Chip | | | |
| **$T_j$** | Operating Junction Temperature | $T_j = \Theta_{ja}$ * Power+ $T_a$ | | | |
| **$T_C$** | Operating Case Temperature | $T_C = T_j - \Psi_{jt}$* Power | | | |
| **$\Theta_{ja}$** | Junction to Ambient Thermal Resistance | Provided by Package Vendor. For QFN48, $\Theta_{ja}$ =30.7 | | | |
| **$\Psi_{jt}$** | Junction to Top Thermal Characterization | Provided by Package Vendor. For QFN48, $\Psi_{jt}$ =0.11 | | | |
| **Power** | Chip Power Consumption | Measured Chip Power Consumption | | | |

**Note:**

Thermal test board condition, please refer to JEDEC JESD51-5

Thermal test method environmental conditions refer to JESD51-2

Example: IF chip power consumption is 0.7W; $T_a$ =40°C

$T_j$ =30.7 *0.7+40=61.49°C

$T_C$ =61.49-0.11*0.7=61.413°C

## 7.3 DC Electrical Characteristics for VBUS pin

| Symbols | Parameter | VCC=3.3V | | | VCC=2.5V | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{IH}$ | Input High Voltage Level | 2.0 | | | 1.7 | | | V |
| $V_{IL}$ | Input Low Voltage Level | | | 0.8 | | | 0.6 | V |
| $V_{HYS}$ | Input Hysteresis | 0.32 | 0.37 | 0.4 | 0.3 | 0.333 | 0.36 | mV |
| $V_{TH-L2H}$ | VTH of Schmitt Trigger low to high | 1.4 | 1.6 | 1.8 | 1.1 | 1.294 | 1.5 | V |
| $V_{TH-H2L}$ | VTH of Schmitt Trigger high to low | 1 | 1.23 | 1.4 | 0.8 | 0.961 | 1.1 | V |

## 7.4 DC Electrical Characteristics for GPIO pins

| Symbols | Parameter | VCC=3.3V | | | VCC=2.5V | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{IH}$ | Input High Voltage Level | 2.0 | | | 1.7 | | | V |
| $V_{IL}$ | Input Low Voltage Level | | | 0.8 | | | 0.6 | V |
| $V_{HYS}$ | Input Hysteresis | 0.32 | 0.37 | 0.4 | 0.3 | 0.333 | 0.36 | mV |
| $V_{TH-L2H}$ | VTH of Schmitt Trigger low to high | 1.4 | 1.6 | 1.8 | 1.1 | 1.294 | 1.5 | V |
| $V_{TH-H2L}$ | VTH of Schmitt Trigger high to low | 1 | 1.23 | 1.4 | 0.8 | 0.961 | 1.1 | V |
| $V_{OH}$ | Output High Voltage Level | 2.4 | | | 2.0 | | | V |
| $V_{OL}$ | Output Low Voltage Level | | | 0.4 | | | 0.3 | V |
| $I_{OH}$ | Output Driving Current @$V_{OH}$ | 12 | | | 8 | | | mA |
| $I_{OL}$ | Output Driving Current @$V_{OL}$ | 12 | | | 8 | | | mA |
| $R_{UP}$ | Internal Pull-up resistance while Vin=0V | 65 | 96 | 140 | 86 | 136 | 210 | KΩ |
| | Internal Pull-up resistance while Vin=VCC/2 V | 38 | 56 | 81 | 48 | 75 | 114 | KΩ |
| $R_{DN}$ | Internal Pull-down resistance while Vin=VCC | 59 | 96 | 142 | 71 | 126 | 200 | KΩ |
| | Internal Pull-down resistance while Vin=VCC/2 V | 35 | 55 | 79 | 39 | 68 | 106 | KΩ |
| $I_{IL-UP}$ | Input pull-up leakage current after Vin is read, Rup is off & Iil < 1uA when VIN=0 | 21 | 34.4 | 56 | 10 | 18.4 | 32 | uA |
| | Input pull-up leakage current after Vin is read, Rup is off & Iil < 1uA when VIN=VCC/2 | 18 | 29.4 | 47 | 9.8 | 16.6 | 29 | uA |
| $I_{IL-DN}$ | Input pull-down leakage current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC | 21 | 34.5 | 60 | 11 | 20 | 38.5 | uA |
| | Input pull-down leakage current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC/2 | 18 | 30 | 50 | 10 | 18.5 | 35 | uA |

## 7.5 DC Electrical Characteristics for RST# pins

| Symbols | Parameter | VCC=3.3V | | | VCC=2.5V | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{IH}$ | Input High Voltage Level | 2.6 | | | 1.95 | | | V |
| $V_{IL}$ | Input Low Voltage Level | | | 1.4 | | | 0.9 | V |
| $V_{HYS}$ | Input Hysteresis | 0.21 | 0.23 | 0.25 | 0.2 | 0.22 | 0.25 | mV |
| $V_{TH-L2H}$ | VTH of Schmitt Trigger low to high | 1.9 | 2.2 | 2.55 | 1.37 | 1.65 | 1.94 | V |
| $V_{TH-H2L}$ | VTH of Schmitt Trigger high to low | 1.65 | 1.97 | 2.35 | 1.12 | 1.43 | 1.74 | V |
| $I_{IL}$ | Input pull-up leakage current while Vin=0V | | | 1 | | | 1 | uA |

## 7.6 External Crystal Electrical Specification

Note: please refer to the figure 3

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $f_{XTAL}$ | Frequency | | 25 | | MHz |
| $\Delta f_{XTAL}$ | Long Term Stability (at $25^0$C) | -30 | | 30 | ppm |
| $T_C$ | Temperature Stability | -30 | | 30 | ppm |
| $F_A$ | Aging | -5 | | 5 | ppm |
| $C_L$ | Load Capacitance (Single-end mode) | | 16 | | pF |
| $C_0$ | Shunt Capacitance | 1 | 3 | 7 | pF |

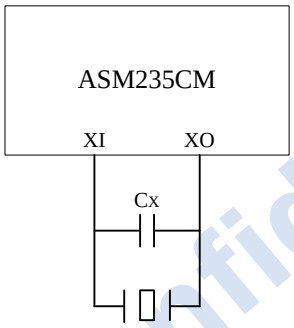



**Figure 3: Differential Crystal Design**

## 7.7 Differential Clock Oscillator Electrical Specification

Note: please refer to the figure 3

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $f_{CLK}$ | Frequency | | 25 | | MHz |
| $\Delta f_{CLK}$ | Long Term Stability (all condition) | -150 | | 150 | ppm |
| $C_X$ | External Load Capacitance (Differential mode) | | 10 | | pF |
| $C_{TOTAL}$ | Total External Equivalent Capacitance from XI pin to XO pin (Differential mode) | 9 | 11 | 15 | Pf |
| $R_{TOTAL}$ | Total External Equivalent Series Resistance from XI pin to XO pin | | | 60 | Ω |

## 7.8 Internal Linear Regular Electrical Specification

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IN\_LINEAR}$ | Input Voltage Range for internal linear regulator | 4.0 | 5 | 5.5 | V |
| $V_{OUT\_LINEAR}$ | Output Voltage Range for internal linear regulator | 2.375 | 2.5 | 2.625 | V |
| $I_{MAX}$ | Maximum capacity of current output | | | 230 | mA |

## 7.9 Internal Switching Regular Electrical Specification

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IN\_SWITCH}$ | Input Voltage Range for internal switching regulator | 4.0 | | 5.5 | V |
| $V_{OUT\_SWITCH}$ | Output Voltage Range for internal switching regulator | 1.0 | 1.05 | 1.1 | V |
| $\Delta V_N$ (p-p) | 5V input voltage noise/ripple Range | -8 | | 8 | % |
| $F_{OSC}$ | OSC frequency | | 1.5 | | MHz |
| $I_{MAX}$ | Maximum capacity of current output | | | 300 | mA |
| $IP_{(LM)}$ | P-channel current limiter | | 1 | | A |

- **Strong recommendation to have 10uF decoupling capacitor placed close to pin47 to filter the noise/ripple of switching regulator input, VCCIN.**

## 7.10 USB Type-C CC Channel Specification

| Symbols | Parameter | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| tCCDebounce | Delay time for Debounce on CC bus while device attached | 100 | | 200 | ms | |

- **External resistors, Rd, are required to be pulled-down on CC1 and CC2.**

# 8. Power on Sequence

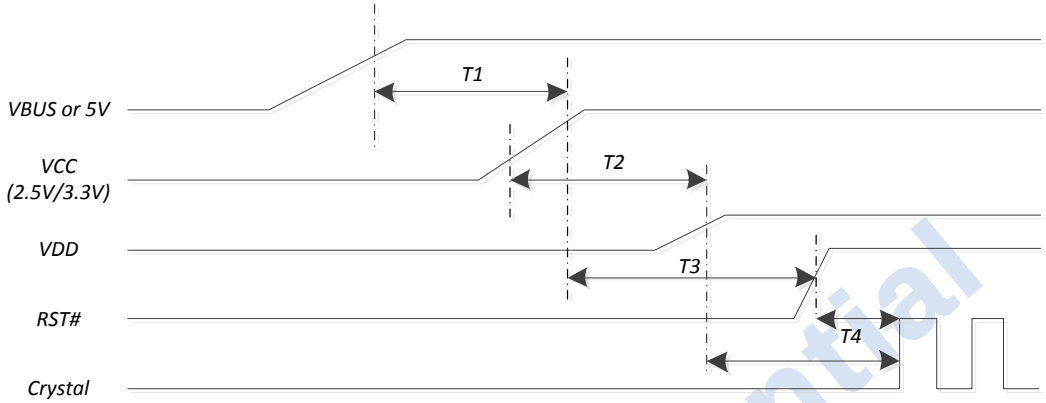



**Figure 4: Timing diagram**

| Symbols | Parameter | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| **T1** | The delay of VCC after 5V or VBUS is available | 0 | 5 | 10 | ms | Measure from 90% of VCC Internal to 90% of 5V or VBUS |
| **T2** | The delay of VDD after VCC is available | N/A | | 90 | ms | Measure from 10% of VCC to 90% of VDD |
| **T3** | The delay of RST# after VCC is available | 0 | | N/A | ms | 3.3V IO: Measure from 90% of VCC to 2V of RST#<br>2.5V IO: Measure from 90% of VCC to 1.7V of RST# |
| **T4** | The crystal clock is stable after RST# and VDD is available | 22.3 | 65 | 107.2 | ms | 3.3V IO: Measure from 90% of VDD or 2V of RST#<br>2.5V IO: Measure from 90% of VDD or 1.7V of RST# |
| **$T_{SLEW-VBUS-5V}$** | Slew rate of VBUS or 5V | N/A | | 30 | ms | Internal LDO:Measure from 10% to 90% of VBUS or 5V<br>External LDO:No need to check this timing |
| **$T_{SLEW-VDD}$** | Slew rate of VDD | 0 | | 10 | ms | Measure from 10% to 90% of VDD |

# 9. PCB Design Guide under Thermal Pad

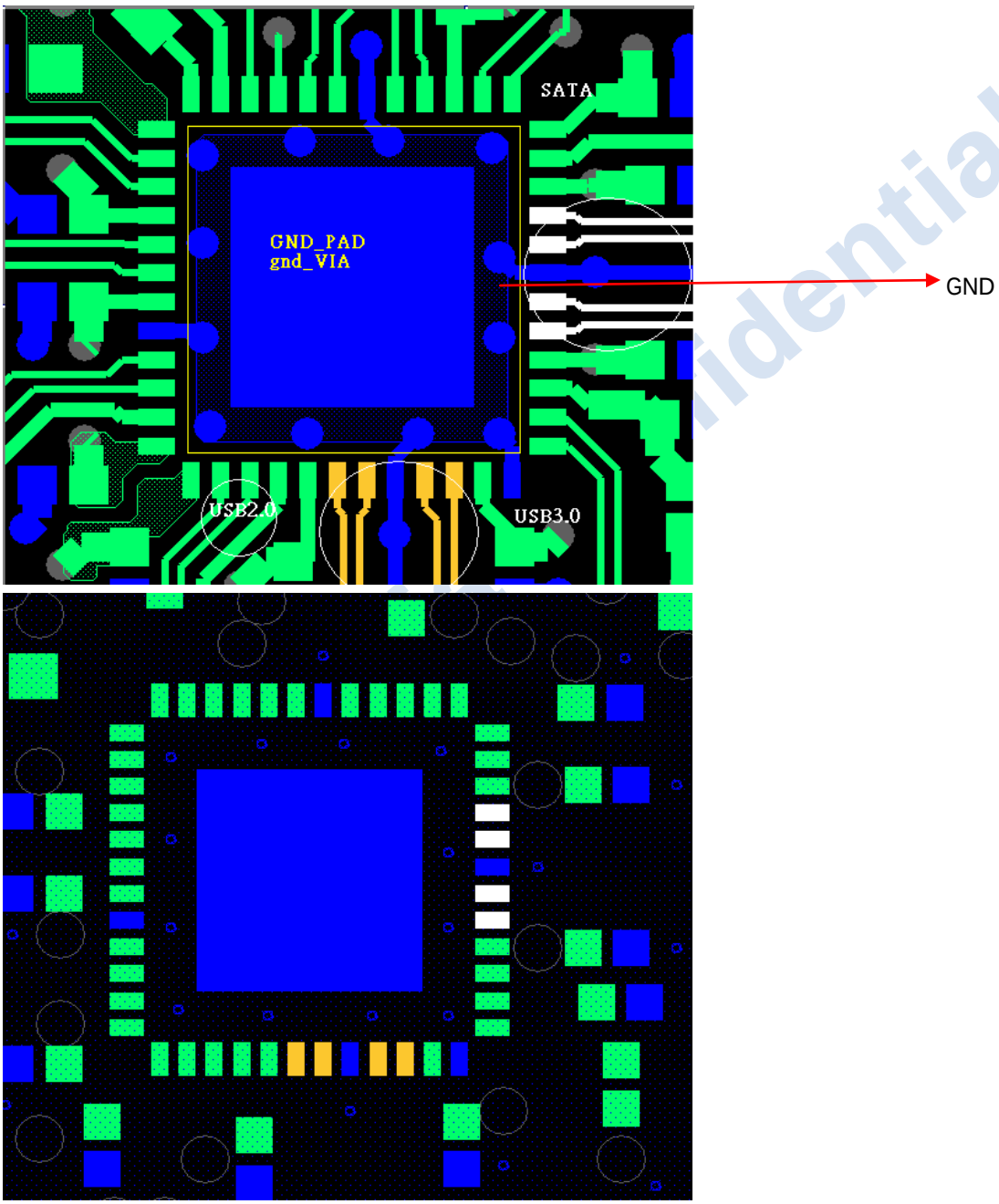
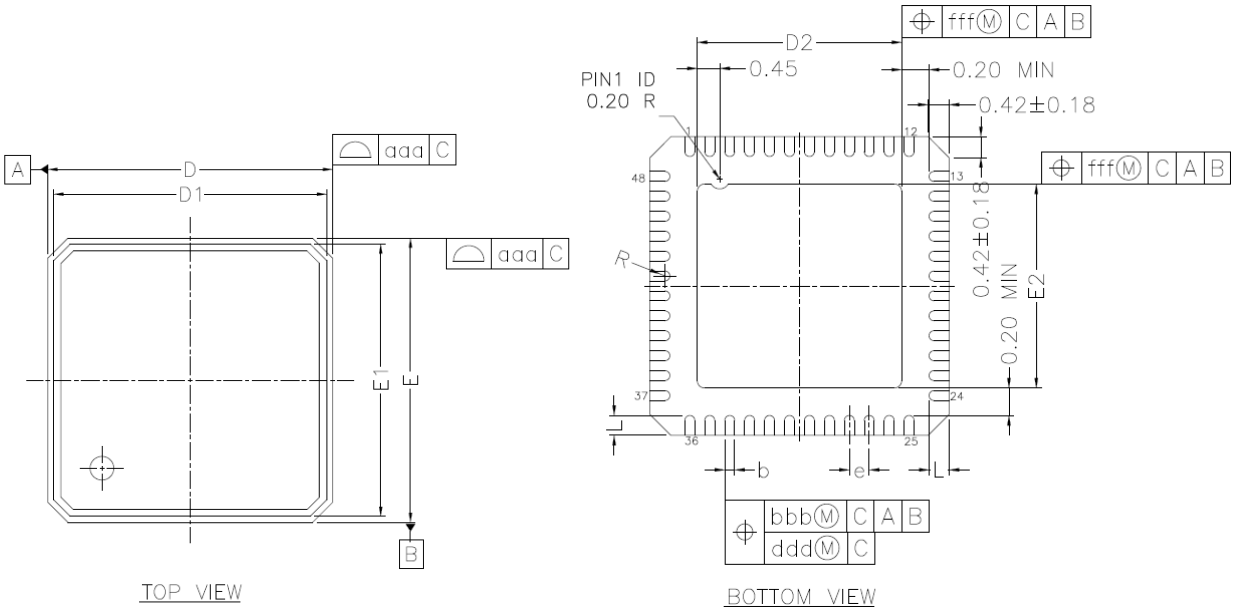


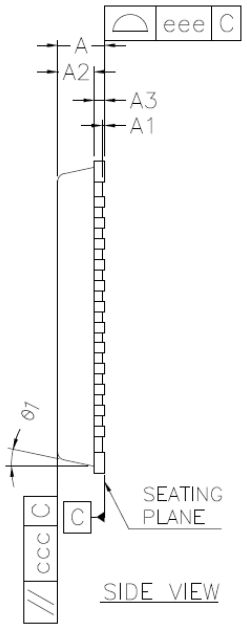

**Figure 5: Symbol 1 for via design rule under Thermal pad**

# 10. Package Information




* CONTROLLING DIMENSION : MM

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.02 | 0.05 | 0.00 | 0.001 | 0.002 |
| A2 | 0.60 | 0.65 | 0.70 | 0.024 | 0.026 | 0.028 |
| A3 | 0.20 REF. | | | 0.008 REF. | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 6.00 bsc | | | 0.236 bsc | | |
| D1 | 5.75 bsc | | | 0.226 bsc | | |
| D2 | 3.95 | 4.10 | 4.25 | 0.156 | 0.161 | 0.167 |
| E | 6.00 bsc | | | 0.236 bsc | | |
| E1 | 5.75 bsc | | | 0.226 bsc | | |
| E2 | 3.95 | 4.10 | 4.25 | 0.156 | 0.161 | 0.167 |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| e | 0.40 bsc | | | 0.016 bsc | | |
| θ1 | 0° | --- | 14° | 0° | --- | 14° |
| R | 0.075 | --- | --- | 0.003 | --- | --- |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | --- | --- | 0.10 | --- | --- | 0.004 |
| bbb | --- | --- | 0.07 | --- | --- | 0.003 |
| ccc | --- | --- | 0.10 | --- | --- | 0.004 |
| ddd | --- | --- | 0.05 | --- | --- | 0.002 |
| eee | --- | --- | 0.08 | --- | --- | 0.003 |
| fff | --- | --- | 0.10 | --- | --- | 0.004 |



NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. −1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.20 AND 0.25 mm FROM TERMINALTIP.
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
PAD FROM MEASURING.
9.APPLIED ONLY TO TERMINALS.
10.PACKAGE CORNERS UNLESS
OTHERWISE SPECIPIED
ARE R0.175±0.025 mm.

**Figure 6: Mechanical Specification – QFN 48**

# 11. Top Marking Information


1. asmedia: ASMedia Logo
2. ASM235CM: Product Name
3. YYWW: Date Code
4. X: Version of Marking Rule
5. XXXXXXX: Serial No. reserved for vendor
6. XX: Version code