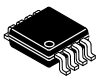
ASM3P1819N

Product Preview

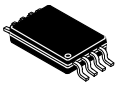
Low Power Mobile VGA EMI Reduction IC

ON Semiconductor®

http://onsemi.com

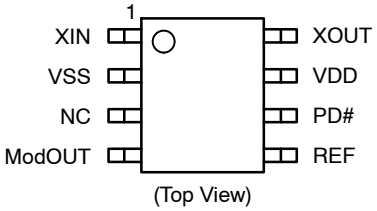


SOIC−8
S SUFFIX
CASE 751BD



TSSOP−8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Description

The ASM3P1819N is a versatile spread spectrum frequency modulator designed specifically for a wide range of input clock frequencies from 20 to 40 MHz. The ASM3P1819N can generate an EMI reduced clock from crystal, ceramic resonator, or system clock.

The ASM3P1819N reduces electromagnetic interference (EMI) at the clock source, allowing a system wide EMI reduction for all the down stream clocks and data dependent signals. The ASM3P1819N allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The ASM3P1819N modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, thereby decreasing the peak amplitude of its harmonics. This results in a significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators.

Lowering EMI by increasing a signal's bandwidth is called "spread spectrum clock generation". The ASM3P1819N uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

Applications

The ASM3P1819N is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high−speed digital applications such as PC peripheral devices, consumer electronics and embedded controller system.

Features

- FCC Approved Method of EMI Attenuation
- Provides up to 15 dB EMI Reduction
- Generates a Low EMI Spread Spectrum Clock and a Non−spread Reference Clock of the Input Frequency
- Optimized for Frequency Range from 20 MHz to 40 MHz
- Internal Loop Filter Minimizes External Components and Board Space
- Down Spread Deviation: −1.25%
- Low Inherent Cycle−to−Cycle Jitter
- 3.3 V Operating Voltage
- CMOS/TTL Compatible Inputs and Outputs
- Low Power CMOS Design
- Supports Notebook VGA and Other LCD Timing Controller Applications
- Power Down Function for Mobile Application
- Products are Available for Industrial Temperature Range
- Available in 8 pin SOIC and TSSOP Packages
- These are Pb−Free Devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

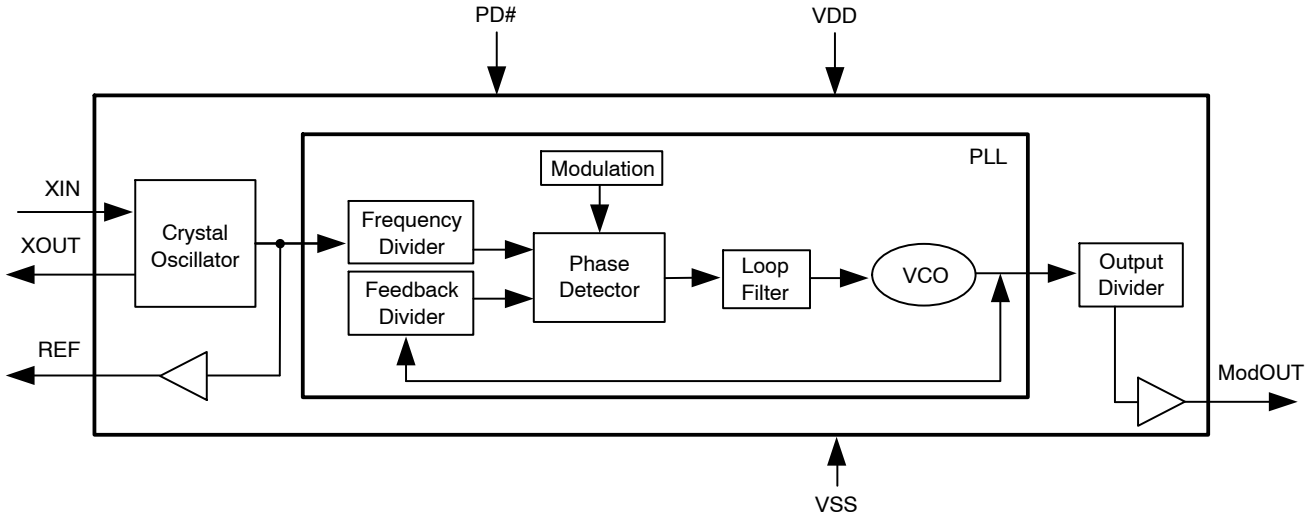


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	XIN	I	Connect to externally generated Clock signal or Crystal.
2	VSS	P	Ground Connection. Connect to system ground.
3	NC	–	No Connect.
4	ModOUT	O	Spread spectrum clock output.
5	REF	O	Non−modulated Reference clock output of the input frequency.
6	PD#	I	Power down control pin. Pull LOW to enable Power−Down mode. This pin has an internal pull−up resistor.
7	VDD	P	Connect to +3.3 V.
8	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	−40 to +85	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OUTPUT FREQUENCY AND MODULATION RATE

Input Frequency Range (MHz)	Output Frequency Range (MHz)	Modulation Rate	Spread Deviation (%)
20 to 40	20 to 40	Input Frequency / 512	−1.25

Table 4. DC ELECTRICAL CHARACTERISTICS
(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated.)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low voltage	VSS − 0.3		0.8	V
V_{IH}	Input High voltage	2.0		VDD + 0.3	V
I_{IL}	Input Low current			−20.0	μA
I_{IH}	Input High current			1.0	μA
I_{XOL}	X_{OUT} Output low current @ 0.4 V, VDD = 3.3 V		3		mA
I_{XOH}	X_{OUT} Output high current @ 2.5 V, VDD = 3.3 V		3		mA
V_{OL}	Output Low voltage VDD = 3.3 V, I_{OL} = 20 mA			0.4	V
V_{OH}	Output High voltage VDD = 3.3 V, I_{OH} = 20 mA	2.5			V
I_{CC}	Dynamic Supply current 3.3 V and 10 pF probe loading	7.1 $f_{IN\ -\ min}$		26.9 $f_{IN\ -\ max}$	mA
I_{DD}	Static Supply current		4.5		mA
VDD	Operating Voltage		3.3		V
t_{ON}	Power up time (First locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock Output impedance		50		Ω

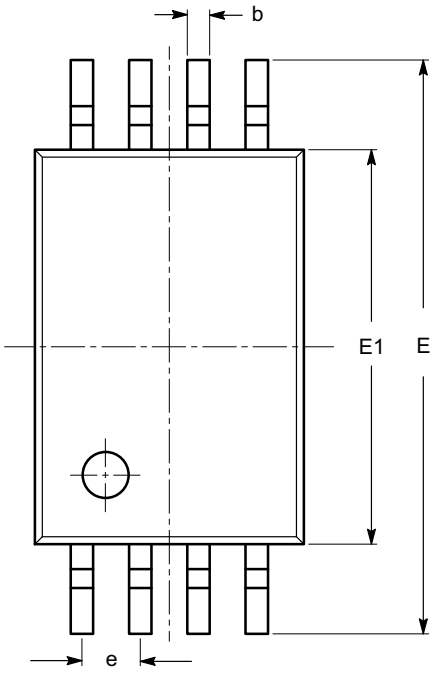
Table 5. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency	20		40	MHz
f_{OUT}	Output Frequency	20		40	MHz
t_{LH} (Note 1)	Output Rise time (Measured from 0.8 V to 2.0 V)		0.69		nS
t_{HL} (Note 1)	Output Fall time (Measured from 2.0 V to 0.8 V)		0.66		nS
t_{JC}	Jitter (Cycle to Cycle)	−200		200	pS
t_D	Output Duty cycle	45	50	55	%

1. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

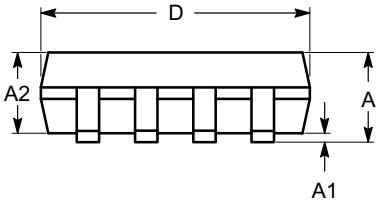
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

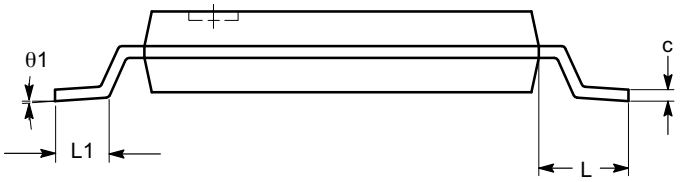


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



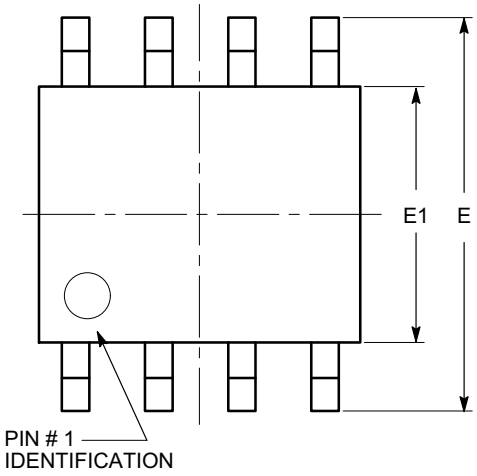
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

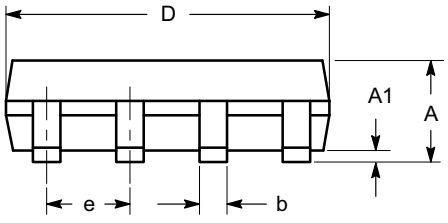
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

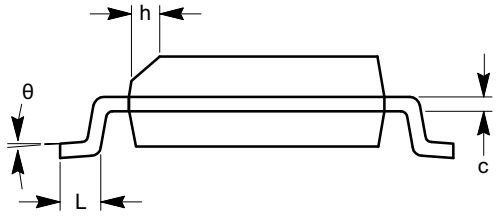


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 6. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM3P1819NF−08−ST	3P1819NF	8−Pin SOIC, Tube, Pb Free	Commercial
ASM3P1819NF−08−SR	3P1819NF	8−Pin SOIC, Tape and Reel, Pb Free	Commercial
ASM3P1819NG−08−ST	3P1819NG	8−Pin SOIC, Tube, Green	Commercial
ASM3P1819NG−08−SR	3P1819NG	8−Pin SOIC, Tape and Reel, Green	Commercial
ASM3I1819NF−08−ST	3I1819NF	8−Pin SOIC, Tube, Pb Free	Industrial
ASM3I1819NF−08−SR	3I1819NF	8−Pin SOIC, Tape and Reel, Pb Free	Industrial
ASM3I1819NG−08−ST	3I1819NG	8−Pin SOIC, Tube, Green	Industrial
ASM3I1819NG−08−SR	3I1819NG	8−Pin SOIC, Tape and Reel, Green	Industrial
ASM3P1819NF−08−TT	3P1819NF	8−Pin TSSOP, Tube, Pb Free	Commercial
ASM3P1819NF−08−TR	3P1819NF	8−Pin TSSOP, Tape and Reel, Pb Free	Commercial
ASM3P1819NG−08−TT	3P1819NG	8−Pin TSSOP, Tube, Green	Commercial
ASM3P1819NG−08−TR	3P1819NG	8−Pin TSSOP, Tape and Reel, Green	Commercial
ASM3I1819NF−08−TT	3I1819NF	8−Pin TSSOP, Tube, Pb Free	Industrial
ASM3I1819NF−08−TR	3I1819NF	8−Pin TSSOP, Tape and Reel, Pb Free	Industrial
ASM3I1819NG−08−TT	3I1819NG	8−Pin TSSOP, Tube, Green	Industrial
ASM3I1819NG−08−TR	3I1819NG	8−Pin TSSOP, Tape and Reel, Green	Industrial

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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ASM3P1819N/D