

ASM3P2182A

Product Preview

LCD Panel EMI Reduction IC

Description

The ASM3P2182A is a versatile spread spectrum frequency modulator designed specifically for a wide range of input clock frequencies from 25 MHz to 210 MHz. (Refer to *Input Frequency and Modulation Rate Table*). The ASM3P2182A can generate an EMI reduced clock from an OSC or a system generated clock. The ASM3P2182A offers a Center Spread clock and with a percentage deviation from $\pm 0.13\%$ or $\pm 1.24\%$.

The ASM3P2182A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The ASM3P2182A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The ASM3P2182A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The ASM3P2182A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

Applications

The ASM3P2182A is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high-speed digital applications such as PC peripheral devices, consumer electronics, and embedded controller systems.

Features

- FCC Approved Method of EMI Attenuation
- Provides up to 15 dB EMI Reduction
- Generates a 1X Low EMI Spread Spectrum Clock of the Input Frequency
- Input Frequency Range: 25 MHz to 210 MHz
- Internal Loop Filter Minimizes External Components and Board Space
- Center Spread
- 4 Spread Frequency Deviation Selections: $\pm 0.13\%$ to $\pm 1.24\%$
- Low Inherent Cycle-to-Cycle Jitter
- 3.3 V Operating Voltage
- TTL or CMOS Compatible Inputs and Outputs
- Low Power CMOS Design
- Supports Notebook VGA and Other LCD Timing Controller Applications
- Products are Available for Industrial Temperature Range
- Available in 8-pin SOIC and TSSOP Packages
- These are Pb-Free Devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



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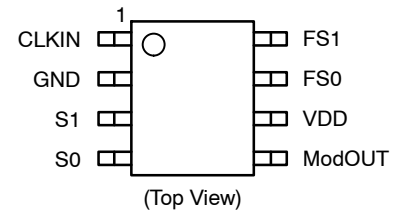


SOIC-8
S SUFFIX
CASE 751BD



TSSOP-8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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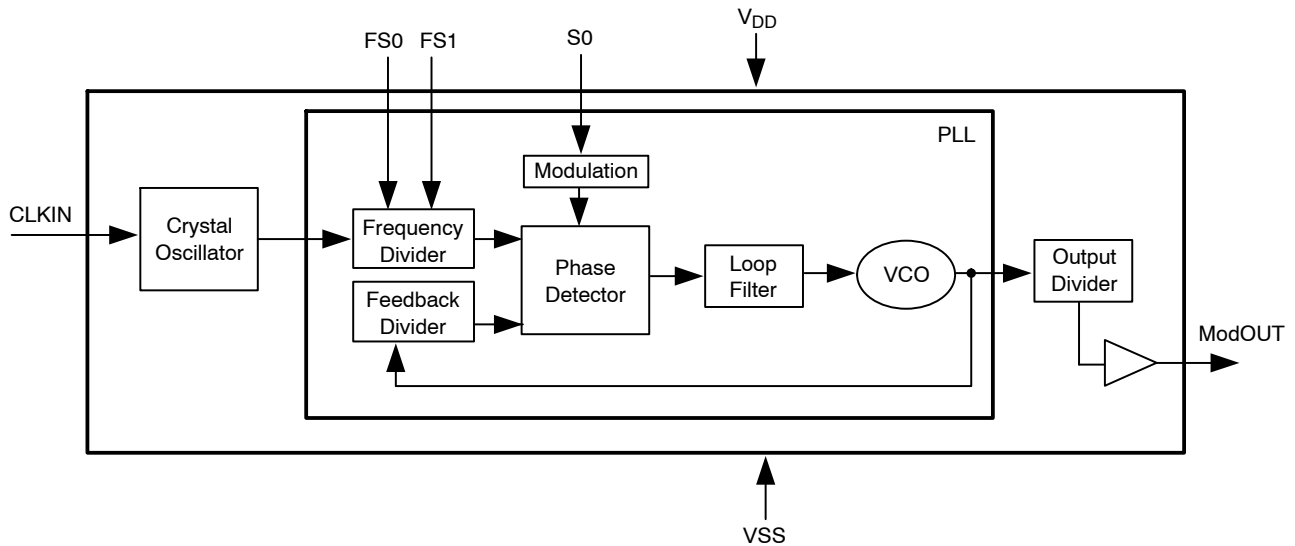


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLKIN	I	Connect to externally generated clock signal.
2	GND	P	Ground to entire chip.
3	S1	I	Spread range select. Digital logic input used to select frequency deviation (Refer to <i>Spread Deviation Table</i>). This pin has an internal pull-up resistor.
4	S0	I	Spread range select. Digital logic input used to select frequency deviation (Refer to <i>Spread Deviation Table</i>). This pin has an internal pull-up resistor.
5	ModOUT	O	Spread spectrum low EMI output.
6	VDD	P	Power supply for the entire chip (3.3 V).
7	FS0	I	Frequency range select. Digital logic input used to select frequency range (Refer to <i>Input Frequency and Modulation Rate Table</i>). This pin has an internal pull-up resistor.
8	FS1	I	Frequency range select. Digital logic input used to select frequency range (Refer to <i>Input Frequency and Modulation Rate Table</i>). This pin has an internal pull-up resistor.

Table 2. INPUT FREQUENCY AND MODULATION RATE TABLE

FS1 (pin 8)	FS0 (pin 7)	Frequency Range
0	0	25 MHz to 50 MHz
0	1	50 MHz to 103 MHz
1	0	75 MHz to 150 MHz
1	1	160 MHz to 210 MHz

Table 3. SPREAD DEVIATION SELECTION TABLE

S1	S0	Spreading Range (±%)								
		25 MHz	40 MHz	65 MHz	81 MHz (Note 1)	81 MHz (Note 2)	108 MHz	120 MHz	162 MHz	200 MHz
0	0	0.28	0.19	0.15	0.12	0.18	0.15	0.1	0.1	0.06
0	1	0.8	0.3	0.3	0.2	0.5	0.3	0.19	0.3	0.1
1	0	1.2	0.54	0.45	0.4	0.8	0.6	0.36	1.0	0.6
1	1	2.1	1.0	1.1	0.9	1.4	1.1	0.75	1.9	1.2

1. Frequency Range: 50 MHz to 103 MHz
2. Frequency Range: 75 MHz to 150 MHz

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Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage pin with respect to Ground	-0.5 to +4.6	V
V _{IN}	Input Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V
V _{OUT}	Output Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V
T _{STG}	Storage temperature	-55 to +125	°C
T _s	Max. Soldering Temperature (10 sec)	260	°C
T _J	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22-A114-B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Min	Typ	Max	Unit
VDD	Operating Voltage	2.7	3.3	3.7	V
T _A	Operating Temperature (Ambient Temperature)	0		+70	°C
C _L	Load Capacitance			15	pF
C _{IN}	Input Capacitance		5		pF

Table 6. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V _{IL}	Input low voltage	GND - 0.3		0.8	V
V _{IH}	Input high voltage	2.0		V _{DD} + 0.3	V
I _{IL}	Input low current			-35	μA
I _{IH}	Input high current			35	μA
V _{OL}	Output low voltage (V _{DD} = 3.3 V, I _{OL} = 20 mA)			0.4	V
V _{OH}	Output high voltage (V _{DD} = 3.3 V, I _{OH} = 20 mA)	2.5			V
I _{CC}	Dynamic supply current Normal mode (3.3 V and 10 pF loading)	8.46	12	17.78	mA
I _{DD}	Static supply current Standby mode (Note 3)		0.6		mA
V _{DD}	Operating voltage	2.7	3.3	3.7	V
t _{ON}	Power up time (first locked clock cycle after power up)		0.18		mS
Z _{OUT}	Clock out impedance		50		Ω

3. CLKIN pin is pulled low.

Table 7. AC ELECTRICAL CHARACTERISTICS

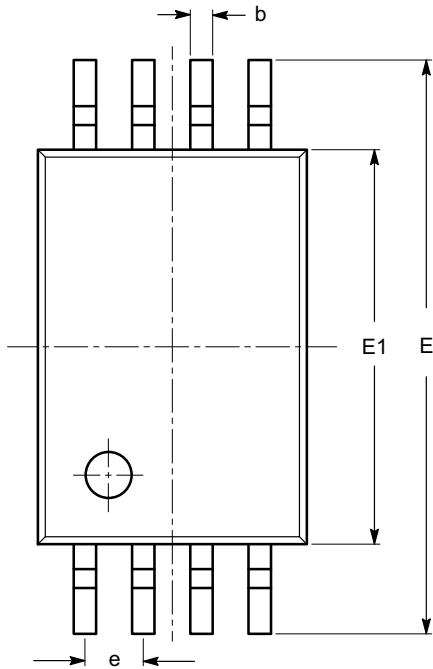
Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	25		210	MHz
ModOUT	Output frequency	25		210	MHz
t _{LH} (Note 4)	Output rise time (measured at 0.8 V to 2.0 V)	1.2	1.32	1.4	nS
t _{HL} (Note 4)	Output fall time (measured at 2.0 V to 0.8 V)	0.8	0.9	1.0	nS
t _{JC}	Jitter (cycle to cycle)			360	pS
T _D	Output duty cycle	45	50	55	%

4. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

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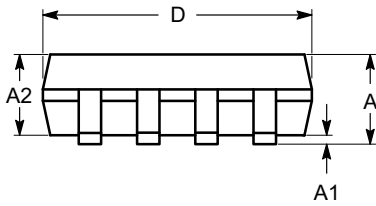
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL-01
ISSUE O

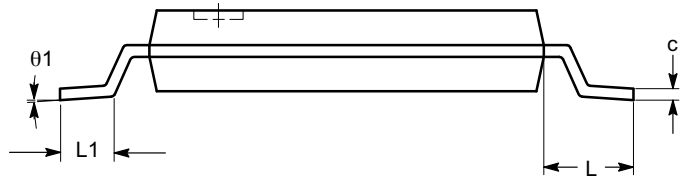


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

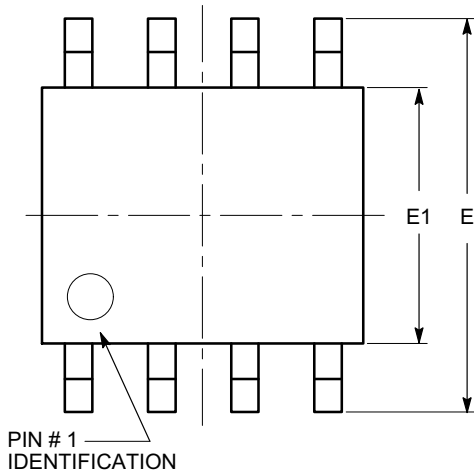
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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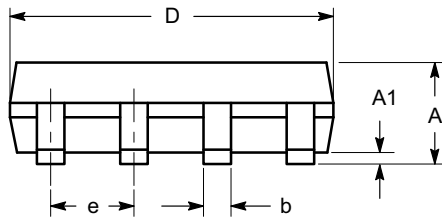
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD-01
ISSUE O

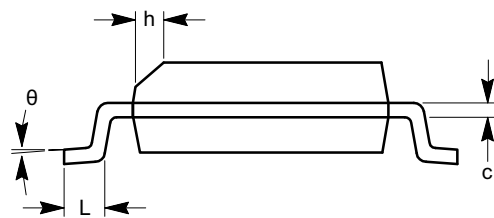


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW


Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM3P2182AF-08TT	3P2182AF	8-Pin TSSOP, TUBE, Pb Free	Commercial
ASM3P2182AF-08TR	3P2182AF	8-Pin TSSOP, TAPE & REEL, Pb Free	Commercial
ASM3P2182AF-08ST	3P2182AF	8-Pin SOIC, TUBE, Pb Free	Commercial
ASM3P2182AF-08SR	3P2182AF	8-Pin SOIC, TAPE & REEL, Pb Free	Commercial
ASM3P2182A-08TT	3P2182A	8-Pin TSSOP, TUBE	Commercial
ASM3P2182A-08TR	3P2182A	8-Pin TSSOP, TAPE & REEL	Commercial
ASM3P2182A-08ST	3P2182A	8-Pin SOIC, TUBE	Commercial
ASM3P2182A-08SR	3P2182A	8-Pin SOIC, TAPE & REEL	Commercial
ASM3P2182AG-08TT	3P2182AG	8-Pin TSSOP, TUBE, Green	Commercial
ASM3P2182AG-08TR	3P2182AG	8-Pin TSSOP, TAPE & REEL, Green	Commercial
ASM3P2182AG-08ST	3P2182AG	8-Pin SOIC, TUBE, Green	Commercial
ASM3P2182AG-08SR	3P2182AG	8-Pin SOIC, TAPE & REEL, Green	Commercial

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