



EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15dB EMI reduction.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input frequency range: 25MHz to 50 MHz.
- Internal loop filter minimizes external components and board space.
- Down Spread and Center Spread.
- 2 spread frequency deviation selections: -1.25% and $\pm 0.6\%$.
- Low inherent cycle-to-cycle jitter.
- 3.3V operating voltage range.
- TTL or CMOS compatible inputs and outputs.
- Low power CMOS design.
- Supports notebook VGA and other LCD timing controller applications.
- Products are available for industrial temperature range.
- Available in 8-pin SOIC and TSSOP.

Product Description

The ASM3P2185A is a versatile spread spectrum frequency modulator designed specifically for a wide range of input clock frequencies from 25MHz to 50MHz. The ASM3P2185A can generate an EMI reduced clock from an OSC or a system generated clock.

The ASM3P2185A reduces electromagnetic interference (EMI) at the clock source, allowing system wide EMI reduction for all the down stream clocks and data dependent signals. The ASM3P2185A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

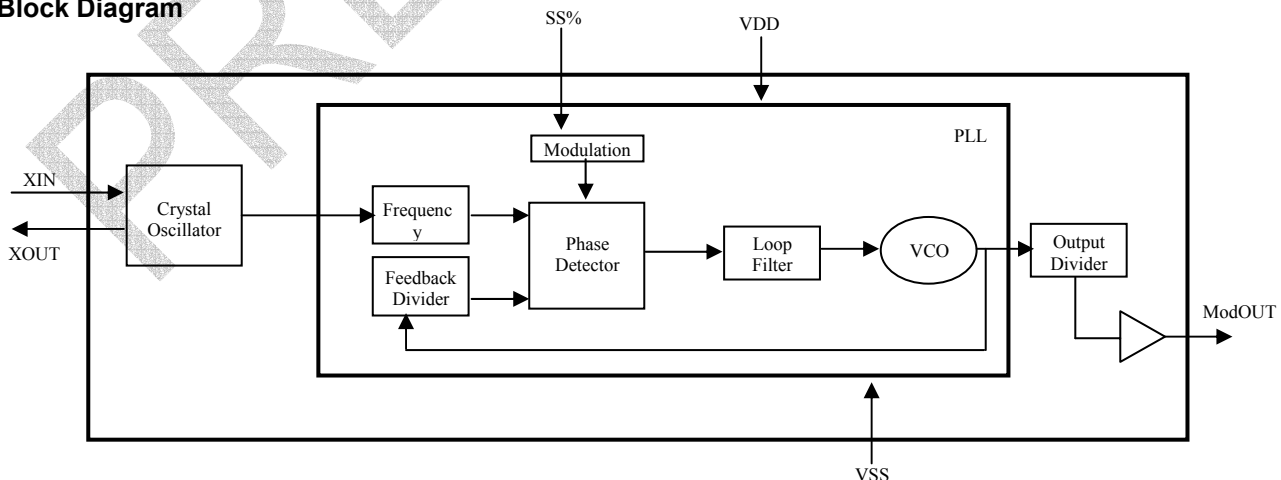
The ASM3P2185A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The ASM3P2185A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

Applications

The ASM3P2185A is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high-speed digital applications such as PC peripheral devices, consumer electronics, and embedded controller systems.

Block Diagram

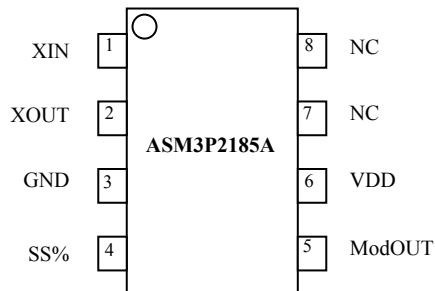




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Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected to either an external crystal or an external reference clock.
2	XOUT	I	Crystal connection. Input connection for an external crystal. If using an external reference, this pin must be left unconnected.
3	GND	P	Ground to entire chip.
4	SS%	I	Spread range select. Digital logic input used to select frequency deviation (Refer <i>Spread Deviation Table</i>). This pin has an internal pull-up resistor.
5	ModOUT	O	Spread spectrum low EMI output.
6	VDD	P	Power supply for the entire chip (3.3V).
7	NC		No Connect.
8	NC		No Connect.

Spread Deviation Selection Table

SS% (pin 4)	Spread Deviation (%)
0	- 1.25
1	± 0.6%



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to 70	°C

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND - 0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	$V_{DD} + 0.3$	V
I_{IL}	Input low current	-	-	-35	μA
I_{IH}	Input high current	-	-	35	μA
I_{XOL}	XOUT Output low current (@ 0.4V, $V_{DD} = 3.3V$)	-	TBD	-	mA
I_{XOH}	XOUT Output high current (@ 2.5V, $V_{DD} = 3.3V$)	-	TBD	-	mA
V_{OL}	Output low voltage ($V_{DD} = 3.3V, I_{OL} = 20mA$)	-	-	0.4	V
V_{OH}	Output high voltage ($V_{DD} = 3.3V, I_{OH} = 20mA$)	2.5	-	-	V
I_{CC}	Dynamic supply current Normal mode (3.3V and 10pF loading)	8.46	12	17.78	mA
I_{DD}	Static supply current Standby mode		0.6		mA
V_{DD}	Operating voltage	2.7	3.3	3.7	V
t_{ON}	Power up time (first locked clock cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock out impedance	-	50	-	Ω



AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
XIN	Input frequency	25	-	50	MHz
ModOUT	Output frequency	25	-	50	MHz
t_{LH}^*	Output rise time (measured at 0.8V to 2.0V)	1.2	1.32	1.4	ns
t_{HL}^*	Output fall time (measured at 2.0V to 0.8V)	0.8	0.9	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
T_D	Output duty cycle	45	50	55	%
t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

PRELIMINARY

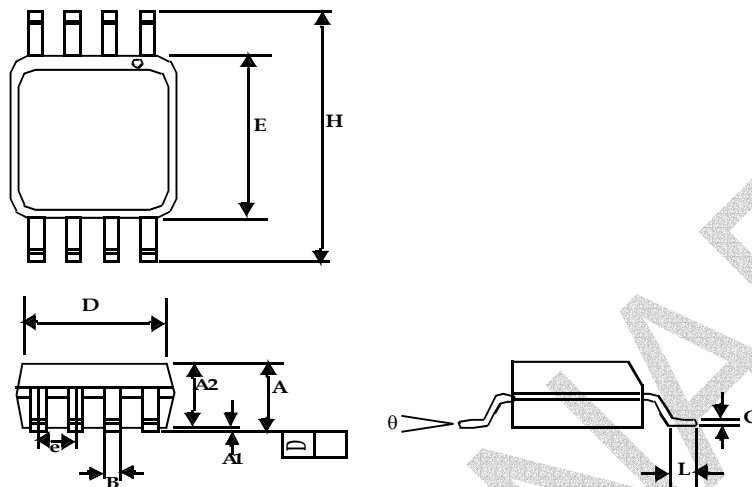


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Package Information

8-Pin SOIC



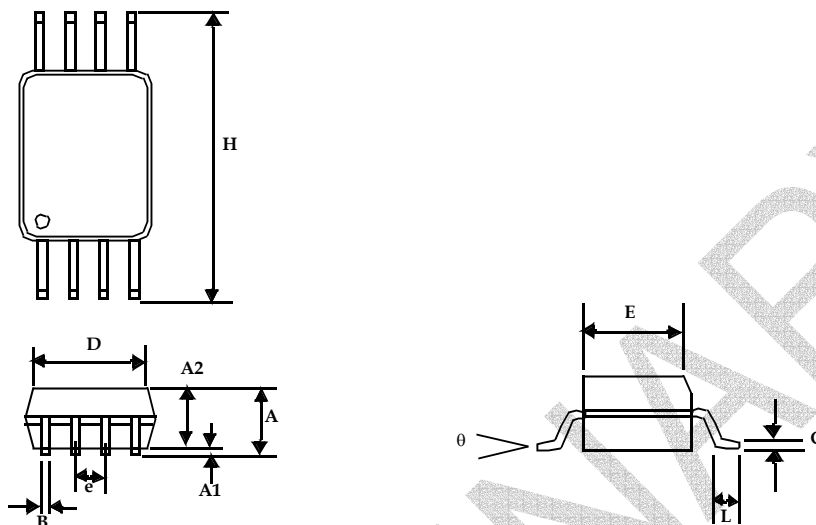
Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.057	0.071	1.45	1.80
A1	0.004	0.010	0.10	0.25
A2	0.053	0.069	1.35	1.75
B	0.012	0.020	0.31	0.51
C	0.004	0.01	0.10	0.25
D	0.186	0.202	4.72	5.12
E	0.148	0.164	3.75	4.15
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.70	6.30
L	0.012	0.028	0.30	0.70
□	0°	8°	0°	8°



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8-Pin TSSOP



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.047			1.10
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.244	0.260	6.20	6.60
L	0.018	0.030	0.45	0.75
θ	0°	8°	0°	8°

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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