ASM3P2855D

ON Semiconductor®

Custom Clock Generator for FAX System

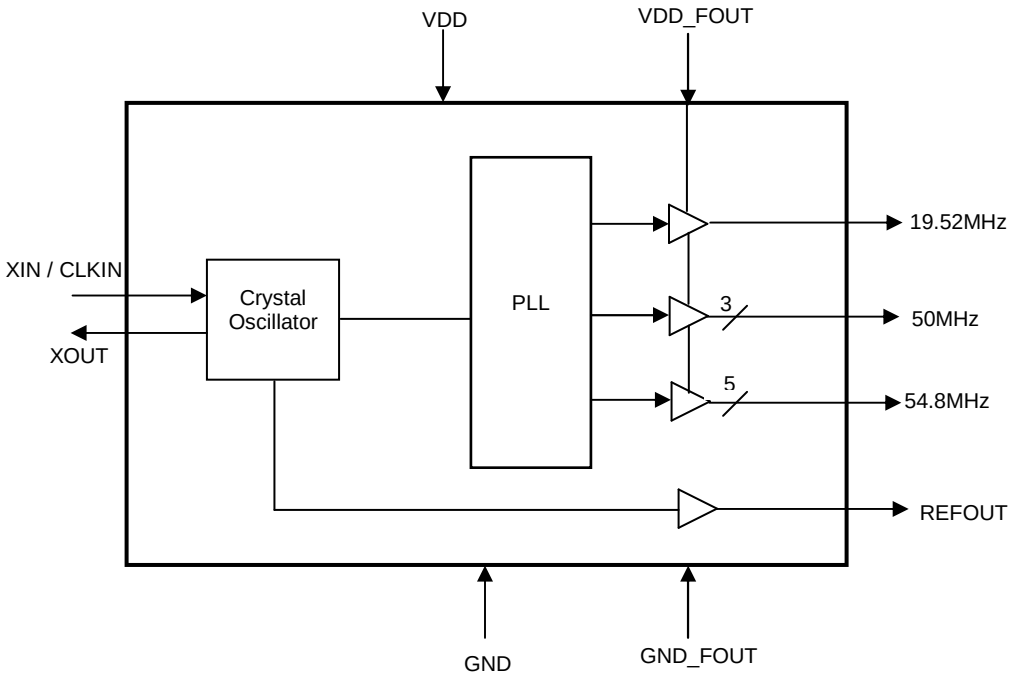
Features

- Generates Custom Clocks for FAX system from an inexpensive 24MHz Crystal
- 3 x 50MHz synchronized clocks
- 5 x 54.8MHz synchronized clocks
- 1 x 19.52MHz clock for Scanner
- REFOUT Clock
- Supply Voltage 3.3 V ± 0.3V
- Available in 16L TSSOP, Green package

Product Description

ASM3P2855D is a custom clock generator for FAX system. ASM3P2855D realizes all the ten clocks required by the various components and subsystems of the FAX system. It uses an inexpensive 24MHz crystal as the input to generate five synchronized 54.8MHz clocks and three synchronized 50MHz PCI clocks that can be used by CPU, HDD, PCI Analyzer, ASIC2 and ASIC3, Ethernet, LAN PHY and for the CPU Timer, a 19.52MHz clock used by ASIC1 for Scanner. The custom clock generator ASM3P2855D works with a Supply Voltage of 3.3V ± 0.3V. The device is available in a 16L TSSOP Green package.

Block Diagram



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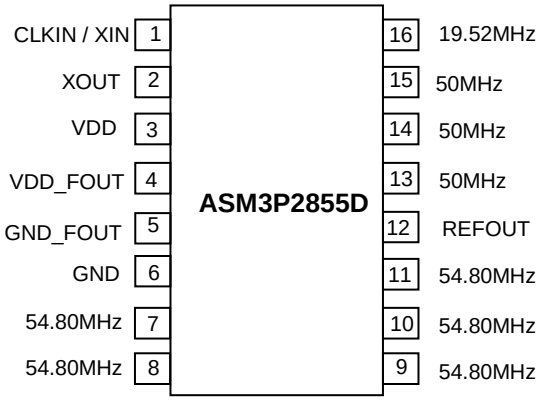
Pin Diagram



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or external reference Clock input.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	VDD	P	Power supply for the core
4	VDD_FOUT	P	Power supply for the output buffers.
5	GND_FOUT	P	Ground connection for the output buffers
6	GND	P	Ground connection
7	54.80MHz	O	Synchronous 54.80MHz Clock Output
8	54.80MHz	O	Synchronous 54.80MHz Clock Output
9	54.80MHz	O	Synchronous 54.80MHz Clock Output
10	54.80MHz	O	Synchronous 54.80MHz Clock Output
11	54.80MHz	O	Synchronous 54.80MHz Clock Output
12	REFOUT	O	24MHz Reference Clock Output
13	50MHz	O	Synchronous 50MHz Clock Output
14	50MHz	O	Synchronous 50MHz Clock Output
15	50MHz	O	Synchronous 50MHz Clock Output
16	19.52MHz	O	19.52MHz Clock Output

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, VDD_FOUT	Power Supply Voltage relative to GND	-0.5 to +4.6	V
V_{IN}	Input Voltage relative to GND (Input Pins)	-0.5 to VDD+0.5	
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
T_A	Operating Temperature	0		+70	℃
VDD	Output Core Voltage	+3.0	+3.3	+3.6	V
VDD_FOUT	Output Buffer Voltage	+3.0	+3.3	+3.6	V

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND-0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD+0.3	V
I_{IL}	Input low current			-35	µA
I_{IH}	Input high current			35	µA
I_{XOL}	XOUT output low current (V_{XOL} @ 0.4V, VDD = 3.3V)		3		mA
I_{XOH}	XOUT output high current (V_{XOH} @ 2.5V, VDD = 3.3V)		3		mA
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 10mA)			0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OH} = -10mA)	2.5			V
I_{DD}	Static supply current[1]			12	mA
I_{CC}	Dynamic supply current (VDD = 3.3V,Unloaded Outputs)		32		mA
VDD	Operating Core Voltage	3.0	3.3	3.6	V
VDD_FOUT	Operating Buffer Voltage	3.0	3.3	3.6	V
t_{ON}	Power-up time (first locked cycle after power-up)[2]			5	mS
Z_O	Output impedance		30		Ω

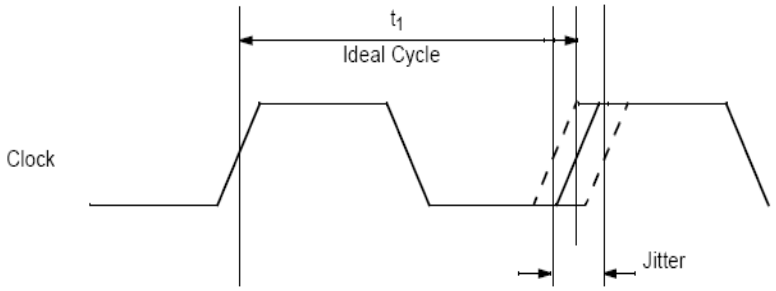
Notes: 1. CLKIN / XIN is pulled to GND.
2. VDD and CLKIN inputs are stable.

AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
XIN / CLKIN	Input frequency			24		MHz
F_{OUT}	Output frequency	At Pin 12		24		MHz
		At Pins 7,8,9,10,11		54.80		
		At Pins 13,14,15		50		
		At Pin 16		19.52		
t_{LH}[1]	Output rise time (measured from 20% to 80%)			1.0		nS
t_{HL}[1]	Output fall time (measured from 80% to 20%)			1.0		nS
t_D	Output duty cycle		45	50	55	%
t_{JP}	Period Jitter (Unloaded Outputs)				±275	pS

Note: 1. t_{LH} and t_{HL} are measured into a capacitive load of 15pF.

Period Jitter

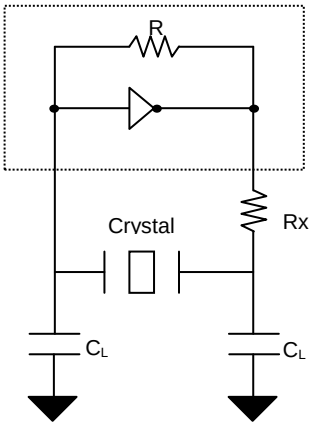


Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	24MHz
Frequency tolerance	± 50 ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance(C_P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

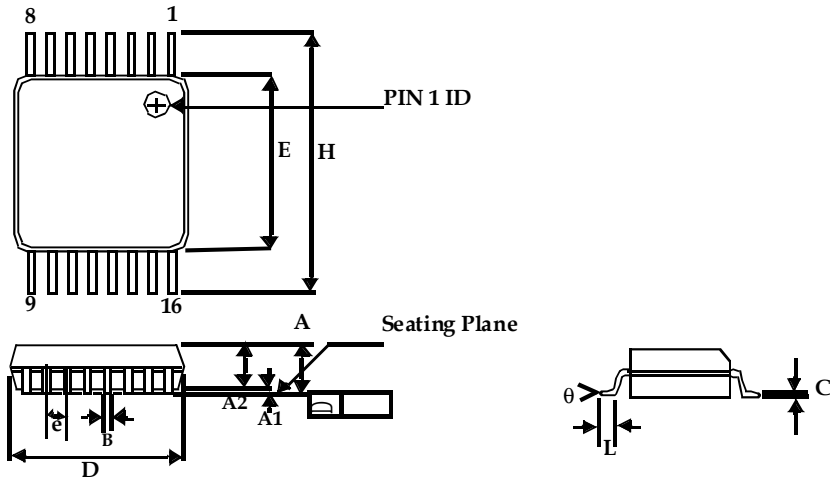
Typical Crystal Interface Circuit



$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace etc.

Package Information

16-lead Thin Shrunk Small Outline Package (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
θ	0°	8°	0°	8°

Ordering Code

Ordering Code	Marking	Package Type	Operating Range
ASM3P2855DG-16TR	3P28 55D	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	0℃ to +7 0℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

PUBLICATION ORDERING INFORMATION

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