DDR 14-Bit Registered Buffer

Features

Fully JEDEC JC40 - JC42.5 compliant for DDR1 applications to include: PC1600, PC2100, PC2700 & PC3200 (> JEDEC defined DDR 400 @ 200MHz)

Low voltage operation; VDD: 2.3V - 2.7V.

- SSTL 2 Class II outputs.
- Differential clock inputs.
- Available in 48 pin TSSOP and TVSOP packages.

Product Description

The ASM4SSTVF16857 is a universal 14-bit register (D F/F based), designed for 2.3V to 2.7V V_{DD} . The device supports SSTL_2 I/O levels, and is fully compliant with the JEDEC JC40, JC42.5 DDR I specifications covering PC1600, PC2100, PC2700, and PC3200 operational ranges. 14-bit refers to 2Q outputs for each D input - designed for use in Stacked Registers (stacked memory devices), Buffered DIMM applications.

Data flow from D to Q is controlled by the differential clock (CLK/CLKB) along with a controlled reset (RESETB). The positive edge of CLK is used to trigger the data transfer, and CLKB is used to maintain sufficient noise margins, whereas the RESETB input is designed and intended for use at power-up.

The ASM4SSTVF16857 supports a low power standby mode of operation. A logic low level at RESETB, assures that all internal registers and outputs (Q) are reset to a logic low state, and that all input receivers, data (D) buffers, and clock (CLK/CLKB) are switched off. Note that RESETB should be supported with a

LVCMOS level at a valid logic state since VREF may not be stable during power-up.

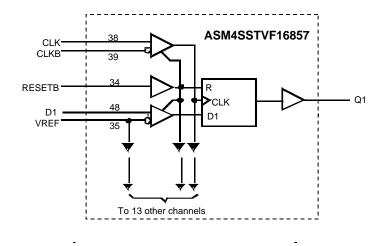
To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESETB must be held at a logic low level during power-up.

In the JEDEC defined Registered DDR DIMM application, RESETB is specified to be asynchronous with respect to CLK/CLKB; therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby mode, the register will be cleared and the outputs will be driven to a logic low level quickly relative to the time to disable the differential input receivers. This ensures there are no "glitches" on any output. However, when coming out of low power standby mode, the register will become active quickly relative to the time taken to enable the differential input receivers. When the data inputs are at a logic level low and the clock is stable during the lowto-high transition of RESETB until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic low level.

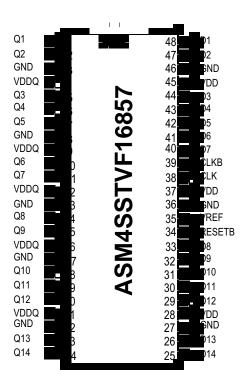
Applications

- JEDEC and Non JEDEC DDR Memory Modules Planar configurations
 - •Supports PC1600 PC2100 PC2700 PC3200
- SSTL 2I/O
- Provides a complete support solution for JEDEC JC42.5 (JC45) DDR I RDIMMs' when used with the ASM5CVF857 Zero Delay Buffer.

Block Diagram



Pin Configurations



48-pin TSSOP & TVSOP 6.10 mm body, 0.50 mm pitch - TSSOP 4.40mm body, 0.40mm pitch - TSSOP (TVSOP)

Pin Descriptions

Pin #	Pin Name	Туре	Description
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q (14:1)	0	Data output.
3, 8, 13, 17, 22, 27, 36, 46	GND	Р	Ground to entire chip.
com 4, 9, 12, 16, 21	VDDQ	Р	Output supply voltage.
25, 26, 29, 30, 31, 32, 33, 40, 41, 42, 43, 44, 47, 48	D(14:1)	I	Data input.
38	CLK	I	Positive clock input.
39	CLKB	-	Negative clock input.
28, 37, 45	VDD	Р	Core supply voltage.
34	RESETB	I	Rest Active low.
35	VREF	ı	Input reference voltage.

Truth Table¹

	Inputs						
RESETB	CLK	CLKB	D	Q			
L	X or floating	X or floating	X or floating	L			
Н			н	н			
Н			L	L			
Н	L or H	L or H	X	Q_0^2			

^{1.} H=High signal level, L=Low signal level, = transition from low to high, = transition from high to low, X = don't care 2. Output level before the indicated steady state input conditions were established.



Parameter	Min	Max	Unit
Storage Temperature	-65	+150	°C
Supply Voltage	-0.5	3.6	V
Input Voltage ¹	-0.5	V _{DD} + 0.5	V
Output Voltage ^{1,2}	-0.5	V _{DD} + 0.5	V
Input Clamp Current	±	mA	
Output Clamp Current	±	50	mA
Continuous Output Current	±50		mA
VDD, VDDQ or GND current/pin	10	00	mA
Package Thermal Impedance ³	5	5	°C/W

- 1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
- 2. This current will flow only when the output is in the high state level $V_0 > V_{DDQ}$. 3. The package thermal impedance is calculated in accordance with JESD 51.

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.



Recommended Operating Conditions

Guaranteed by design. Not 100% tested in production.

Parameter	Description		Min	Тур	Max	Unit
V_{DD}	Supply voltage		2.3	2.5	2.7	V
_{som} V _{DDQ}	Output supply voltage	PC1600, PC2100, PC2700	2.3		2.7	٧
		PC3200	2.5		2.7	
V_{REF}	Reference voltage (V _{REF} = V _{DDQ} /2)	PC1600, PC2100, PC2700	1.15	1.25	1.35	٧
		PC3200	1.25	1.3	1.35	
V _{TT}	Termination voltage		V _{REF} - 0.04	V_{REF}	V _{REF} + 0.004	V
Vı	Input voltage		0		V_{DD}	V
V _{IH(DC)}	DC input high voltage		V _{REF} + 0.15			V
V _{IH(AC)}	AC input high voltage	Data	V _{REF} + 0.31			V
V _{IL(DC)}	DC input low voltage	Inputs			V _{REF} - 0.15	V
V _{IL(AC)}	AC input low voltage				V _{REF} - 0.31	V
ViH	Input high voltage level	RESETB	1.7			V
V _{IL}	Input low voltage level	RESETS			0.7	V
V _{ICR}	Common mode input range	CLK	0.97		1.53	V
V _{ID}	Differential input voltage	CLKB	0.36			V
V _{IX}	Cross-point voltage of differential clock pair		(V _{DDQ} /2) - 0.2		(V _{DDQ} /2) +0.2	V
I _{OH}	High-level output current				-20	mA
I _{OI}	Low-level output current				20	mA
T _A	Operating free-air temperature		0		70	°C



DC Electrical Characteristics - PC1600, PC2100, PC2700

 T_{A} = 0°C to 70°C, V_{DD} = 2.5 \pm 0.2V, and V_{DDQ} = 2.5 \pm 0.2V (unless otherwise stated)

Guaranteed by design. Not 100% production tested.

Symbol	Parameter	Test conditions		V _{DD}	Min	Тур	Max	Units
V _{IK}		I _I = -18 mA		2.3 V			-1.2	V
V _{он}		I _{OH} = -100 μA		2.3 V to 2.7 V	V _{DD} - 0.2			V
com		I _{OH} = -16 mA		2.3 V	1.95			V
V_{OL}		I _{OL} = 100 μA		2.3 V to 2.7 V			0.2	V
VOL		I _{OL} = 16 mA		2.3 V			0.35	V
I _I	All inputs	$V_{I} = V_{DD}$ or GND		2.7 V			± 5	μΑ
I _{DD}	Standby (static)	RESETB = GND		2.7 V			0.01	μΑ
IDD	Operating (static)	$V_{I} = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
	Dynamic operating (clock only)	$\begin{split} & \text{RESETB} = V_{\text{DD}}, \\ & V_{\text{I}} = V_{\text{IH}(\text{AC})} \text{ or } V_{\text{IL}(\text{AC})}, \\ & \text{CLK and CLKB switching} \\ & 50\% \text{ duty cycle} \end{split}$	I _O = 0	2.7 ∨		28		μΑ/clock MHz
I _{DDD}	Dynamic operating (per each data input)	$\begin{split} & \text{RESETB} = V_{\text{DD}}, V_{\text{I}} = V_{\text{IH(AC)}} \text{or} \\ & V_{\text{IL(AC)}}, \text{CLK} \text{and} \text{CLKB} = \\ & \text{switching 50% duty cycle;} \\ & \text{One data input switching at half} \\ & \text{clock frequency, 50% duty cycle} \end{split}$		2.7 ∨		15		μΑ/clock MHz/data input
r _{OH}	Output high	I _{OH} = -20 mA		2.3 V to 2.7 V	7	13.5	20	Ω
r_{OL}	Output low	I _{OL} = 20 mA		2.3 V to 2.7 V	7		20	Ω
r _{O(D)}	r _{OH} - r _{OL} each separate bit	I _O = 20 mA, T _A = 25° C		2.5 V			4	Ω
	Data inputs	$V_i = V_{REF} \pm 310 \text{ mV}, \ V_{ICR} = 1.25 \text{ V}$	·,	2.5 V	2.5		3.5	pF
C _i	CLK & CLKB	$V_{I(PP)} = 360 \text{ mV}$		2.5 V	2.5		3.5	pF
	RESETB	$V_i = V_{DD}$ or GND		2.5V	2.5		3.5	pF

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 $T_A = 0$ °C to 70°C, $V_{DD} = 2.6 \pm 0.2$ V, and $V_{DDQ} = 2.6 \pm 0.2$ V (unless otherwise stated) Guaranteed by design. Not 100% production tested.

Symbol	Parameters	Test condition	ns	V _{DD} (V)	Min	Тур	Max	Units
V _{IK}		I _I = -18 mA		2.5			-1.2	٧
V _{он}		I _{OH} = -100 μA		2.5 V to 2.7	V _{DD} - 0.2			٧
U.com ^{sh}		I _{OH} = -8 mA		2.5	1.95			٧
V _{OL}		I _{OL} = 100 μA		2.5 V to 2.7			0.2	V
VOL		I _{OL} = 8 mA		2.5			0.35	V
l _l	All inputs	$V_I = V_{DD}$ or GND		2.7			± 5	μΑ
I _{DD}	Standby (static)	RESETB = GND		2.7			0.01	μΑ
Julia	Operating (static)	$V_{I} = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7			25	mA
	Dynamic operating (clock only)	$\begin{aligned} & \text{RESETB} = V_{\text{DD}}, \\ & V_{\text{I}} = V_{\text{IH(AC)}} \text{ or } V_{\text{IL(AC)}}, \\ & \text{CLK and CLKB switching} \\ & 50\% \text{ duty cycle} \end{aligned}$	I _O = 0	2.7		328		μΑ/clock MHz
I _{DDD}	Dynamic operating (per each data input)	RESETB = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLKB = switching 50% duty cycle; One data input switching at half clock frequency, 50% duty cycle		2.7		15		μΑ/clock MHz/data input
r _{OH}	Output high	I _{OH} = -20 mA		2.5 V to 2.7	7	13.5	20	Ω
r _{OL}	Output low	I _{OL} = 20 mA		2.5 V to 2.7	7		20	Ω
r _{O(D)}	r _{OH} - r _{OL} each separate bit	I _O = 20 mA, T _A = 25° C		2.6			4	Ω
	Data inputs	$V_I = V_{REF} \pm 310 \text{ mV}, V_{ICR} =$	1.25 V,	2.6	2.5		3.5	pF
C _i	CLK & CLKB	V _{I(PP)} = 360 mV		2.6	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.6	2.5		3.5	pF

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Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted).

Guaranteed by design. Not 100% production tested.

* this parameter is not necessarily production tested.

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L.com Symbol	Parameters		V _{DDQ} = 2.	5V±0.2V	V _{DDQ} = 2.6V	/±0.1V	Unit
			Min	Max	Min	Max	
f _{CLOCK}	Clock frequency			200		270	MHz
t _W	Pulse duration, CK, CKLB h	igh or low	2.5		2.5		ns
t _{ACT} *	Differential inputs active tim		22		22	ns	
t _{INACT} *	Differential inputs inactive til	me		22		22	ns
ts	Setup time, fast slew rate	Data before CLK↑, CLKB↓	0.75		0.4		ns
15	Setup time, slow slew rate	Bata sciole CERT, CERBY	0.9		0.6		ns
t _h	Hold time, fast slew rate	Data after CLK↑, CLKB↓	0.75		0.4		ns
c _{ll}	Hold time, slow slew rate	Data and CERT, CERD	0.9		0.6		ns
t _{SL}	Output slew rate, measurem	nent point at 20% and 80%	1	4	1	4	V/ns

Noto:

- 1. Data inputs must be low for a minimum time of t_{ACT} max, after which RESETB is taken high.
- 2. Data and clock inputs must be held at valid levels (not floating) for a minimum time of tINACTmax after which RESETB is taken low.
- 3. For data signal input slew rate >= V/ns
- 4. For data signal input slew rate >=0.5 V/ns and < 1V/ns
- 5. CLK,CLKB signals input slew rates are >=1V/ns



Switching Characteristics - PC1600, PC2100, PC2700

(Over recommended operating free-air temperature range unless otherwise noted.)

Symbol	From (input)	To (output)	VDD = 2.5 V ± 0.2 V).2 V	Units
			Min	Тур	Max	
f _{max}			200	-	_	MHz
t _{PD}	CLK, CLKB	Q	1.1		2.8	ns
t _{phl}	RESETB	Q	_	_	5.0	ns

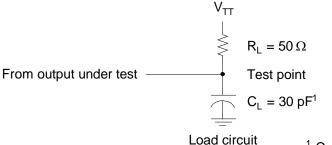
Switching Characteristics - PC3200

(Over recommended operating free-air temperature range unless otherwise noted.)

Symbol	From (input)	To (output)	VDD = 2.6 V ± 0.1 V		0.1 V	Units
		(33,13,	Min	Тур	Max	
f _{max}			280			MHz
t _{PD}	CLK, CLKB	Q	1.1		2.2	ns
t _{phl}	RESETB	Q			5.0	ns



Parameter Measurement Information ($V_{DD} = 2.5 \text{ V} \pm 0.2 \text{V}$)



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¹ C_L includes probe and jig capacitance.

Voltage and Current Waveforms

In the following waveforms, note that all input pulses are supplied by generators having the following characteristics: $PRR \le 10 \text{ MHz}$, $Z_0 = 50 \Omega$, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

The outputs are measured one at a time with one transition per measurement.

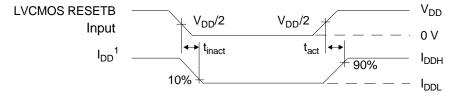
 $V_{TT} = V_{REF} = V_{DDQ}/2$.

 $V_{IH} = V_{REF} + 310 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

 $V_{IL} = V_{REF}$ - 310 mV (AC voltage levels) for differential inputs. $V_{IL} = GND$ for LVCMOS input.

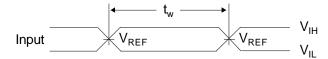
 t_{PLH} and t_{PHL} are the same as t_{pd} .

Input active and inactive times

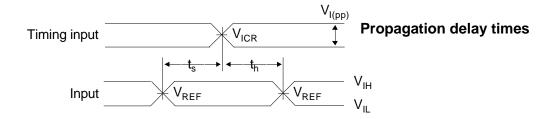


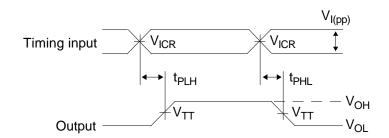
 $^{^{1}}$ I_{DD} tested with clock and data inputs held at V _{DD} or GND, and I_O = 0 mA.

Pulse duration

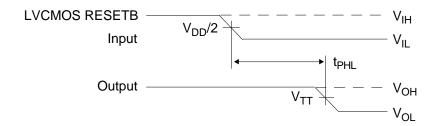


Setup and hold times

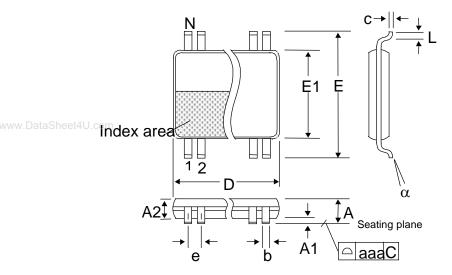




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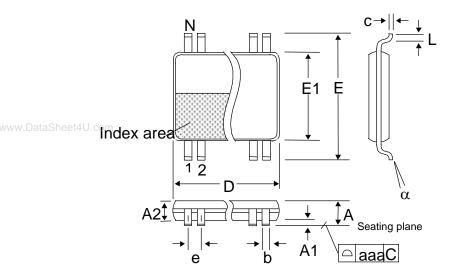
6.10 mm (240 mil) body, 0.50 mm (0.020 mil) pitch TSSOP

Symbol	Millim	neters	Inches		
Syllibol	Min	Max	Min	Max	
Α	_	1.20	_	0.047	
A1	0.05	0.15	0.002	0.006	
A2	0.80	1.05	0.32	0.041	
b	0.17	0.27	0,007	0.011	
С	0.09	0.20	0.0035	0.008	
D		See variat	ions below		
E	8.10	basic	0.319	basic	
E1	6.00	6.20	0.236	0.244	
е	0.50	basic	0.020	basic	
L	0.45	0.75	0.018	0.030	
N		See variat	e variations below		
а	0°	8°	0°	8°	
aaa	_	0.10	_	0.004	

Variations:

N	D (r	nm) D (in		D (mm) D (inch)	
IN .	Min	Max	Min	Max	
48	12.40	12.60	0.488	0.496	





4.40 mm (173 mil) body, 0.40 mm (16 mil) pitch TVSOP

Symbol	Millim	neters	Inches			
Syllibol	Min	Max	Min	Max		
Α	_	1.20	_	0.047		
A1	0.05	0.15	0.002	0.006		
A2	0.80	1.05	0.32	0.041		
b	0.13	0.23	0,005	0.009		
С	0.09	0.20	0.0035	0.008		
D		See variat	ions below			
E	6.40	basic	0.252	basic		
E1	4.30	4.50	0.169	0.177		
е	0.40	basic	0.016	basic		
L	0.45	0.75	0.018	0.030		
N		See variat	See variations below			
а	0°	8°	0°	8°		
aaa	_	0.08	_	0.003		

Variations

N	D (mm)		D (inch)	
	Min	Max	Min	Max
48	9.60	9.80	0.378	0.386

Ordering Codes

Ordering Number	Marking	Package Type	Quantity per reel	Temperature
ASM4SSTVF16857-48TT	AS4SSTVF16857T	48-pin TSSOP, tube		0°C to 70°C
ASM4SSTVF16857-48TR	AS4SSTVF16857T	48-pin TSSOP, tape and reel	2500	0°C to 70°C
ASM4SSTVF16857-48VT	AS4SSTVF16857V	48-pin TVSOP, tube		0°C to 70°C
ASM4SSTVF16857-48VR	AS4SSTVF16857V	48-pin TVSOP, tape and reel	2500	0°C to 70°C

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