



3.3V 'SpreadTrak' Zero Delay Buffer

General Features

- 10 MHz to 133- MHz operating range, compatible with CPU and PCI bus frequencies.
- Zero input - output propagation delay.
- Multiple low-skew outputs.
 - Output-output skew less than 250 ps.
 - Device-device skew less than 700 ps.
 - One input drives 9 outputs, grouped as 4 + 4 + 1 (ASM5P23S09A).
 - One input drives 5 outputs (ASM5P23S05A).
- Less than 200 ps cycle-to-cycle jitter is compatible with Pentium® based systems.
- Test Mode to bypass PLL (ASM5P23S09A only, refer Select Input Decoding Table).
- Available in 16-pin, 150-mil SOIC, 4.4 mm TSSOP, and 150-mil SSOP packages (ASM5P23S09A) or in 8-pin, 150-mil SOIC package (ASM5P23S05A).
- 3.3V operation, advanced 0.35µ CMOS technology.
- 'SpreadTrak'.

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133- MHz frequencies, and has higher drive than the -1 devices. All parts have on-chip PLLs that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The ASM5P23S09A has two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding Table. If all the output clocks are not required, Bank B can be three-stated. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

Multiple ASM5P23S09A and ASM5P23S05A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 250 ps, and the output to output skew is guaranteed to be less than 250ps.

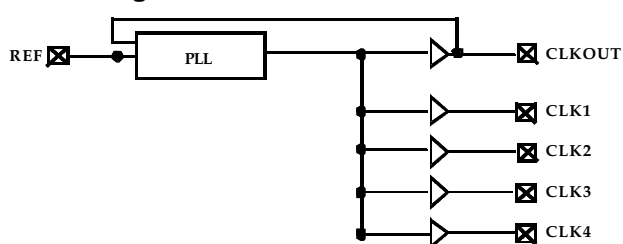
Functional Description

ASM5P23S09A is a versatile, 3.3V zero-delay buffer designed to distribute high-speed clocks with Spread Spectrum capability. It is available in a 16-pin package. The ASM5P23S05A is the eight-pin version of the ASM5P23S09A. It accepts one reference input and drives out five low-skew clocks.

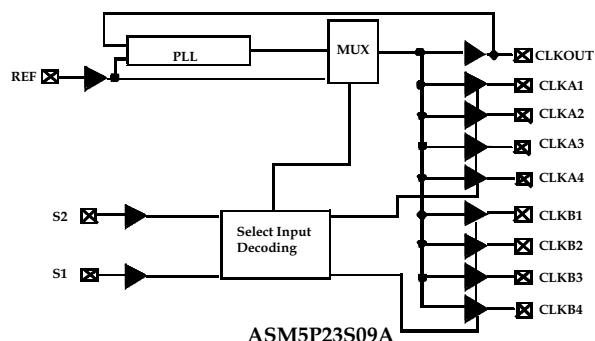
The -1H version of the ASM5P23SXXA operates at up to

The ASM5P23S09A and the ASM5P23S05A are available in two different configurations, as shown in the ordering information table. The ASM5P23SXXA-1 is the base part. The ASM5P23SXXA-1H is the high drive version of the -1 and its rise and fall times are much faster than -1 part.

Block Diagram



ASM5P23S05A



ASM5P23S09A



Select Input Decoding for ASM5P23S09A

| S2 | S1 | Clock A1 - A4 | Clock B1 - B4 | CLKOUT ¹ | Output Source | PLL Shut-Down |
|----|----|---------------|---------------|---------------------|---------------|---------------|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

Notes:

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the output.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero-input-output delay.

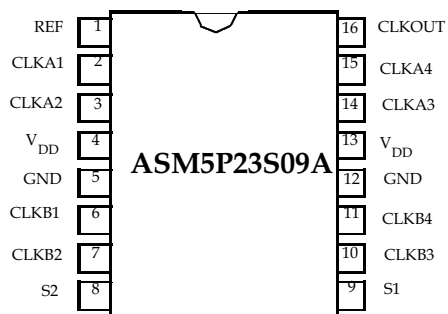
SpreadTrak

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. ASMP5P23S09A and ASMP5P23S05A are designed so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

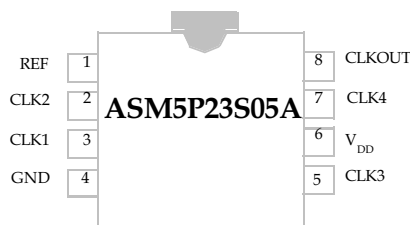


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Pin Configuration



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Pin Description for ASM5P23S09A

| Pin # | Pin Name | Description |
|-------|---------------------|--|
| 1 | REF ² | Input reference frequency, 5V tolerant input |
| 2 | CLKA1 ³ | Buffered clock output, bank A |
| 3 | CLKA2 ³ | Buffered clock output, bank A |
| 4 | V _{DD} | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB1 ³ | Buffered clock output, bank B |
| 7 | CLKB2 ³ | Buffered clock output, bank B |
| 8 | S2 ⁴ | Select input, bit 2 |
| 9 | S1 ⁴ | Select input, bit 1 |
| 10 | CLKB3 ³ | Buffered clock output, bank B |
| 11 | CLKB4 ³ | Buffered clock output, bank B |
| 12 | GND | Ground |
| 13 | V _{DD} | 3.3V supply |
| 14 | CLKA3 ³ | Buffered clock output, bank A |
| 15 | CLKA4 ³ | Buffered clock output, bank A |
| 16 | CLKOUT ³ | Buffered output, internal feedback on this pin |

Pin Description for ASM5P23S05A

| Pin # | Pin Name | Description |
|-------|---------------------|--|
| 1 | REF ² | Input reference frequency, 5V-tolerant input |
| 2 | CLK2 ³ | Buffered clock output |
| 3 | CLK1 ³ | Buffered clock output |
| 4 | GND | Ground |
| 5 | CLK3 ³ | Buffered clock output |
| 6 | V _{DD} | 3.3V supply |
| 7 | CLK4 ³ | Buffered clock output |
| 8 | CLKOUT ³ | Buffered clock output, internal feedback on this pin |

Notes:

2. Weak pull-down.
3. Weak pull-down on all outputs.
4. Weak pull-up on these inputs.



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Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|--|------|-----------|------|
| Supply Voltage to Ground Potential | -0.5 | +7.0 | V |
| DC Input Voltage (Except REF) | -0.5 | VDD + 0.5 | V |
| DC Input Voltage (REF) | -0.5 | 7 | V |
| Storage Temperature | -65 | +150 | °C |
| Max. Soldering Temperature (10 sec) | | 260 | °C |
| Junction Temperature | | 150 | °C |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | | 2000 | V |

Note: These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.

Operating Conditions for ASM5P23S05A and ASM5P23S09A - Commercial Temperature Devices

| Parameter | Description | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| V _{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| C _L | Load Capacitance, below 100 MHz | | 30 | pF |
| C _L | Load Capacitance, from 100 MHz to 133 MHz | | 10 | pF |
| C _{IN} | Input Capacitance | | 7 | pF |



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Electrical Characteristics for ASM5P23S05A and ASM5P23S09A - Commercial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|-----------------|----------------------------------|---|-----|-------|------|
| V _{IL} | Input LOW Voltage ⁵ | | | 0.8 | V |
| V _{IH} | Input HIGH Voltage ⁵ | | 2.0 | | V |
| I _{IL} | Input LOW Current | V _{IN} = 0V | | 50.0 | μA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | | 100.0 | μA |
| V _{OL} | Output LOW Voltage ⁶ | I _{OL} = 8mA (-1) I _{OH} = 12mA (-1H) | | 0.4 | V |
| V _{OH} | Output HIGH Voltage ⁶ | I _{OL} = -8mA (-1) I _{OH} = -12mA (-1H) | 2.4 | | V |
| I _{DD} | Supply Current | Unloaded outputs at 66.67 MHz, SEL inputs at V _{DD} | | TBD | mA |

Notes:

5. REF input has a threshold voltage of V_{DD}/2
 6. Parameter is guaranteed by design and characterization. Not 100% tested in production
 7. S1 / S2 inputs are CMOS, TTL compatible inputs –

The input must toggle somewhere between 0.8 and 2.0. We guarantee the limits of 0.8 and 2.0, but can't guarantee anything tighter than that. As V_{DD} moves higher the toggle point will move higher, but will always stay below 2.0V. As V_{DD} moves lower, the toggle point will move lower, but always stay higher than 0.8V. What the 2.0V MIN V_{IH} specification means is that you put 2.0V or a higher voltage into the device, and you will have a logic HIGH. If you put 0.8V or a lower voltage into the device, you will have a logic LOW (V_{IL} spec = 0.8V max). It will toggle someplace in between 0.8V and 2.0V, but we don't guarantee exactly where, and the exact point will change depending upon conditions. Characterization shows we toggle at 1.1V and 1.5V (showing a little hysteresis), everything is perfect. We meet spec, plus have ~ 300mV noise immunity on the low end and ~500mV noise immunity on the high side. Under nominal conditions, with no hysteresis, most devices will toggle at about 1.5V for both high and low.

Switching Characteristics for ASM5P23S05A-1 and ASM5P23S09A-1 - Commercial Temperature Devices⁷

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-------------------|--|---|----------|------|---------------|------|
| 1/t ₁ | Output Frequency | 30-pF load 10-pF load | 10 10 | | 100 133.33 | MHz |
| | Duty Cycle ⁶ = (t ₂ / t ₁) * 100 | Measured at 1.4V, F _{OUT} = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| t ₃ | Output Rise Time ⁶ | Measured between 0.8V and 2.0V | | | 2.50 | ns |
| t ₄ | Output Fall Time ⁶ | Measured between 2.0V and 0.8V | | | 2.50 | ns |
| t ₅ | Output-to-output skew ⁶ | All outputs equally loaded | | | 250 | ps |
| t ₆ | Delay, REF Rising Edge to CLKOUT Rising Edge ⁶ | Measured at V _{DD} /2 | | 0 | ±350 | ps |
| t ₇ | Device-to-Device Skew ⁶ | Measured at V _{DD} /2 on the CLKOUT pins of the device | | 0 | 700 | ps |
| t _J | Cycle-to-cycle jitter ⁶ | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| t _{LOCK} | PLL Lock Time ⁶ | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |

Notes:

7. All parameters specified with loaded outputs.

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ASM5P23S09A
ASM5P23S05A

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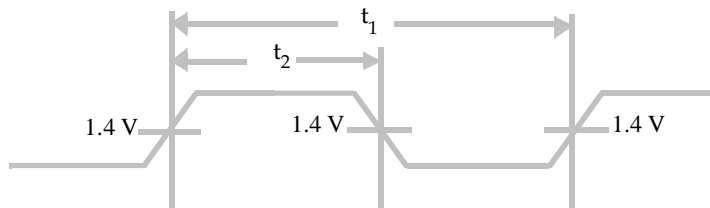
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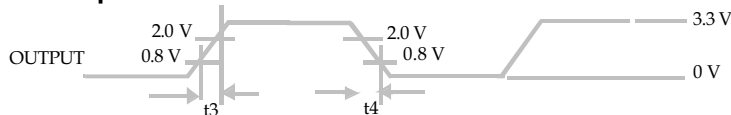
Switching Characteristics for ASM5I23S05A-1H and ASM5I23S09A-1H - Industrial Temperature Devices⁷

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-------------------|--|--|------|------|--------|------|
| 1/t ₁ | Output Frequency | 30-pF load | 10 | | 100 | MHz |
| | | 10-pF load | 10 | | 133.33 | |
| | Duty Cycle ⁶ = (t ₂ / t ₁) * 100 | Measured at 1.4 V, F _{OUT} = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| | Duty Cycle ⁶ = (t ₂ / t ₁) * 100 | Measured at 1.4 V, F _{OUT} < 50.0 MHz | 45.0 | 50.0 | 55.0 | |
| t ₃ | Output Rise Time ⁶ | Measured between 0.8V and 2.0V | | | 1.50 | ns |
| t ₄ | Output Fall Time ⁶ | Measured between 2.0V and 0.8V | | | 1.50 | ns |
| t ₅ | Output-to-output skew ⁶ | All outputs equally loaded | | | 250 | ps |
| t ₆ | Delay, REF Rising Edge to CLKOUT Rising Edge ⁶ | Measured at VDD /2 | | 0 | ± 350 | ps |
| t ₇ | Device-to-Device Skew ⁶ | Measured at VDD/2 on the CLKOUT pins of the device | | 0 | 700 | ps |
| t ₈ | Output Slew Rate ⁶ | Measured between 0.8V and 2.0V using Test Circuit #2 | 1 | | | V/ns |
| t _J | Cycle-to-cycle jitter ⁶ | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| t _{LOCK} | PLL Lock Time ⁶ | Stable power supply, valid clock pre sented on REF pin | | | 1.0 | ms |

Switching Waveforms
Duty Cycle Timing



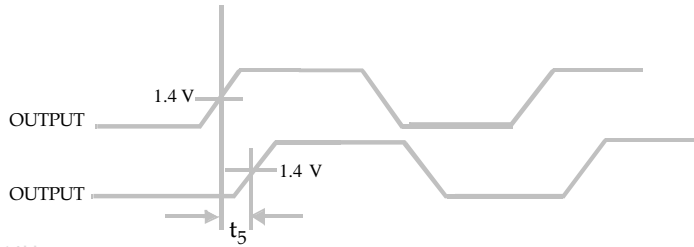
All Outputs Rise/Fall Time





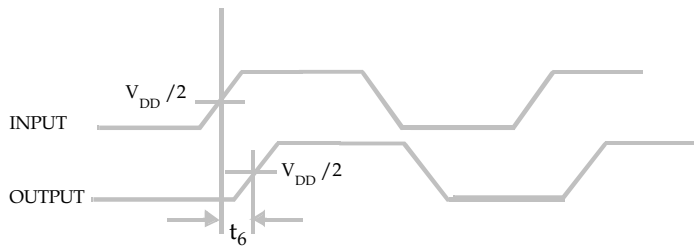
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Output - Output Skew

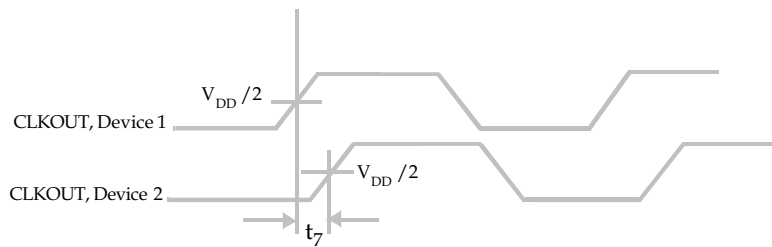


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Input - Output Propagation Delay



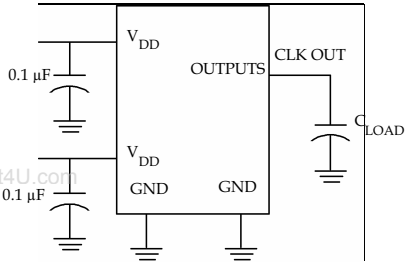
Device - Device Skew



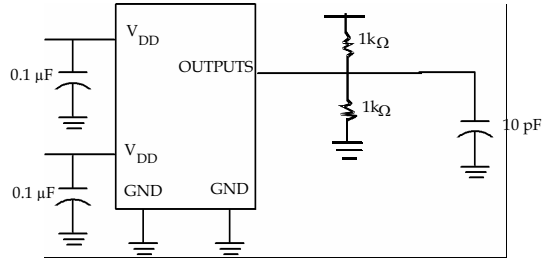


Test Circuits

Test Circuit #1



Test Circuit #2



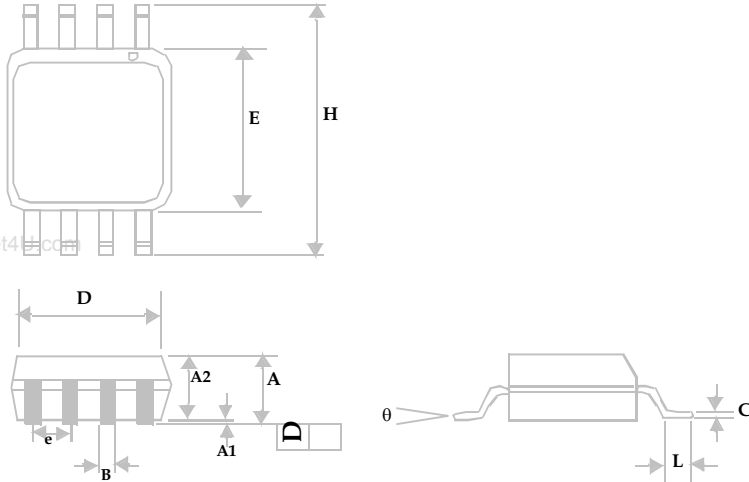
For parameter t_j (output slew rate) on -1H devices

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Package Information: 8-lead (150-mil) SOIC

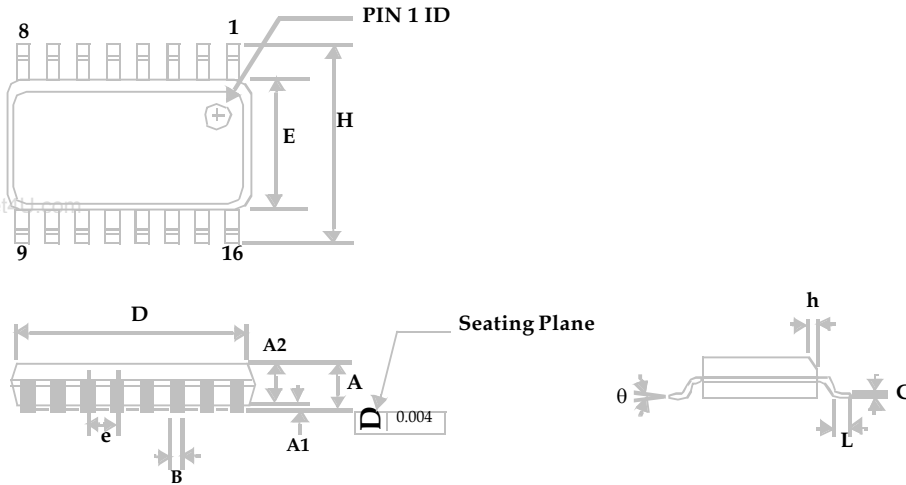


| Symbol | Dimensions in inches | | Dimensions in millimeters | |
|----------|----------------------|-------|---------------------------|------|
| | Min | Max | Min | Max |
| A | 0.057 | 0.071 | 1.45 | 1.80 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| A2 | 0.053 | 0.069 | 1.35 | 1.75 |
| B | 0.012 | 0.020 | 0.31 | 0.51 |
| C | 0.004 | 0.01 | 0.10 | 0.25 |
| D | 0.186 | 0.202 | 4.72 | 5.12 |
| E | 0.148 | 0.164 | 3.75 | 4.15 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.224 | 0.248 | 5.70 | 6.30 |
| L | 0.012 | 0.028 | 0.30 | 0.70 |
| θ | 0° | 8° | 0° | 8° |



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Package Information: 16-lead (150 Mil) Molded SOIC

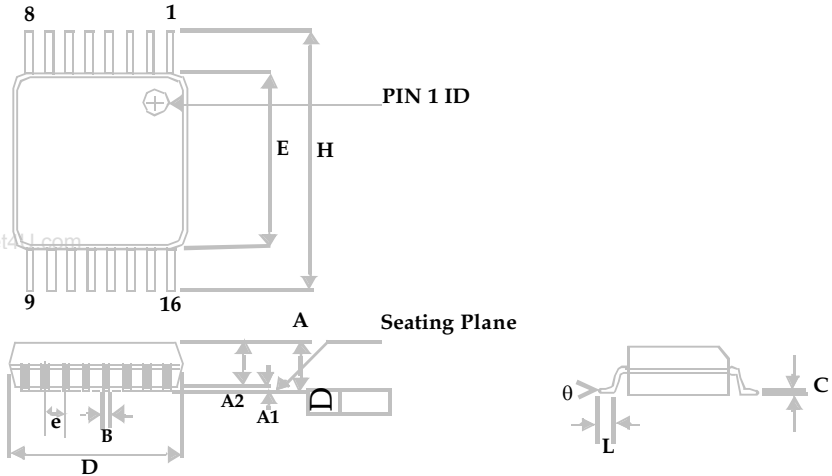


| | DIMENSIONS | | | |
|----|------------|--------|-------------|-------|
| | INCHES | | MILLIMETERS | |
| | MIN | MAX | MIN | MAX |
| A | 0.061 | 0.068 | 1.55 | 1.73 |
| A1 | 0.004 | 0.0098 | 0.102 | 0.249 |
| A2 | 0.055 | 0.061 | 1.40 | 1.55 |
| B | 0.013 | 0.019 | 0.33 | 0.49 |
| C | 0.0075 | 0.0098 | 0.191 | 0.249 |
| D | 0.386 | 0.393 | 9.80 | 9.98 |
| E | 0.150 | 0.157 | 3.81 | 3.99 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.230 | 0.244 | 5.84 | 6.20 |
| h | 0.010 | 0.016 | 0.25 | 0.41 |
| L | 0.016 | 0.035 | 0.41 | 0.89 |
| θ | 0° | 8° | 0° | 8° |



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Package Information: 16-lead Thin Shrunken Small Outline Package (4.40-MM Body)

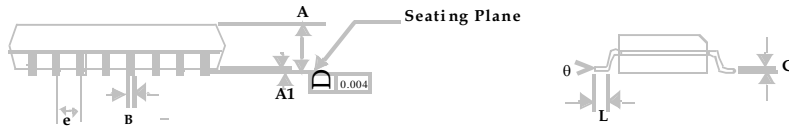
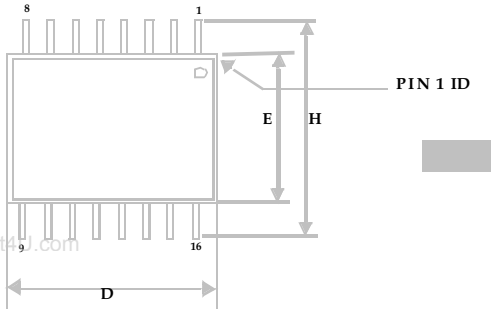


| | DIMENSIONS (inches) | | DIMENSIONS (mm) | |
|----|---------------------|-------|-----------------|------|
| | MIN | MAX | MIN | MAX |
| A | | 0.043 | | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.003 | 0.37 | 0.85 | 0.95 |
| B | 0.007 | 0.012 | 0.19 | 0.30 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.193 | 2.008 | 4.90 | 5.10 |
| E | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.026 BSC | | 0.65 BSC | |
| H | 0.246 | 0.256 | 6.25 | 6.50 |
| L | 0.020 | 0.028 | 0.50 | 0.70 |
| θ | 0° | 8° | 0° | 8° |



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Package Information: 16-lead (150-mil) SSOP



| | DIMENSIONS (inches) | | DIMENSIONS (millimeters) | |
|----------|---------------------|-------|--------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.049 | 0.065 | 1.245 | 1.651 |
| A1 | 0.004 | 0.010 | 0.102 | 0.254 |
| B | 0.008 | 0.012 | 0.203 | 0.305 |
| C | 0.007 | 0.010 | 0.178 | 0.254 |
| D | 0.189 | 0.197 | 4.801 | 5.004 |
| E | 0.150 | 0.157 | 3.81 | 3.988 |
| e | 0.025 BSC | | 0.635 BSC | |
| H | 0.228 | 0.244 | 5.791 | 6.198 |
| L | 0.016 | 0.050 | 0.406 | 1.27 |
| θ | 0° | 8° | 0° | 8° |



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Ordering Codes

| Ordering Code | Package Type | Operating Range |
|----------------------|---------------------------------|-----------------|
| ASM5P23S09A-1-16-ST | 16-pin 150-mil SOIC-TUBE | Commercial |
| ASM5I23S09A-1-16-ST | 16-pin 150-mil SOIC-TUBE | Industrial |
| ASM5P23S09A-1-16-SR | 16-pin 150-mil SOIC-TAPE & REEL | Commercial |
| ASM5I23S09A-1-16-SR | 16-pin 150-mil SOIC-TAPE & REEL | Industrial |
| ASM5P23S09A-1-16-TT | 16-pin 4.4-mm TSSOP-TUBE | Commercial |
| ASM5I23S09A-1-16-TT | 16-pin 4.4-mm TSSOP-TUBE | Industrial |
| ASM5P23S09A-1-16-TR | 16-pin 4.4-mm TSSOP-TAPE & REEL | Commercial |
| ASM5I23S09A-1-16-TR | 16-pin 4.4-mm TSSOP-TAPE & REEL | Industrial |
| ASM5P23S09A-1H-16-ST | 16-pin 150-mil SOIC-TUBE | Commercial |
| ASM5I23S09A-1H-16-ST | 16-pin 150-mil SOIC-TUBE | Industrial |
| ASM5P23S09A-1H-16-SR | 16-pin 150-mil SOIC-TAPE & REEL | Commercial |
| ASM5I23S09A-1H-16-SR | 16-pin 150-mil SOIC-TAPE & REEL | Industrial |
| ASM5P23S09A-1H-16-TT | 16-pin 4.4-mm TSSOP-TUBE | Commercial |
| ASM5I23S09A-1H-16-TT | 16-pin 4.4-mm TSSOP-TUBE | Industrial |
| ASM5P23S09A-1H-16-TR | 16-pin 4.4-mm TSSOP-TAPE & REEL | Commercial |
| ASM5I23S09A-1H-16-TR | 16-pin 4.4-mm TSSOP-TAPE & REEL | Industrial |
| ASM5P23S05A-1-08-ST | 8-pin 150-mil SOIC-TUBE | Commercial |
| ASM5I23S05A-1-08-ST | 8-pin 150-mil SOIC-TUBE | Industrial |
| ASM5P23S05A-1-08-SR | 8-pin 150-mil SOIC-TAPE & REEL | Commercial |
| ASM5I23S05A-1-08-SR | 8-pin 150-mil SOIC-TAPE & REEL | Industrial |
| ASM5P23S05A-1-08-TT | 8-pin 4.4-mm TSSOP-TUBE | Commercial |
| ASM5I23S05A-1-08-TT | 8-pin 4.4-mm TSSOP-TUBE | Industrial |
| ASM5P23S05A-1-08-TR | 8-pin 4.4-mm TSSOP-TAPE & REEL | Commercial |
| ASM5I23S05A-1-08-TR | 8-pin 4.4-mm TSSOP-TAPE & REEL | Industrial |
| ASM5P23S05A-1H-08-ST | 8-pin 150-mil SOIC-TUBE | Commercial |
| ASM5I23S05A-1H-08-ST | 8-pin 150-mil SOIC-TUBE | Industrial |
| ASM5P23S05A-1H-08-SR | 8-pin 150-mil SOIC-TAPE & REEL | Commercial |
| ASM5I23S05A-1H-08-SR | 8-pin 150-mil SOIC-TAPE & REEL | Industrial |
| ASM5P23S05A-1H-08-TT | 8-pin 4.4-mm TSSOP-TUBE | Commercial |
| ASM5I23S05A-1H-08-TT | 8-pin 4.4-mm TSSOP-TUBE | Industrial |
| ASM5P23S05A-1H-08-TR | 8-pin 4.4-mm TSSOP-TAPE & REEL | Commercial |
| ASM5I23S05A-1H-08-TR | 8-pin 4.4-mm TSSOP-TAPE & REEL | Industrial |

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 Preliminary datasheet. Specification subject to change without notice.

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Alliance Semiconductor Corporation
2595, Augustine Drive,
Santa Clara, CA 95054
Tel# 408-855-4900
Fax: 408-855-4999
www.alsc.com

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