July 2004

rev 1.2

Low Power µP Supervisor Circuits

General Description

The ASM705 / 706 / 707 / 708 and AS813L are cost effective CMOS supervisor circuits that monitor power-supply and battery voltage level, and µP/µC operation.

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions. A reset is generated when the supply drops below 4.65V (ASM705/707/813L) or 4.40V (ASM706/708). For 3V power supply applications, refer to the ASM705P/R/S/T data sheet. In addition, the ASM705/706/813L feature a 1.6 second watchdog timer. The ASM707/708 have both active-HIGH and active-LOW reset outputs but no watchdog function. The ASM813L has the same pin-out and functions as the ASM705 but has an active-HIGH reset output. A versatile power-fail circuit has a 1.25V threshold, useful in low battery detection and for monitoring non-5V supplies. All devices have a manual reset ($\overline{MR}$) input. The watchdog timer output will trigger a reset if connected to $\overline{MR}$.

All devices are available in 8-pin DIP, SO and MicroSO packages.

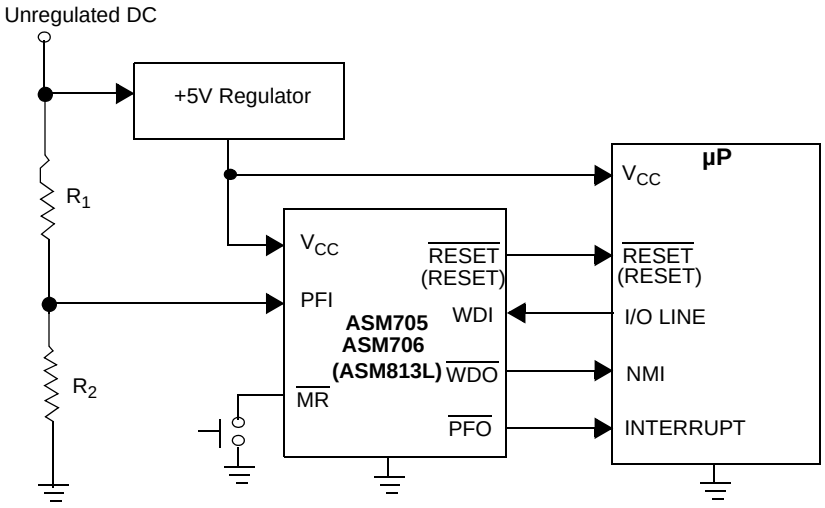
Features

- Precision power supply monitor
  - •4.65V threshold (ASM705/707/813L)
  - •4.40V threshold (ASM706/708)
- Debounced manual reset input
- Voltage monitor
  - •1.25V threshold
  - •Battery monitor / Auxiliary supply monitor
- Watchdog timer (ASM705/706/813L)
- 200ms reset pulse width
- Active HIGH reset output (ASM707/708/813L)
- MicroSO package

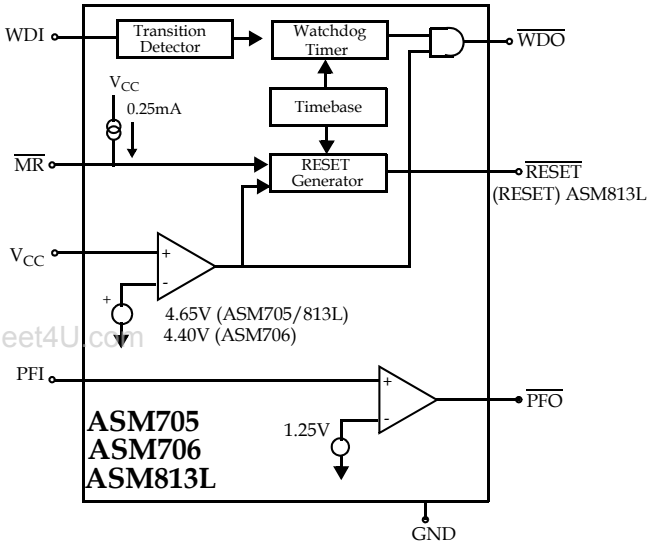
Applications

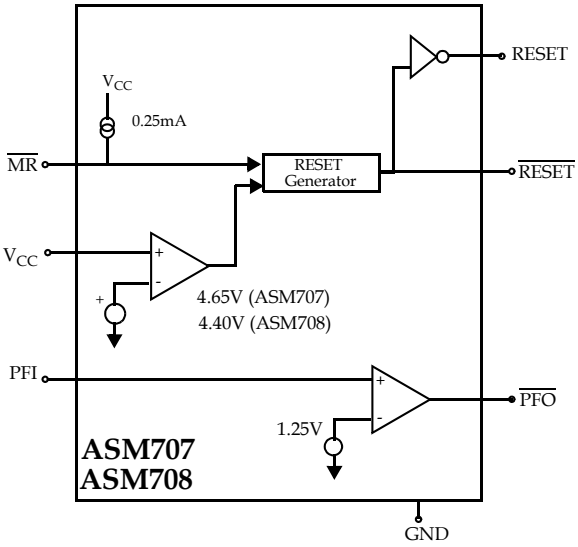
- Computers and embedded controllers
- Portable/Battery-operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and hendheld equipment
- Automative Systems
- Safety Systems

Typical Operating Circuit



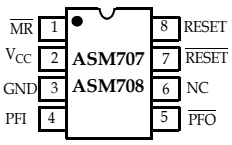
Block Diagrams

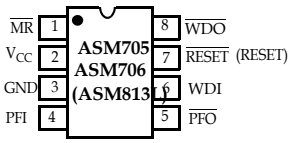




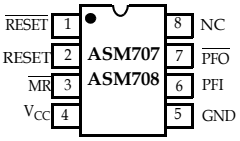
Pin Configuration

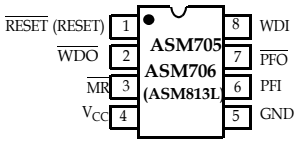
DIP/SO





MicroSO





Pin Description

Pin Number						Name	Function
ASM705/706		ASM707/708		ASM813L			
DIP/ SO	MicroSO	DIP/ SO	MicroSO	DIP/ SO	MicroSO		
1	3	1	3	1	3	$\overline{MR}$	Manual reset input. The active LOW input triggers a reset pulse. A 250 µA pull-up current allows the pin to be driven by TTL/CMOS logic or shorted to ground with a switch.
2	4	2	4	2	4	V_{CC}	+5V power supply input.
3	5	3	5	3	5	GND	Ground reference for all signals.
4	6	4	6	4	6	PFI	Power-fail input voltage monitor. With PFI less than 1.25V, $\overline{PFO}$ goes LOW. Connect PFI to Ground or V_{CC} when not in use.
5	7	5	7	5	7	$\overline{PFO}$	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	-	-	6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6sec at WDI allows the internal timer to run-out, setting $\overline{WDO}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high impedance three-state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated ; or WDI sees a rising or falling edge.
-	-	6	8	-	-	NC	Not Connected
7	1	7	1	-	-	$\overline{RESET}$	Active LOW reset output. Pulses LOW for 200ms when triggered, and stays LOW whenever V_{CC} is below the reset threshold. $\overline{RESET}$ remains LOW for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	2	-	-	8	2	$\overline{WDO}$	Watchdog output. $\overline{WDO}$ goes LOW when the 1.6 second internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when V_{CC} falls below the reset threshold, $\overline{WDO}$ goes LOW. Unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width and as soon as V_{CC} exceeds the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
-	-	8	2	7	1	RESET	Active HIGH reset output. The inverse of $\overline{RESET}$. The ASM813L has only a RESET output.

Detailed Description

A proper reset input enables a microprocessor / microcontroller to start in a known state. ASM70X and ASM813L assert reset to prevent code execution errors during power-up, power-down and brown-out conditions.

RESET/$\overline{\text{RESET}}$ Timing

The RESET/$\overline{\text{RESET}}$ signals are designed to start a µP/µC in a known state or return the system to a known state.

The ASM707/708 have two reset outputs, one active-HIGH RESET and one active-LOW $\overline{\text{RESET}}$ output. The ASM813L has only an active-HIGH output. RESET is simply the complement of $\overline{\text{RESET}}$.

$\overline{\text{RESET}}$ is guaranteed to be LOW with V_{CC} above 1.2V. During a power-up sequence, $\overline{\text{RESET}}$ remains low until the supply rises above the threshold level, either 4.65V or 4.40V. $\overline{\text{RESET}}$ goes high approximately 200ms after crossing the threshold.

During power-down, $\overline{\text{RESET}}$ goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.4V with V_{CC} above 1.2V.

In a brownout situation where V_{CC} falls below the threshold level, $\overline{\text{RESET}}$ pulses low. If a brownout occurs during an already initiated reset, the pulse will continue for a minimum of 140ms.

Power Failure Detection With Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output ($\overline{\text{PFO}}$) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{\text{PFO}}$ output to transit LOW. Normally $\overline{\text{PFO}}$ interrupts the processor so the system can be shut down in a controlled manner.

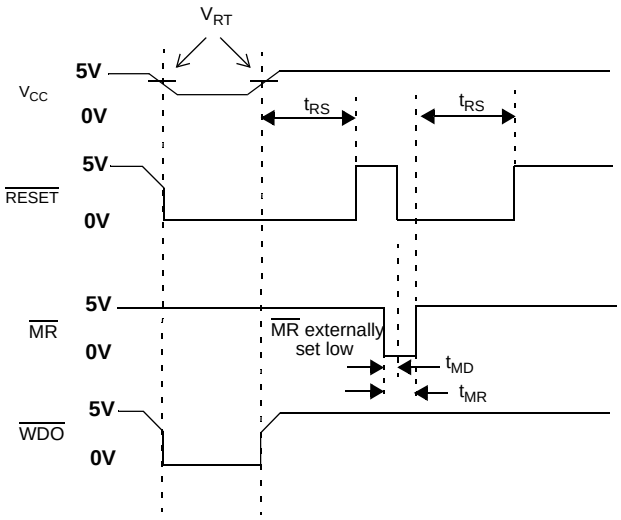


Figure 1: WDI Three-state operation

Manual Reset ($\overline{\text{MR}}$)

The active-LOW manual reset input is pulled high by a 250µA pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces $\overline{\text{RESET}}$ to be generated. The ASM813L should be used when an active-HIGH RESET is required.

Watchdog Timer

The watchdog timer available on the ASM705/706/813L monitors µP/µC activity. An output line on the processor is used to toggle the WDI line. If this line is not toggled within 1.6 seconds, the internal timer puts the watchdog output, $\overline{\text{WDO}}$, into a LOW state. $\overline{\text{WDO}}$ will remain LOW until a toggle is detected at WDI.

If WDI is floated or connected to a three-stated circuit, the watchdog function is disabled, meaning, it is cleared and not counting. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown. Additional

transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{WDO}$ will also become LOW and remain so, whenever the supply voltage, V_{CC} , falls below the device threshold level. $\overline{WDO}$ goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for $\overline{WDO}$ as there is for the RESET outputs. If WDI is floated, $\overline{WDO}$ essentially acts as a low-power output indicator.

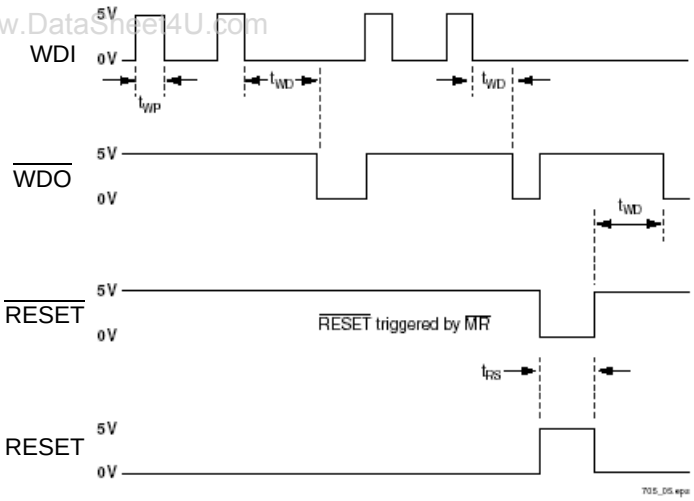


Figure 2: Watchdog Timing

Application Information

Ensuring That $\overline{RESET}$ is Valid Down to V_{CC} = 0V

When V_{CC} falls below 1.1V, the ASM705-708 $\overline{RESET}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{RESET}$ to the wrong state, a pull-down resistor should be connected to the $\overline{RESET}$ pin, thus draining such charges to ground and holding $\overline{RESET}$ low. The resistor value is not critical. A 100kΩ resistor will pull $\overline{RESET}$ to ground without loading it.

Bi-directional Reset Pin Interfacing

The ASM705/6/7/8 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the $\overline{RESET}$ output and the µP/µC bi-directional $\overline{RESET}$ pin.

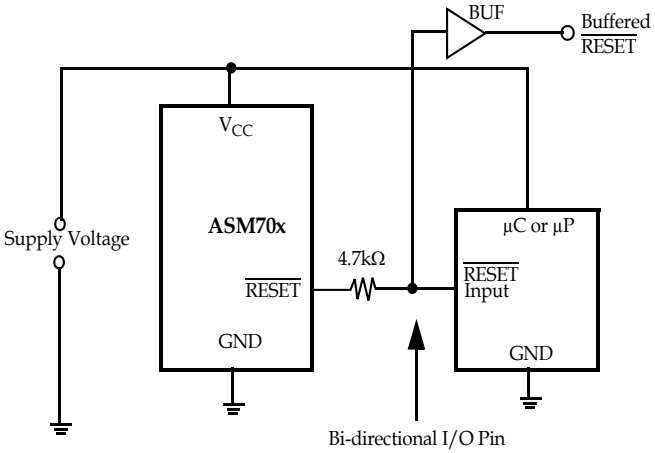


Figure 3: Bi-directional Reset Pin Interfacing

Monitoring Voltages Other Than V_{CC}

The ASM705-708 can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the Power Fail input (PFI), the $\overline{PFO}$ will go LOW if the voltage at PFI goes below 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and $\overline{PFO}$ pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a $\overline{RESET}$ for voltages other than V_{CC} then the $\overline{PFO}$ output is to be connected to the $\overline{MR}$.

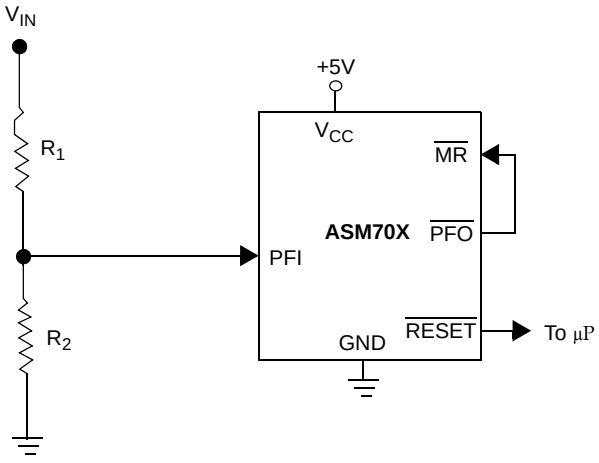


Figure 4: Monitoring +5V and an additional supply V_{IN}

Monitoring a Negative Voltage

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, $\overline{PFO}$ will be LOW, and when the negative rail is failing (not negative enough), $\overline{PFO}$ goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The $\overline{RESET}$ output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the V_{CC} line, the PFI threshold tolerance, and the resistors.

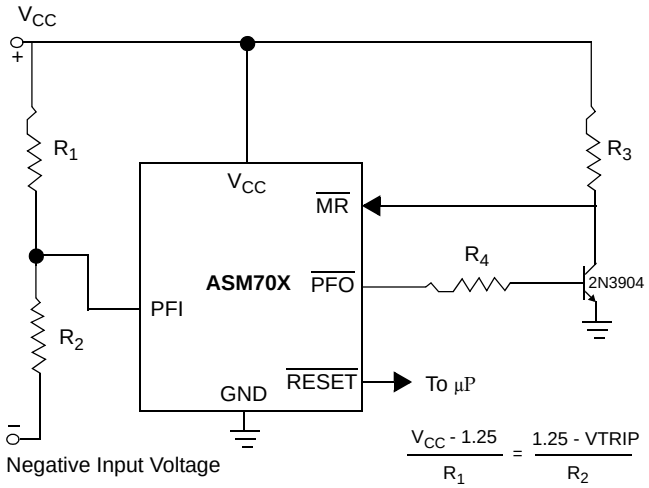


Figure 5: Monitoring a negative voltage

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Pin Terminal Voltage with Respect to Ground			
V_{CC}	-0.3	6.0	V
All other inputs [1]	-0.3	V_{CC} + 0.3	V
Input Current at V_{CC} and GND		20	mA
Output Current: All outputs		20	mA
Rate of Rise at V_{CC}		100	V/µs
Plastic DIP Power Dissipation (Derate 9mW/°C above 70°C)		700	mV
SO Power Dissipation (Derate 5.9mW/°C above 70°C)		470	mW‘
MicroSO Power Dissipation (Derate 4.1mW/°C above 70°C)		330	mW
Operating Temperature Range			
ASM705E/706E/707E/708E/813LE	-40	+85	°C
ASM706C/707C/708C/813LC	0	70	°C
Storage Temperature Range	-65	160	°C
Lead Temperature (Soldering 10sec)		300	°C

Note:
1. The input voltage limits of PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.
These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.

Electrical Characteristics

Unless otherwise noted, specifications are over the operating temperature range and V_{CC} supply voltages are 2.7V to 5.5V (ASM706P, ASM708R), 3.0 V to 5.5V (ASM706/708S), 3.15V to 5.5V (ASM706/708T) and 4.1V to 5.5.V (ASM706/708J)

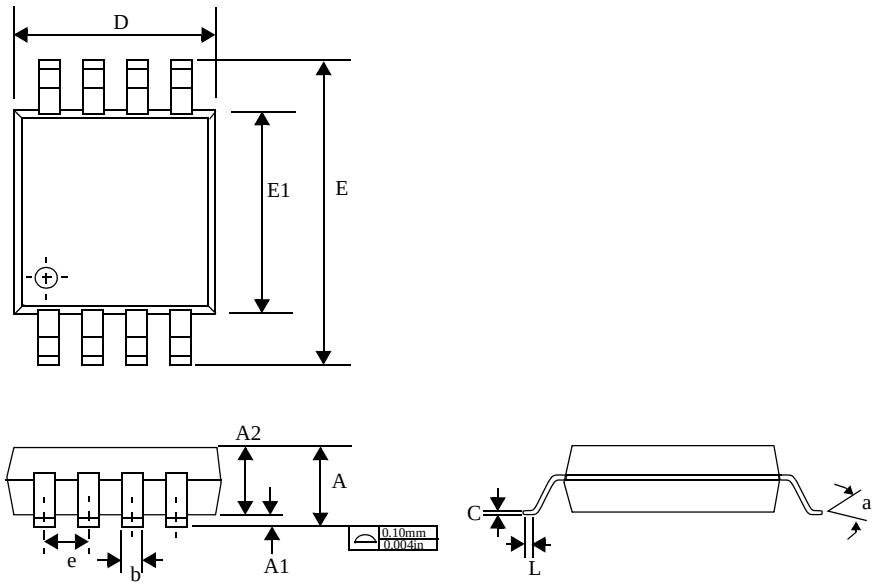
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}	ASM705/6/7/8C	1.2		5.5	V
		ASM813L	1.1		5.5	
		ASM705/6/7/8E, ASM813E	1.2		5.5	
Supply Current	I_{CC}	ASM705/706C/813LC		75	140	µA
		ASM705E/706E/813LE		75	140	
		ASM707C/708C		50	140	
		ASM707E/708E		50	140	
RESET Threshold	V_{RT}	ASM705/707/813L, Note 1	4.50	4.65	4.75	V
		ASM706/708 Note 1	4.25	4.40	4.50	
RESET Threshold Hysteresis		Note 1		40		mV
RESET Pulse Width	t_{RS}	Note 1	140	200	280	ms
$\overline{MR}$ Pulse Width	t_{MR}		0.15			µs
$\overline{MR}$ to RESET Out Delay	t_{MD}	Note 1			0.25	µs
$\overline{MR}$ Input Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
$\overline{MR}$ Pullup current		$\overline{MR}$ = 0V	100	250	600	µA
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		I_{SINK} = 3.2mA			0.4	
		ASM705/5/7/8, V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
RESET Output Voltage		ASM707/8/813L, I_{SOURCE} = 800µA	V_{CC}-1.5			V
		ASM707/8, I_{SINK} = 1.2mA			0.4	
		ASM813L, I_{SINK} =3.2mA			0.4	
		ASM813L, V_{CC} = 1.2V, I_{SOURCE} = 4µA	0.9			

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Watchdog Timeout Period	t_{WD}	ASM705/6/813L	1.00	1.60	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH}=0.8V_{CC},	50			ns
WDI Input Threshold	V_{IH}	ASM705/706/813L, V_{CC} = 5V	3.5			V
	V_{IL}				0.8	
WDI Input Current		ASM705/6/813L, WDI = V_{CC}		50	150	µA
		ASM705/6/813L, WDI = 0V	-150	-50		
$\overline{WDO}$ Output Voltage	V_{OH}	ASM705/6/813L, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
	V_{OL}	ASM705/6/813L, I_{SINK} = 1.2mA			0.4	
PFI Input Threshold		V_{CC} = 5V	1.2	1.25	1.3	V
PFI Input Current			-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA	V_{CC} - 1.5			V
	V_{OL}	I_{SINK} = 3.2mA			0.4	

Notes 1: $\overline{RESET}$ (ASM705/6/7/8), RESET(ASM707/8, ASM813L)

Package Dimensions

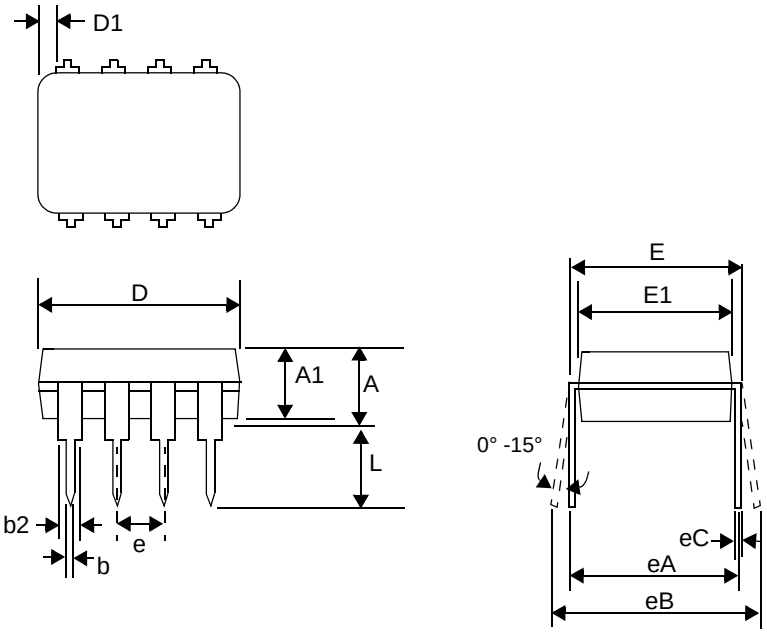
8-Pin MicroSO



	Inches		Millimeteres	
	Min	Max	Min	Max
A	-	0.0433	-	0.10
A1	0.0020	0.0059	0.050	0.15
A2	0.0295	0.0374	0.75	0.95
b	0.0098	0.0157	0.25	0.40
C	0.0051	0.0091	0.13	0.23
D	0.1142	0.1220	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.193 BSC		4.90 BSC	
E1	0.1142	0.1220	2.90	3.10
L	0.0157	0.0276	0.40	0.70
a	0°	6°	0°	6°

Package Dimensions (contd)

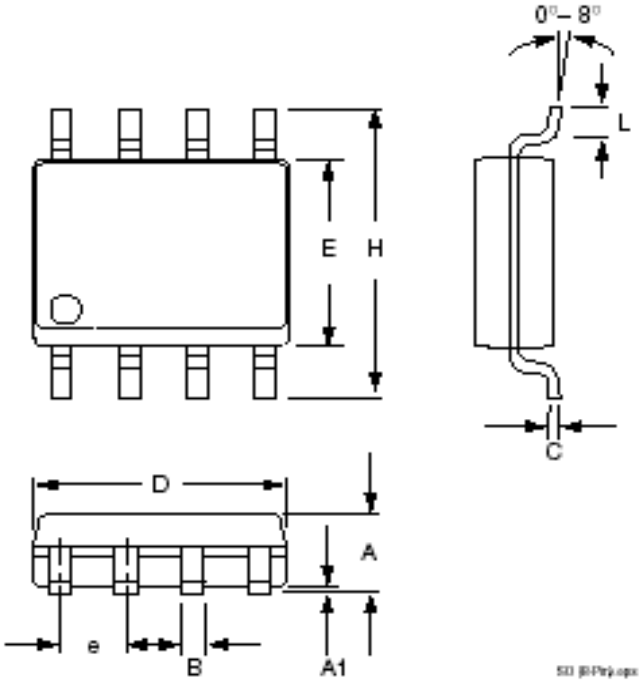
Plastic DIP (8-Pin)



	Inches		Millimeteres	
	Min	Max	Min	Max
A	-	0.210	-	5.33
A1	0.015	-	0.38	-
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	-	0.13	-
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	-	2.54	
eA	0.300	-	7.62	
eB	-	0.430	-	10.92
eC	-	0.060		
L	0.115	0.150	2.92	3.81

Package Dimensions (contd)

SO (8-Pin)



	Inches		Millimeteres	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	2.00

rev 1.2

Ordering Codes

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package
ASM705 Active LOW Reset, Watchdog Output And Manual RESET			
ASM705CPA	4.65	0°C to +70 °C	8-Plastic DIP
ASM705CSA	4.65	0°C to +70 °C	8-SO
ASM705CUA	4.65	0°C to +70 °C	8-MicroSO
ASM705EPA	4.65	-40°C to +85°C	8-Plastic DIP
ASM705ESA	4.65	-40°C to +85°C	8-SO
ASM705EUA	4.65	-40°C to +85°C	8-MicroSO
ASM706 Active LOW Reset, Watchdog Output And Manual RESET			
ASM706CPA	4.40	0°C to +70 °C	8-Plastic DIP
ASM706CSA	4.40	0°C to +70 °C	8-SO
ASM706CUA	4.40	0°C to +70 °C	8-MicroSO
ASM706EPA	4.40	-40°C to +85°C	8-Plastic DIP
ASM706ESA	4.40	-40°C to +85°C	8-SO
ASM707 Active LOW & HIGH Reset with Manual RESET			
ASM707CPA	4.65	0°C to +70 °C	8-Plastic DIP
ASM707CSA	4.65	0°C to +70 °C	8-SO
ASM707CUA	4.65	0°C to +70 °C	8-MicroSO
ASM707EPA	4.65	-40°C to +85°C	8-Plastic DIP
ASM707ESA	4.65	-40°C to +85°C	8-SO
ASM708Active LOW & HIGH Reset with Manual RESET			
ASM708CPA	4.40	0°C to +70 °C	8-Plastic DIP
ASM708CSA	4.40	0°C to +70 °C	8-SO
ASM708CUA	4.40	0°C to +70 °C	8-MicroSO
ASM708EPA	4.40	-40°C to +85°C	8-Plastic DIP
ASM708ESA	4.40	-40°C to +85°C	8-SO
ASM813L Active HIGH Reset, Watchdog Output And Manual RESET			
ASM813LCPA	4.65	0°C to +70 °C	8-Plastic DIP
ASM813LCSA	4.65	0°C to +70 °C	8-SO
ASM813LCUA	4.65	0°C to +70 °C	8-MicroSO
ASM813LEPA	4.65	-40°C to +85°C	8-Plastic DIP
ASM813LESA	4.65	-40°C to +85°C	8-SO

Feature Summary

	ASM705	ASM706	ASM707	ASM708	ASM813L
Power fail detector	◆	◆	◆	◆	◆
Brownout detection	◆	◆	◆	◆	◆
Manual RESET input	◆	◆	◆	◆	◆
Power-up/down RESET	◆	◆	◆	◆	◆
Watchdog Timer	◆	◆			◆
Active HIGH RESET output			◆	◆	◆
Active LOW RESET output	◆	◆	◆	◆	
RESET Threshold (V)	4.65	4.40	4.65	4.40	4.65

Alliance Semiconductor Corporation
2575, Augustine Drive,
Santa Clara, CA 95054
Tel: 408 - 855 - 4900
Fax: 408 - 855 - 4999
www.alsc.com

Part Number:ASM705 / 706 / 707 / 708
ASM813L
Document Version: 1.2