7 + 2 Phase Output Controller with SVID Interface for Notebook and Ultrabook CPU Applications

ASP1900A/B

The ASP1900 is a dual rail, seven plus two phase buck solution optimized for Intel's IMVP8 CPUs. The multi−phase rail control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing. This provides an ultra−fast initial response to dynamic load events and reduced system cost. The ASP1900 has an ultra−low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

Features

- Vin Range 9 V to 20 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable Vboot
- High Impedance Differential Output Voltage Amplifier
- Dynamic Reference Injection
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Adjustable Switching Frequency Range
- Digitally Stabilized Switching Frequency
- UltraSonic Operation
- PSYS Input Monitor (SVID address 0D)
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- Meets Intel's IMVP8 Specifications
- SVID and SMBus Control Interface
- This is a Pb−Free Device

Typical Applications

- Desktop
- Channel Motherboard

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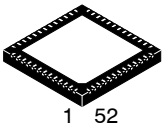
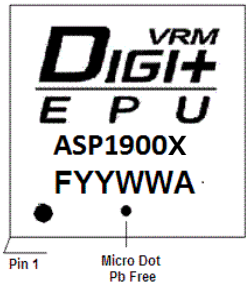


QFN52 6x6, 0.4P
CASE 485BE

MARKING DIAGRAM



X = Specific Device Code (A/B)
F = FAB Location
YY = Year of Production
WW = Work Week Number
A = Assembly Site
• = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
ASP1900AMNTXG	QFN52	2500 / Tape & Reel
ASP1900BMNTXG		

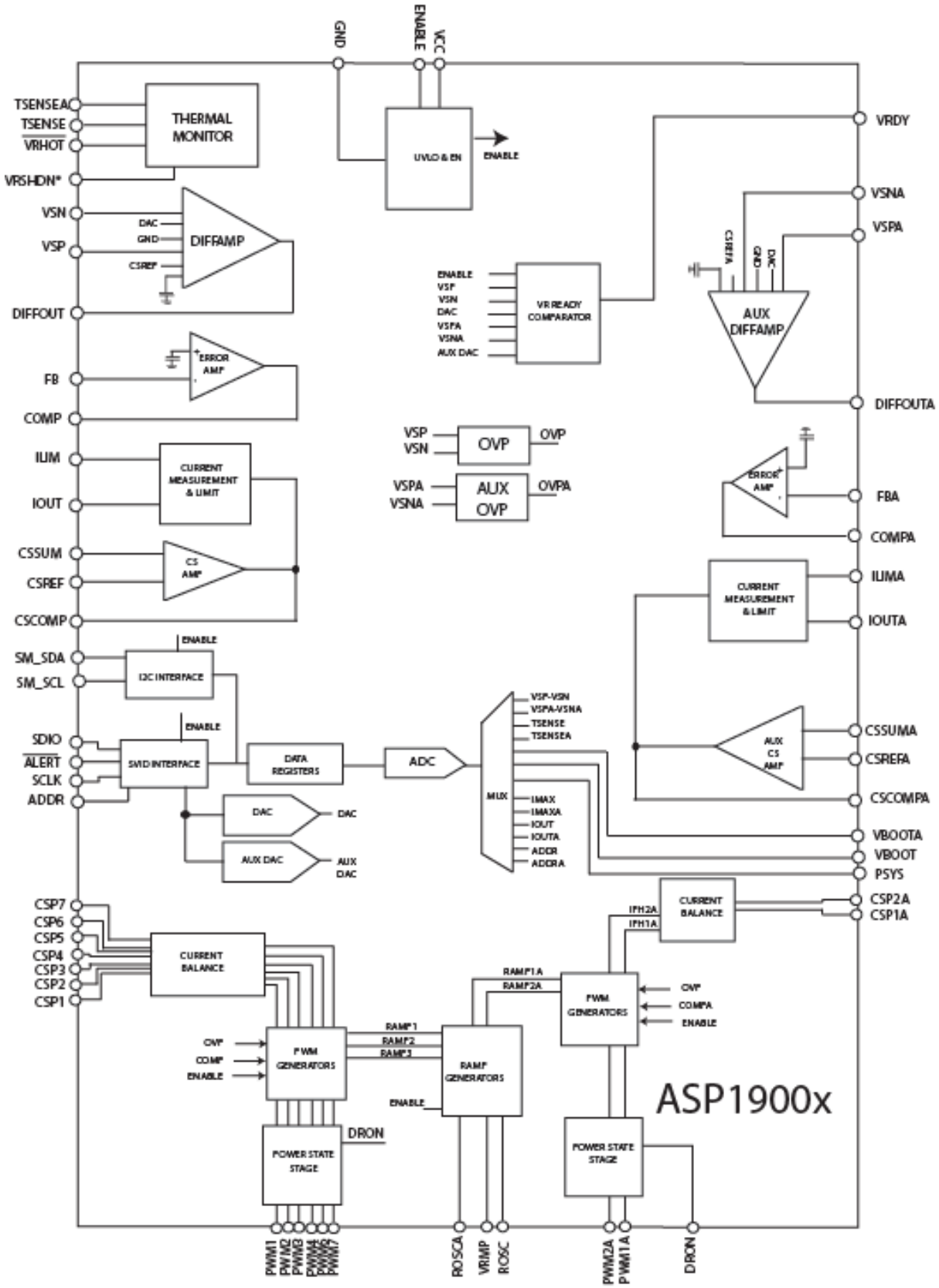


Figure 1. Internal Block Diagram

APPLICATIONS INFORMATION

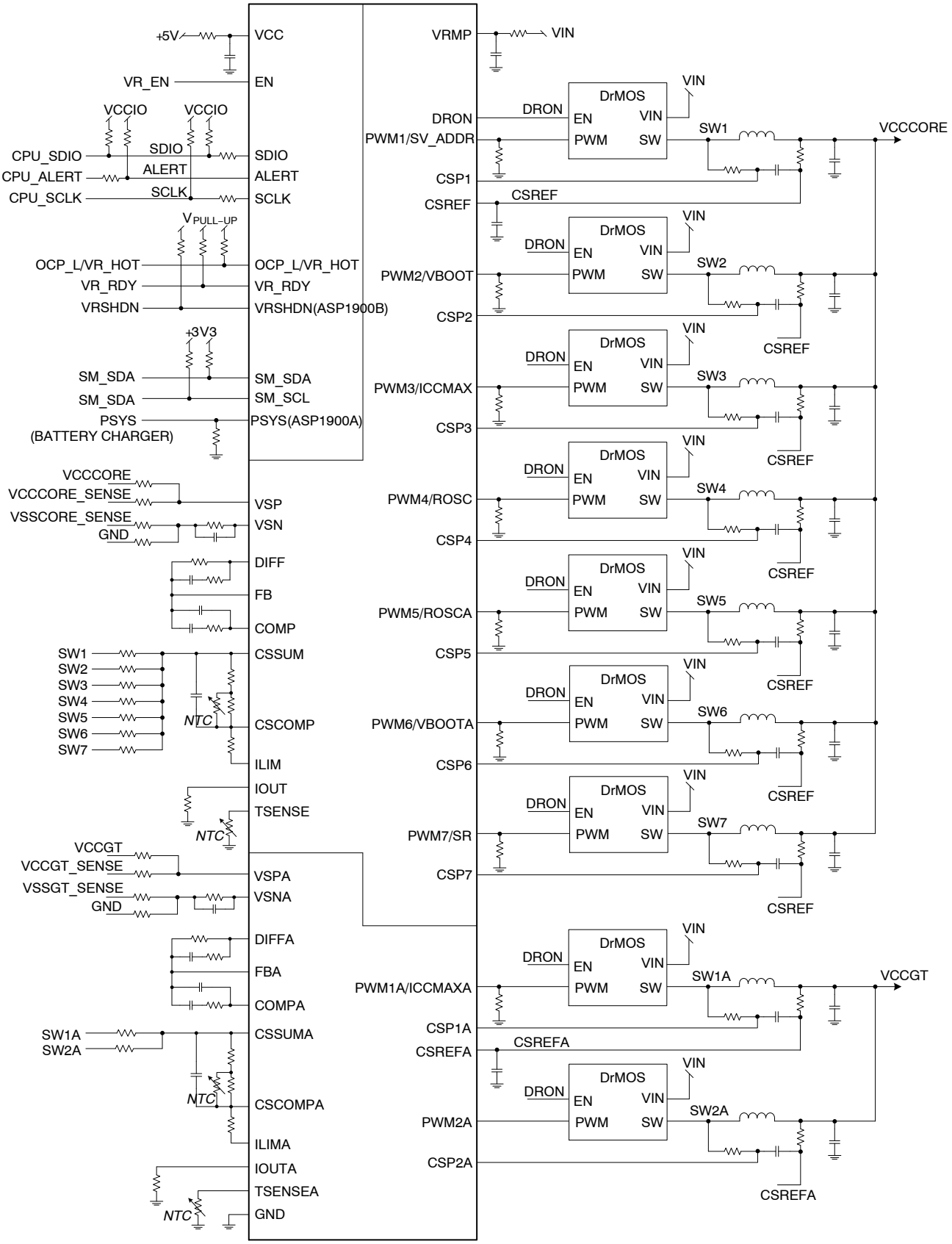


Figure 2. Typical Application Circuit

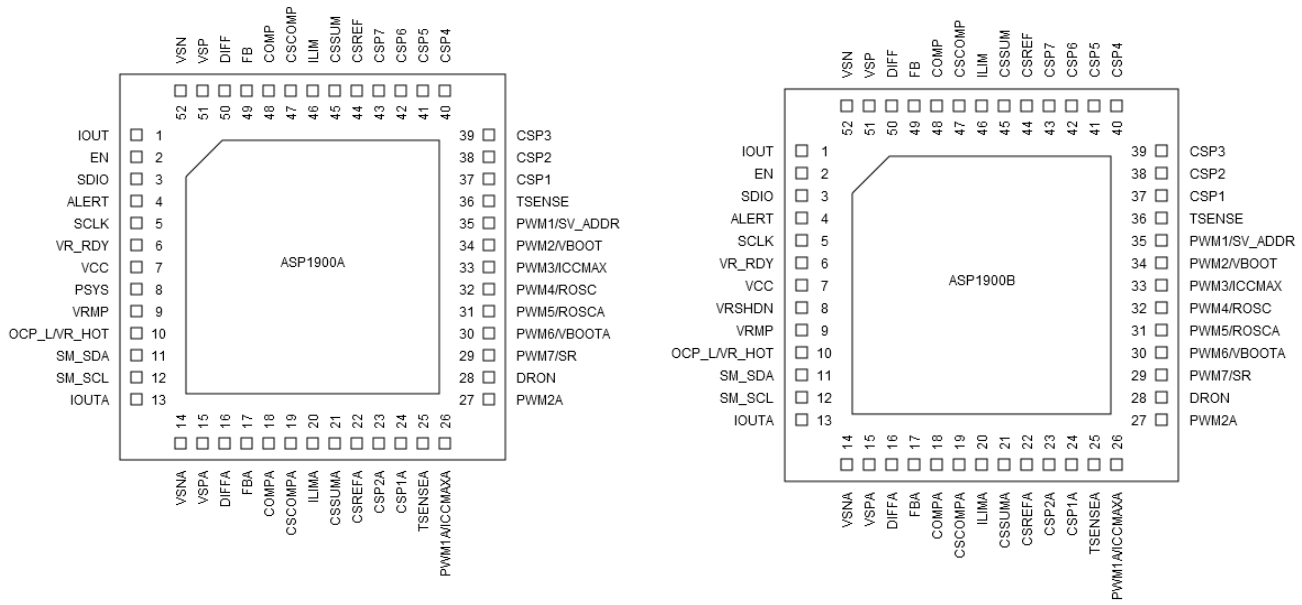


Figure 3. Pinout

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	IOUT	Total output current monitor for seven−phase regulator
2	EN	Enable. High enables both rails
3	SDIO	Serial VID data interface
4	ALERT#	Serial VID ALERT#
5	SCLK	Serial VID clock
6	VR_RDY	VR_RDY indicates both rails are ready to accept SVID commands
7	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
8	PSYS / VRSHDN	ASP1900A: System power signal input. A resistor to ground scales this signal ASP1900B: OD output, pulled and latched low until power off if VR temp reaches programmed level
9	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes
10	OCP_L/VRHOT#	OD output. Indicates high VR temperature, or OCP_L threshold crossed. OCP_L need to enable by SMBus.
11	SM_SDA	SMBus serial data interface
12	SM_SCL	SMBus clock
13	IOUTA	Total output current monitor for two−phase regulator
14	VSNA	Differential output voltage positive sense for two−phase rail
15	VSPA	Differential output voltage negative sense for two−phase rail
16	DIFFA	Output of the two−phase regulator's differential remote sense amplifier
17	FBA	Error amplifier voltage feedback for two−phase regulator
18	COMPA	Output of the error amplifier and the inverting inputs of the PWM comparators for two−phase regulator
19	CSCOMPA	Output of total−current−sense amplifier for two−phase regulator
20	ILIMA	Over−current threshold setting − programmed with a resistor to CSCOMPA for two−phase regulator
21	CSSUMA	Inverting input of total−current−sense amplifier for two−phase regulator
22	CSREFA	Total−current−sense amplifier reference voltage input for two−phase regulator
23	CSP2A	Non−inverting input to current−balance amplifier for Phase 2 of two−phase regulator. Pullup on this pin to disable phase Phase2A
24	CSP1A	Non−inverting input to current−balance amplifier for Phase 1 of two−phase regulator.
25	TSENSEA	Temperature sense input for two−phase regulator
26	PWM1A / ICCMAXA	PWM1 output for two−phase regulator. During startup, ICCMAX for two−phase regulator is programmed with a pull−down resistor
27	PWM2A	PWM2 output for two−phase regulator.
28	DRON	External FET driver enable for discrete driver or ONSemi DrMOS
29	PWM7/SR	PWM7 output for seven−phase regulator / Pin−program for slew−rate control.
30	PWM6/VBootA	PWM6 output for seven−phase regulator / Pin−program for two−phase Vboot. Can be overridden if SMBus transaction occurs between UVLO and EN.
31	PWM5/ROSCA	PWM5 output for seven−phase regulator / Pulldown on this pin programs RoscA value for GT rail
32	PWM4 / ROSC	PWM4 output for seven−phase regulator / Pulldown on this pin programs Rosc value for main rail
33	PWM3 / ICCMAX	PWM3 output for seven−phase regulator / Pulldown on this pin programs ICCMAX for seven−phase rail during startup
34	PWM2 / VBOOT	PWM2 output for seven−phase regulator / Pin−program for seven−phase Vboot. Can be overridden if SMBus transaction occurs between UVLO and EN.
35	PWM1 / SV_ADDR	PWM1 output for seven−phase regulator / Pulldown on this pin configures SVID address
36	TSENSE	Temperature sense input for seven−phase regulator

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Pin Name	Description
37	CSP1	Differential current sense positive for Phase 1 of seven−phase rail
38	CSP2	Differential current sense positive for Phase 2 of seven−phase rail
39	CSP3	Differential current sense positive for Phase 3 of seven−phase rail
40	CSP4	Differential current sense positive for Phase 4 of seven−phase rail
41	CSP5	Differential current sense positive for Phase 5 of seven−phase rail
42	CSP6	Differential current sense positive for Phase 6 of seven−phase rail
43	CSP7	Differential current sense positive for Phase 7 of seven−phase rail
44	CSREF	Total−current−sense amplifier reference voltage input for seven−phase rail
45	CSSUM	Inverting input of total−current−sense amplifier for seven−phase rail
46	ILIM	Over−current threshold setting − programmed with a resistor to CSCOMP for seven−phase rail
47	CSCOMP	Output of total−current−sense amplifier for seven−phase rail
48	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for seven−phase rail
49	FB	Error amplifier voltage feedback for seven−phase rail
50	DIFF	Output of the seven−phase regulator's differential remote sense amplifier
51	VSP	Differential output voltage sense positive for seven−phase rail
52	VSN	Differential output voltage sense negative for seven−phase rail
	Flag	GND

ABSOLUTE MAXIMUM RATINGS (Note1)

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWMX	VCC + 0.3 V	−0.3 V		1 mA
VSN_MPH	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
DIFFOUT_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	2 mA	
VCC	6.0 V	−0.3 V		
VRMP	25 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
VCC Voltage Range	VCC	4.75	5.25	V
Operating Junction Temperature Range (Note 2)	T_J	−10	125	°C
Operating Ambient Temperature Range	T_A	−10	100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. JEDEC JESD 51−7 with 0 LFM.

THERMAL CHARACTERISTICS

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package (Note 3)	R_{JA}	68	°C/W
Maximum Storage Temperature Range	T_{STG}	− 40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10° < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Voltage Range		4.75		5.25	V
Quiescent Current (PS0, 1)	PS0,1			60	mA
	PS2			60	mA
	PS3			27	mA
	PS4		190		μA
	Enable low		5		mA
UVLO Threshold	VCC rising			4.6	V
	VCC falling	3.9			V
VRMP					
Supply Range		9		20	
UVLO Threshold	VRMP Rising			8	V
	VRMP Falling	6			V
UVLO Hysteresis			800		mV
ENABLE INPUT					
Upper Threshold	Activation Level	0.8			V
Lower Threshold	Deactivation Level			0.3	V
PHASE DETECTION					
CSP Pin Pulldown Current	Pulldown applied only prior to soft start		5		μA
CSP Pin Threshold Voltage		VCC−0.4			V
Phase Detect Timer			100		μs
IMVP8 DAC (PROT 05H)					
System Voltage Accuracy	0.75 V ≤ DAC < 1.52 V	−0.5		0.5	%
	0.5 V< DAC < .745 V	−8		8	mV
	0.25 V < DAC < 0.495 V	−10		10	mV
DAC SLEW RATE					
Soft Start Slew Rate			1/2 fast		mV/μs
Slew Rate Slow			1/2 fast		mV/μs
Slew Rate Fast			>10		mV/μs
VOFS Slew Rate			1/2 fast		mV/μs
DRON					
Output High Voltage	Sourcing 500 μA	3			V
Output Low Voltage	Sinking 500 μA			0.1	V
TSENSE					
VR_Hot Assert Threshold			199		mV
VR_Hot De−Assert Threshold			205		mV
Alert# Assert Threshold			205		mV
Alert# De−Assert Threshold			211		mV
VRSHDN Rising Threshold		142	157	172	mV
VRSHDN De−Assert Threshold			163		mV
Bias Current			500		μA

3. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM.
4. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated: −10° < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
VR_RDY OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = −4 mA		0.3		V
OVP AND UVP					
Absolute Over Voltage Threshold	During Soft Start − CSREF Rising		2.5		V
Over Voltage Threshold Above DAC	VSP−VSN−VID Rising	350	400	475	mV
Over Voltage Delay	VSP−VSN Rising to PWM Low		50		ns
Under Voltage Threshold Below DAC−DROOP (VUVM)	VSP−VSN−VID Falling	370		425	mV
Under Voltage Delay			5		μs
PWM OUTPUT					
Output High Voltage	Sourcing 500 μA	Vcc−0.2			V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA			0.7	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		−400		400	nA
−3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ		12		MHz
Closed Loop DC Gain	VSP − VSN = −0.3 V to 1.3 V		1		V/V
CURRENT SUMMING AMPLIFIER					
Input Bias Current	CSSUM = CSREF = 1.0 V	−14		14	μA
Offset Voltage (Vos) (Note 5)		−300		300	μV
Open Loop Gain			80		dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ		10		MHz
CURRENT BALANCE AMPLIFIERS					
Differential Mode input Voltage Range	CSREF = 1.2 V	−30		30	mV
−3 dB Bandwidth	Guarantee by Simulation		8		MHz
OVER−CURRENT PROTECTION					
ILIM Threshold Current (delayed OCP shutdown)	PS0	8	9	10	μA
	PS1, PS2, PS3		9/N*		μA
ILIM Threshold Current (immediate OCP shutdown)	PS0	11	13	15.5	μA
	PS1, PS2, PS3		13/N*		μA
Shutdown Delay	Immediate		300		ns
	Delayed		20		μs
ILIM Output voltage offset	ILIM to CSREF	−4		4	mV
IOUT OUTPUT					
Current Gain	IOUT/ILIM, (RLIM = 20 kΩ, RIOUT = 5 kΩ) DAC = 0.8 V, 1.25 V, 1.5 V	9.5	10	10.5	A/A

* N is the phase configuration number in PS0.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated: −10° < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
MODULATORS					
PWM Ramp Duty Cycle Matching	Comp = 2 V, PWM Ton Matching		±1		%
PSYS					
Full Scale Input Voltage			2.5		V
Disable Threshold			VCC−0.2		V
ADC Resolution			9.80		mV/LSB
Register Update Interval			145		μs
VRSHDN					
VOL				0.3	V
Output Leakage Current When High	High Impedance State	−1.0		1.0	μA
I²C					
V_{IH} (SM_SDA, SM_SCL)	Logic High Input Voltage	2.1			V
V_{IL}	Logic Low Input Voltage			0.8	V
Hysteresis			80		mV
V_{OL} (SM_SDA)	SM_SDA Output Low Voltage, ISDA = −6 mA			0.4	V
V_{IH};I_{IL}	Input Current	−1		1	μA
C_{SM_SDA, SM_SCL}	Input Capacitance		5		pF
f_{SM_SCL}	Clock Frequency			1	MHz
SM_SCL Falling Edge to SM_SDA Valid Time				1	μs
SCLK, SDIO					
VIL				0.45	V
VIH		0.65			V
VOL				0.3	V
Output Leakage Current When High		−0.5		0.5	μA
ALERT#					
VOL				0.3	V
Output Leakage Current When High		−0.1		0.1	μA
OSCILLATOR					
Minimum Switching Frequency			180		kHz
Maximum Switching Frequency			1170		kHz
Switching Frequency Accuracy	Multiphase Rail Dual Edge Operation 180 kHz < F_{SW} < 1170 kHz	−10		10	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Timing Diagrams

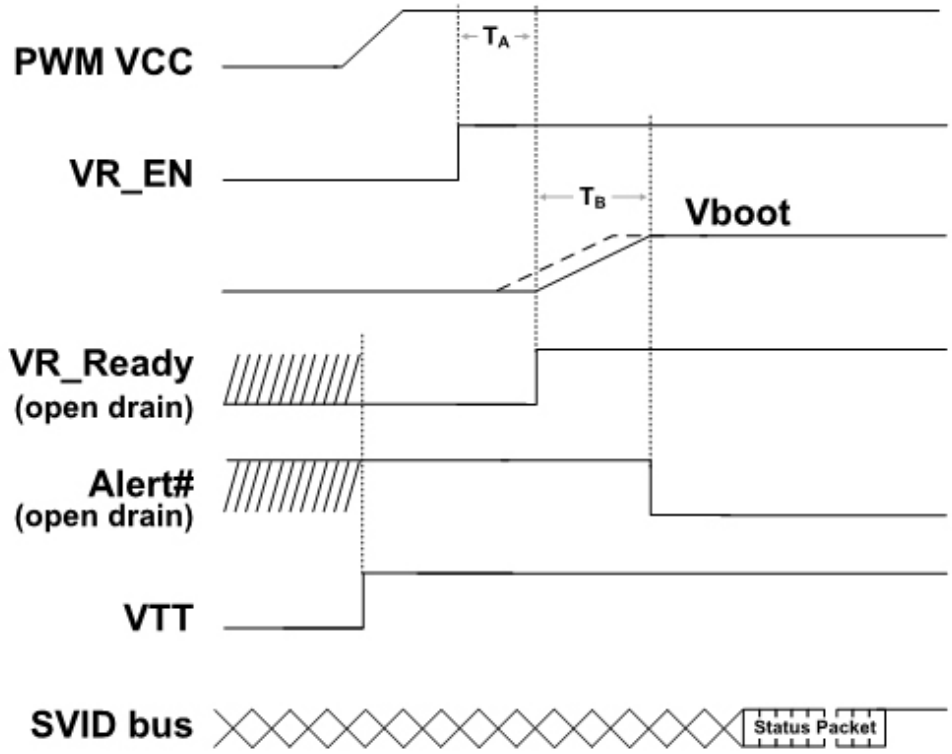


Figure 4. Start−up Timing Diagram − Non Zero V_{BOOT}

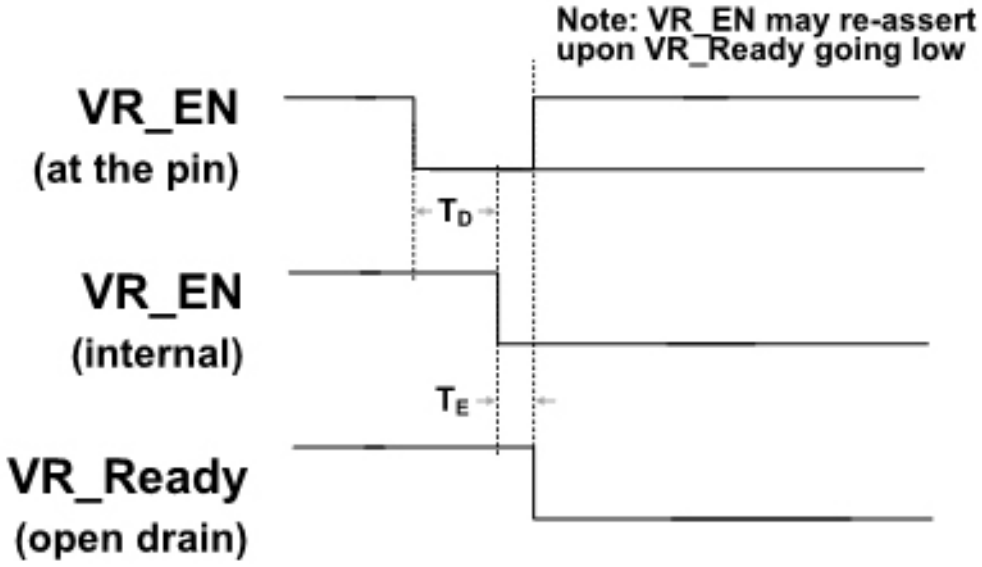


Figure 5. Shut−down Timing Diagram

Description		Min	Typ	Max
TA	VR_EN to VR_Ready. Controller ready accept SVID command			2.5 ms
TB	Non−zero VBOOT ramp time. May start during TA but not later than at the end of TA − to Alert# assertion.			VID/Slow
TD	External de−assertion of VR_EN to the internal recognition of VR_EN de−assertion (glitch filter)	0 μs		1 μs
TE	VR_EN internal de−assertion to VR_Ready de−assertion			500 ns

Table 1. SMBUS START−UP TIMING

Parameter (Note 5)	T_{MIN}	T_{MAX}	Unit	Description
f_{SCLK}		400	kHz	Clock Frequency
t_{LOW}	1.3		μs	Clock low period, between 10% points
t_{HIGH}	0.6		μs	Clock high period, between 90% points
t_R		300	ns	Clock/data rise time
t_F		300	ns	Clock/data fall time
$t_{SU;STA}$	600		ns	Start condition setup time
$t_{HD;STA}$ (Note 6)	600		ns	Start condition hold time
$t_{SU;DAT}$ (Note 7)	100		ns	Data setup time
$t_{SU;STO}$ (Note 8)	600		ns	Stop condition setup time
t_{BUF}	1.3		μs	Bus free time between stop and start conditions

5. Guaranteed by design, but not production tested.
6. Time from 10% of S_{DATA} to 90% of S_{CLK}.
7. Time for 10% or 90% of S_{DATA} to 10% of S_{CLK}.
8. Time for 90% of S_{CLK} to 10% of S_{DATA}.

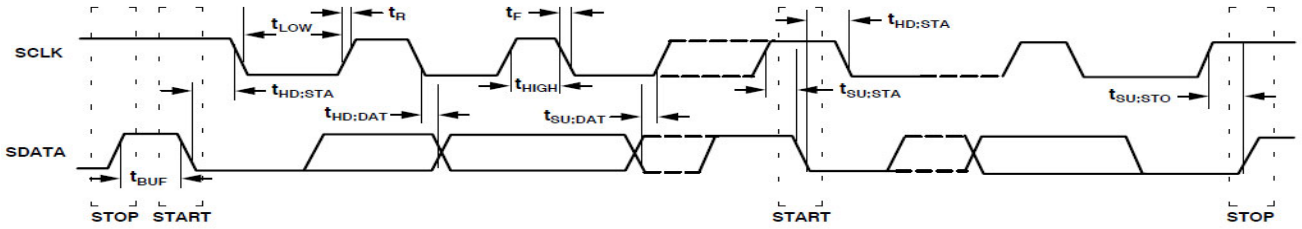


Figure 6. SMBus Timing Diagram

Start Up

Following the rise of VCC above the UVLO threshold, externally programmed configuration data is collected, and all PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRON is asserted (high) to activate the external gate drivers. A digital counter steps the DAC up from zero to the target boot voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced. When the controller is disabled, the PWM signals return to Mid−level. The VR_RDY signal is asserted when the controller is ready to accept the first SVID command.

DEVICE CONFIGURATION

Phase and Rail Configuration

During start−up, the number of operational phases of the multiphase rail is determined by the internal circuitry monitoring the CSP inputs. If a reduced phase count is required the appropriate CSP pins externally pulled to VCC with a resistor during startup. Also, whether or not the PSYS function is active and responds to an address call on the SVID bus is determined by the internal circuitry monitoring the PSYS input. Tying the PSYS input to VCC will cause the PSYS rail to not respond to any calls to address 0Dh on the SVID bus.

ASP1900 Configurations

The ASP1900 has four Configuration features. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- SVID Address
- Slew Rate
  - Programs the slew rate of V_{BOOT} on power up
- Switching Frequency
  - The Fsw values are shown in Table 2
- V_{BOOT}
  - V_{BOOT} options are shown in Table 4 & Table 5

Switching Frequency

Switching frequencies between 180 kHz and 1.17 MHz are programmed at startup with pulldown resistors on Rosc pin (please see pinout for pin number).

Table 2. SWITCHING FREQUENCY

Resistor (kΩ)	Switching frequency (kHz)
10	180 (Default)
15	225
21	270
26.7	315
33.2	360
41.2	405
49.9	450
60.4	495
71.5	540
84.5	630
97.6	720
115	810
133	900
154	990
178	1080
210	1170

Table 3. V_{BOOT}

Resistor (kΩ)	VBOOT(V)
10	0
30	0.8
60	1.05
100	1.2
160	1.4
220	1.5

Table 4. SLEW RATE

Resistor (kΩ)	Slew rate of Vcore and GT (mV/μs)
10	10
30	30

Table 5. SVID ADDRESS

Resistor (kΩ)	“main” SVID address	“A” address
10	0 (Core)	1 (GT)
25	1 (GT)	0 (Core)
45	0 (Core)	2 (SA)
70	1 (GT)	3 (GTUS)
95	0 (Core)	1 (GT)
125	1 (GT)	0 (Core)
165	0 (Core)	2 (SA)
220	1 (GT)	3 (GTUS)

ICCMAX

The SVID interface provides the platform ICCMAX value at register 21h. A resistor to ground on the ICCMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10 k.

$$ICC\_MAX_{21h} = \frac{R \times 10\ \mu A \times 255\ A}{2.5\ V}$$

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

CCM/DCM Operation

In PS0, all rails operate in Continuous Conduction Mode (CCM) which uses the dual−edge control methodology. However, if PS0 is configured as one−phase instead of multi−phase, the control methodology changes to RPM operation. RPM has great transient performance in one−phase CCM operation. The RPM frequency average DC value is targeted to be similar to the PS0 Dual Edge frequency. However, the switching frequency of RPM depends on input voltage, output voltage, load current, inductor value, and output capacitor value. In PS1, all rails operate in one−phase CCM RPM. In PS2 and PS3, all rails operate in either CCM or Discontinuous Conduction Mode

(DCM). It depends on load current in order to prevent loss of efficiency from negative inductor current.

Table 6. POWER STATES

SVID Power State	Typical Operating Mode
PS0	Multiphase rail dual edge
PS1	One−phase CCM RPM
PS2	One−phase DCM RPM
PS3	One−phase DCM RPM
PS4	Standby

PSYS

The PSYS pin is an analog input to the VR controller. It is a system input power monitor that facilitates the monitoring of the total platform system power. The system power is sensed at the platform charging device, the VR controller facilitates reporting back current and through the SVID interface at address 0Dh.

THEORY OF OPERATION

Input Voltage Feed−Forward (VRMP Pin)

Ramp generator circuits are provided for the dual−edge modulator. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled. For multi−phase operation, the dual−edge PWM ramp amplitude is changed according to the following:

$$VRMP\_pp = 0.1 \times Vvrmp$$

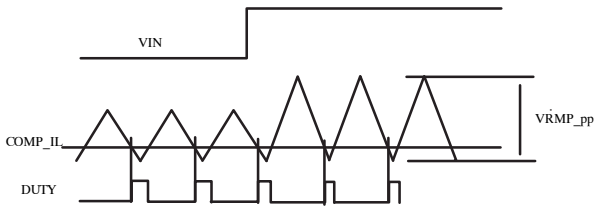


Figure 7. Ramp Feed Forward

Differential Current Feedback Amplifiers

Each phase of the rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 k to avoid offset due to leakage current.

It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance.

The external filter RCSN and CCSN time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

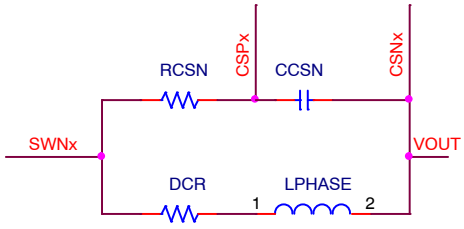


Figure 8. Per Phase Current Sense Network

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \times DCR}$$

Total Current Sense Amplifier

The multiphase rail uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The Rref(n) resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The Rph resistors sum currents from the switch nodes to the virtual CSREF potential created at the CSSUM pin by the amplifier. The total current signal is the difference between the CSCOMP and CSREF voltages.

The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. The Phase 1 inductor is chosen for the thermistor location so that the temperature of the inductor providing current in the PS1 power mode.

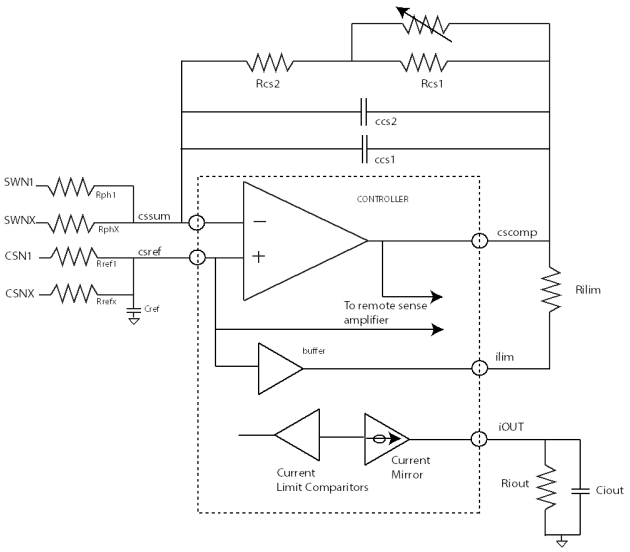


Figure 9. Total Current Sense Amplifier

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot (Iout_{Total} \cdot DCR)$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline. The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$F_z = -\frac{(DCR@25°C)}{(2 \times \pi \times Lphase)}$$

$$F_p = \frac{1}{\left(2\pi \times \left(R_{CS}2 + \left(\frac{R_{CS}1 \times RTH}{R_{CS}1 + RTH}\right)\right) \times (CCs1 + CCs2)\right)}$$

The value of the CREF capacitor (in nF) on the CSREF pin should be:

$$Ccref = \frac{(0.02 \times RTH)}{Rref}$$

Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{DAC}) + (V_{DROOP} - V_{CSREF})$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier.

High Performance Voltage Error Amplifier

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

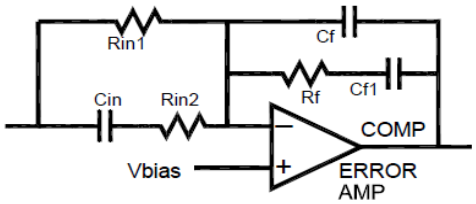


Figure 10. Error Amplifier

Loadline Programming (D_{ROOP})

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

A load line is produced by adding a signal proportional to output load current (VDROOP) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. The load line is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The multiphase rails generates a replica of the CSREF pin voltage at the ILIM pin, and compares ILIM pin current to ICL0 and ICLM0 (ICL1 and ICLM1 in PS1, PS2 and PS3). The controller latches off if ILIM pin current exceeds ICL0 (ICL1 for PS1, PS2, and PS3) for t_OCPDLY, and latches off immediately if ILIM pin current exceeds ICLM0 (ICLM1 for PS1, PS2 and PS3). Set the value of the current limit resistor RLIMIT according to the desired current limit Iout LIMIT.

$$R_{LIMIT} = \frac{\frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot (Iout_{LIMIT} \cdot DCR)}{9\mu \cdot K}$$

where K can be set by 0x19[7:4] for main rail, and set by 0x37[7:4]for aux rail.

Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if desired.

$$R_{IOUT} = \frac{2.5\ V \cdot R_{LIMIT}}{10 \cdot \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot (ICCMAX \cdot DCR)}$$

Programming DAC Feed−Forward Filter

The multiphase rail outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the D_{ROOP} function to current flowing into the charging output capacitors. In the following equations, C_{OUT} is the total output capacitance of the system.

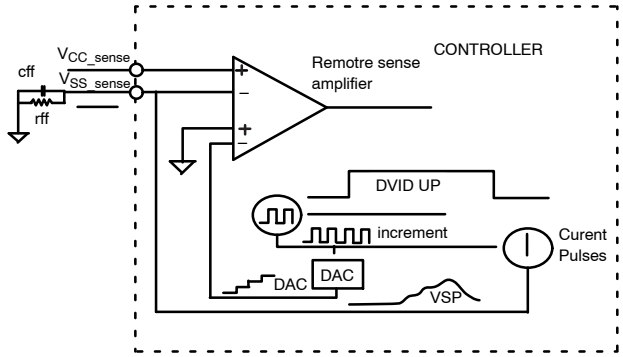


Figure 11. DAC Feed Forward

$$Rff = Cout \times LL \times 453.6 \times 10^{6}$$

$$Cff = \frac{LL \times Cout}{Rff}$$

T_{SENSE} Network

A temperature sense inputs is provided for the multiphase rail. A precision current is sourced out the output of the T_{SENSE} pin to generate a voltage on the temperature sense networks. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. Rcomp1 in the following Figure is optional, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

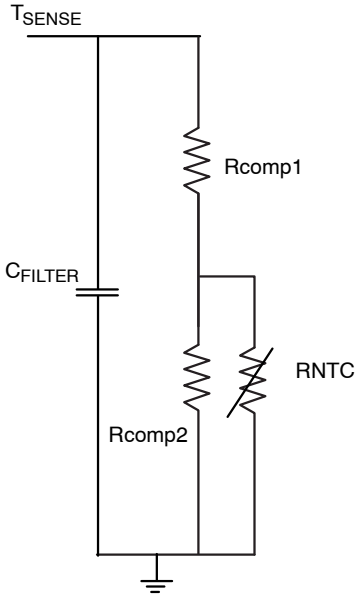


Figure 12. T_{SENSE} Network

PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (IL×DCR×Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output. During steady state PS0 operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

Output Voltage Offset (VOFS)

According to Intel definition, output voltage offset can be implemented through SVID. SMBus also provides flexibility to change VOFS. There are four possibilities to change output voltage offset. For the default setting, VOFS is controlled by SVID. It can also be controlled by SMBus register and ignored SVID setting. When phase shedding feature enable, VOFS can also be adjusted depend on output load.

Table 7. OUTPUT VOLTAGE OFFSET (VOFS) OF IA RAIL

VOFS of IA rail		0x1D[4] OFS Control	
		0 (Follow SVID)	1 (Ignore SVID)
0x1E[5] SMBus VOFS	0 (Disable)	SVID 0x33	SMBus 0x27
	1 (Enable)	SVID 0x33 + SMBus 0x07~0x0A (Depend on phase shedding setting)	SMBus 0x27 + SMBus 0x07~0x0A (Depend on phase shedding setting)

Table 8. OUTPUT VOLTAGE OFFSET (VOFS) OF GT RAIL

VOFS of GT rail		0x39[4] OFS Control	
		0 (Follow SVID)	1 (Ignore SVID)
0x3A[5] SMBus VOFS	0 (Disable)	SVID 0x33	SMBus 0x40
	1 (Enable)	SVID 0x33 + SMBus 0x2B~0x2C (Depend on phase shedding setting)	SMBus 0x40 + SMBus 0x2B~0x2C (Depend on phase shedding setting)

Phase Shedding

The phase shedding feature can be implement by SMBus. For IA−rail, it support three adjustable current threshold, VM0~VM2. And four current stage, LCS0~LCS3, can set each phase number, offset voltage, load−line, and switching frequency. For GT−rail, it support one adjustable current threshold, VM0. And two current stage, LCS0 and LCS1, can also separate their phase number, offset voltage, load−line, and switching frequency.

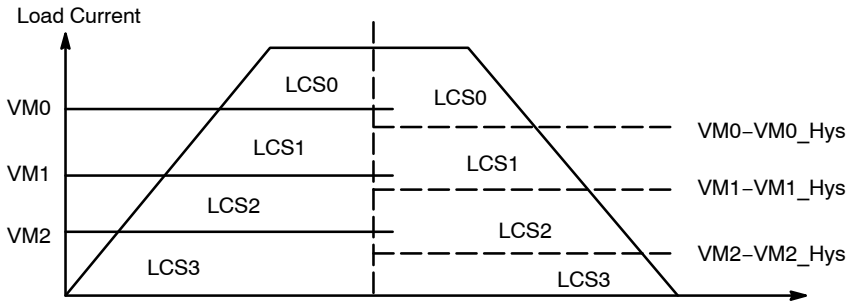


Figure 13. Phase Shedding for IA−Rail

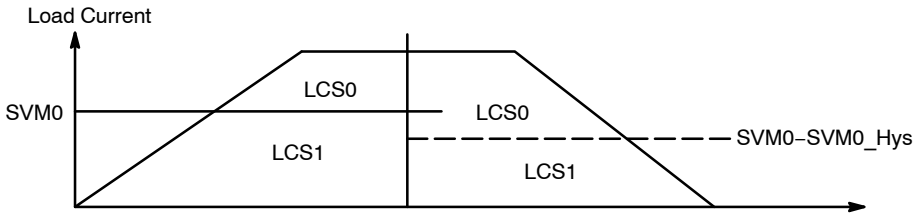


Figure 14. Phase Shedding for GT−Rail

Table 9. PHASE CONFIGURATION

Phase Configuration	Programming Pin in CSPx	Unused Pin
7+2	All CSP pins are connected normally	No unused Pin
7+1	CSP1 to CSP7 and CSP1A pins connected normally. CSP2A connected to VCC through a 2K resistor.	Float PWM2A
6+1	CSP1 to CSP6 and CSP1A pins connected normally. CSP7 and CSP2A connected to VCC through a 2K resistor.	Float PWM2A Use PWM7 for programming SR only.
5+1	CSP1 to CSP5 and CSP1A pins connected normally. CSP6, CSP7, and CSP2A connected to VCC through a 2K resistor.	Float PWM2A Use PWM7 for programming SR only, and PWM6 for programming VBOOTA only.
4+1	CSP1 to CSP4 and CSP1A pins connected normally. CSP5, CSP6, CSP7, andCSP2A connected to VCC through a 2K resistor.	Float PWM2A Use PWM7 for programming SR only, PWM6 for programming VBOOTA only, PWM5 for ROSCA only.

Table 10. PHASE SHEDDING CONFIGURATION

IA Phase Configuration in PS0	IA Rail Phase Configuration when Phase Shedding Enable (SMBus 0x06, IICP0~IICP3)			
	“00”	“01”	“10”	“11”
7	7	4	2	1
6	6	4	2	1
5	5	3	2	1
4	4	3	2	1

FAULT PROTECTION

Over Current Protection (OCP)

A programmable total phase current limit is provided that is decreased when not operating in PS0 mode. This limit is programmed with a resistor between the CSCOMP and ILIM pins. The current from the ILIM pin to this resistor is compared to the ILIM Threshold Currents (ICL0, ICLM0, ICL1, and ICLM1). When the 2−phase rail is operating in PS0, if the ILIM pin current exceeds ICL0, an internal latch−off timer starts.

If the fault is not removed, the controller shuts down when the timer expires. If the current into the pin exceeds ICLM0, the controller shuts down immediately. When operating in PS1, PS2, or PS3, the ILIM pin current limits are ICL1 and ICLM1. To recover from an OCP fault, the EN pin or VCC voltage must be cycled low.

Input Under−voltage Lockouts (UVLO)

The VR monitors the 5 V VCC supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The multiphase phase rail output voltage is monitored for under voltage at the output of the differential amplifier. If the multiphase−phase rail output falls more than VUVM2 below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The multiphase phase output voltage is monitored for OVP at the output of the differential amplifier and also at the CSREF pin. During normal operation, if an output voltage exceeds the DAC voltage by VOVP, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage. At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP Threshold as DAC decreases. When the DAC gets to zero, the PWMs will be held low, and the VR will stay in this mode until the VCC voltage or EN is toggled.

Absolute OVP

During start up, the OVP threshold is set to the Absolute Over Voltage Threshold. This allows the controller to start up without false triggering OVP.

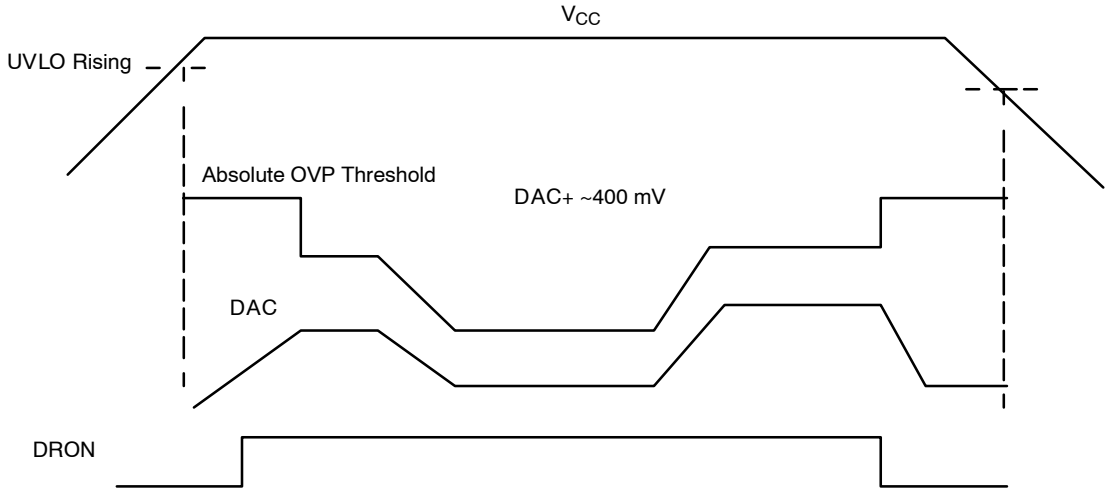


Figure 15. OVP Threshold Behavior

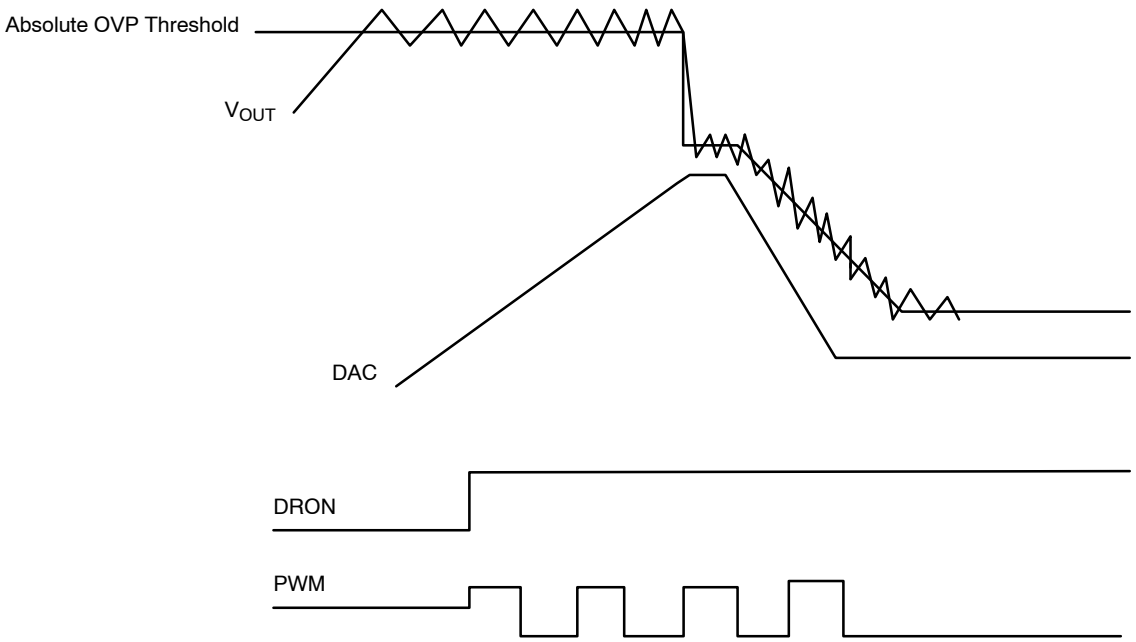


Figure 16. OVP Behavior at Start−up

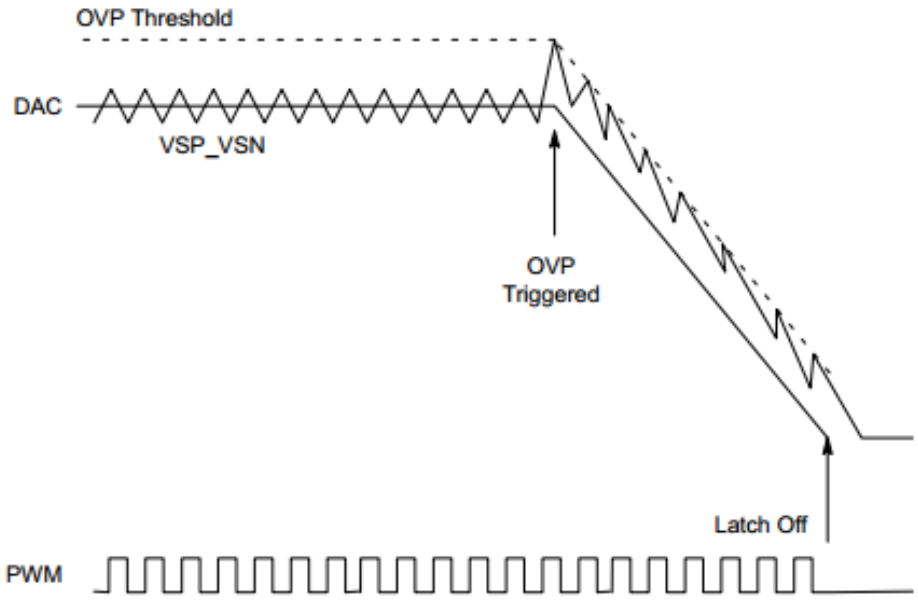


Figure 17. OVP During Normal Operation Mode

Serial VID Interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the VR controller (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT#. The SCLK is unidirectional and generated by the master. The SDIO is bi−directional, used for transferring data from the microprocessor to the VR controller and from the VR controller to the CPU. The ALERT# is an open drain output from the VR controller to signal to the master that the Status Register should be read.

Refer to the relevant Intel document for SVID routing and pull−up topologies.

The SVID bus will operate at a max frequency of 43 MHz.

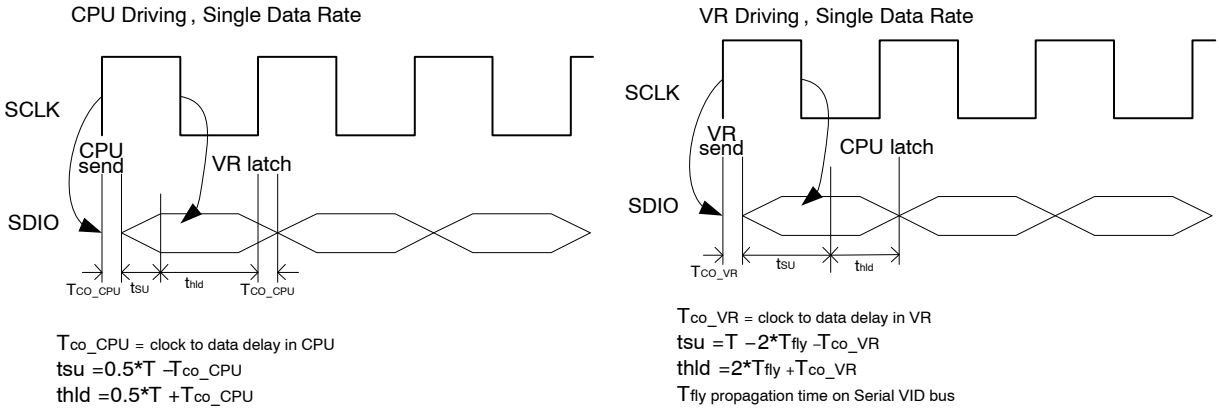


Figure 18. SVID Timing Diagram

Table 11. SLEW RATE

Option	SVID Command Code	Feature Description	Register Address (Indicating the Slew Rate of VID Code Change)
SetVID_Fast	01h	10 mV/μs or 30 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	= 1/2 of SetVID_Fast VID code change slew rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

SMBus (I^2C) Address

In addition to the SVID interface between the CPU and VR, the ASP1900 also supports communication via I^2C over the SMBus. The I^2C interface consists of SM_SDA and SM_SCL. Communication over SMBus can occur once Vcc is ready (even prior to enabling the ASP1900), however, you should wait a min of 5 ms after Vcc is ready before communicating. SMBus slave address is 0x20.

Table 12. SMBUS REGISTER MAP

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR V_{CORE}				
0x01	VM0[7:0]	Current threshold for LCS0 (highest current state) Resolution = (ICCMAX/255) A/bit	R/W	00h
0x02	VM1[7:0]	Current threshold for LCS1 Resolution = (ICCMAX/255) A/bit	R/W	00h
0x03	VM2[7:0]	Current threshold for LCS2 (VM2) Resolution = (ICCMAX/255) A/bit	R/W	00h
0x04	VM1_Hys[6:4] VM0_Hys[2:0]	Bit[6:4]: Set VM1 Hysteresis, 8 steps VM1 Hys = (ICCMAX/100) x (2 + [6:4]) Bit[2:0]: Set VM0 Hysteresis, 8 steps VM0 Hys = (ICCMAX/100) x (2 + [2:0])	R/W	00h
0x05	VM2_Hys[6:4] SVM0_Hys_Arail[2:0]	Bit[6:4]: Set VM2 Hysteresis, 8 steps VM2 Hys = (ICCMAX/100) x (2 + [6:4]) Bit[2:0]: Set SVM0 Hysteresis, 8 steps SVM0 Hys = (ICCMAX/100) x (2 + [2:0])	R/W	00h
0x06	IICP3[7:6] IICP2[5:4] IICP1[3:2] IICP0[1:0]	No. of phases active in each I^2C state Phase count while in I^2C defined states Bit[7:6]: phases on in LCS3 Bit[5:4]: phases on in LCS2 Bit[3:2]: phases on in LCS1 Bit[1:0]: phases on in LCS0 00: 7 phases; 01: 4 phases, 10: 2 phases; 11: 1 phase	R/W	00h
0x07	VOFS0[7:0]	Voltage Offset Adjustment Offsets for I2C states LCS0 – LCS3 (5 mV/step). VOFS is 2's compliment, Bit 7 is sign bit. Voltage change slew rate is SLOW.	R/W	00h
0x08	VOFS1[7:0]		R/W	00h
0x09	VOFS2[7:0]		R/W	00h
0x0A	VOFS3[7:0]		R/W	00h
0x0B	IICF0[7:4] IICF1[3:0]	**Reg Value** **Freq (kHz)** 0000 = 100% 180 (default) 0001 = 125% 225 0010 = 150% 270 0011 = 175% 315 0100 = 200% 360 0101 = 225% 405 0110 = 250% 450 0111 = 275% 495 1000 = 300% 540 1001 = 350% 630 1010 = 400% 720 1011 = 450% 810 1100 = 500% 900 1101 = 550% 990 1110 = 600% 1080 1111 = 650% 1170 IICF0[7:4] = LCS0 operating frequency IICF1[3:0] = LCS1 operating frequency IICF2[7:4] = LCS2 operating frequency IICF3[3:0] = LCS3 operating frequency	R/W	00h
0x0C	IICF2[7:4] IICF3[3:0]		R/W	00h

Table 12. SMBUS REGISTER MAP (continued)

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR V_{CORE}				
0x0D	IICLL0[7:4] IICLL1[3:0]	DC Load Line Adjustment LL adjustment in each I^2C state LCS0 – LCS3 0% – 93.75%, 6.25% steps Default = 50% of externally programmed LL	R/W	88h
0x0E	IICLL2[7:4] IICLL3[3:0]		R/W	88h
0x0F	CB_EN[7] PH1_IGAIN[6:4] PH2_IGAIN[2:0]	Current Balance Gain Adjustment CB_EN[7] = Enable/Disable current balance feature. Enable = 0 (default), Disable = 1 PH1_IGAIN[6:4] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit [3] = Unused PH2_IGAIN[2:0] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x10	PH3_IGAIN[6:4] PH4_IGAIN[2:0]	Current Balance Gain Adjustment PH3_IGAIN[6:4] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit [3] = Unused PH4_IGAIN[2:0] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x11	PH5_IGAIN[6:4] PH6_IGAIN[2:0]	Current Balance Gain Adjustment PH5_IGAIN[6:4] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit [3] = Unused PH6_IGAIN[2:0] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x12	PH7_IGAIN[6:4] Reserved[3:0]	Current Balance Gain Adjustment PH7_IGAIN[6:4] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit [3:0] = Unused	R/W	44h
0x15	LCHVID[7:0]	Latch VID register – default = 1.1 V (Abh) Refer to IMVP8 SVID table. VDAC control by LCHVID when 0x1D[6] = “1”	R/W	ABh
0x16	IOUT[7:0]	Reports Iout	RO	–
0x17	VOUT[7:0]	VCore Voltage Reading VOUT = 2.5 V / 255 * 0x17[7:0] If 0x1E[6] = “0”, VOUT = VDAC If 0x1E[6] = “1”, VOUT = Real Sense Voltage	RO	–

0x18	Protection Indicator[6:0]	Protection Enable/Disable Indicator
		Bit[6] : OCP Indicator
		0 = Not Active; 1 = Active
		Bit[5] : Per phase OCP Indicator
		0 = Not Active; 1 = Active
		Bit[4] : OVP Indicator
		0 = Not Active; 1 = Active
		Bit[3] : UVP Indicator
		0 = Not Active; 1 = Active
		Bit[2:0]: Per phase OCP indicator if Bit[4] = 1
		phase 1 = 001; phase 2 = 010;
		phase 3 = 011; phase 4 = 100;
		phase 5 = 101; phase 6 = 110;
		phase 7 = 111;
			RO	–

Table 12. SMBUS REGISTER MAP (continued)

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR V_{CORE}				
0x19	Total OCP/ OCP_L/OCP_L Hys [7:0]	Total OCP threshold, OCP_L flag assertion level and hysteresis setting OCP[7:4] : Total Current OCP Ratio of ILIM (Over Current Protection) 0000: 50%; 0001: 60%; 0010: 70%; 0011: 80%; 0100: 90% ; 0101: 100%; 0110: 110%; 0111: 120%; 1000: 130%(Default) 1001: 140%; 1010: 150%; 1011: 160%; 1100: 170%; 1101: 180%; 1110: 190%; 1111: 200% OCP_L[3:1] : OCP_L Ratio of ILIM (Over Current Protection) 000: 65%; 001: 70%; 010: 75%; 011: 80%; 100: 85%; 101: 90%(Default); 110: 95%; 111: 100% OCP_L Hys[0] : OCP_L Hysteresis Ratio of ILIM (Over Current Protection) 0: 10% (Default); 1: 20%	R/W	8A
0x1A	IMONOvR/OC/UV/ OV [7:0]	IMONOvR[7]: Overwrite SVID 0x15h (IMON) “1” = Enable ; “0” = Disable IMONOvR[6]: Overwrite SVID 0x15h (IMON) “1” = 1/2 ; “0” = 1/4 OCP[5:4] : Per Phase OCP 00 = 400 mV; 01 = 450 mV (Default); 10 = 600 mV; 11 = 800 mV The lowest threshold for each phase is 400mV/amp gain. The default gain is 6 so this corresponds to ~65 mV across CSP/CSN. Bit[3:2] : UVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV Bit[1:0] : OVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV	R/W	50h
0x1B	OCP_delay [7:0]	OCP Delay Setting – Vcore & Vgt share the same setting OCP_delay[7:5]: Total OCP delay 000 = 5 μs; 001 = 10 μs; 010 = 15 μs; 011 = 20 μs (Default); 100 = 25 μs; 101 = 30 μs; 110 = 35 μs; 111 = 40 μs OCP_delay[4:2]: Per Phase OCP delay 000 = 2 μs; 001 = 4 μs; 010 = 6 μs (Default); 011 = 8 μs; 100 = 10 μs; 101 = 12 μs; 110 = 14 μs; 111 = 16 μs OCP_delay[1:0]: RESERVED	R/W	68h
0x1C	VR_SR[3:0] SVR_SR[7:4]	DVID slew rate. Range is 8–38 mV/μs. 16 steps total, 2 mV/step VR_SR = 8 mV/μs + 0x1C[3:0] × 2 mV/μs SVR_SR = 8 mV/μs + 0x1C[7:4] × 2 mV/μs	R/W	33h

Table 12. SMBUS REGISTER MAP (continued)

<table>
<tr><th>Reg Addr</th><th>Register Name</th><th>Description</th><th>Access</th><th>Default</th></tr>
<tr><td colspan="5">REGISTERS FOR V_{CORE}</td></tr>
<tr><td>0x1D</td><td>Misc1[7:0]</td><td>Bit[7]: Slew Rate Control
0 = Select from pin
1 = Select from register
Bit[6]: VDAC Control
0 = SVID 0x31 VDAC follow SVID
1 = SVID 0x31 VDAC ignore SVID. VDAC control by LCHVID
Bit[5]: PWR State Control
0 = SVID 0x32 PWR state follow SVID
1 = SVID 0x32 PWR state ignore SVID. Phase control by SMBus
Bit[4]: OFS control
0 = SVID 0x33 Offset follow SVID
1 = SVID 0x33 Offset ignore SVID. Offset control by SMBus
Bit[3]: Total OCP Control
0 = Disable Total OCP function (OCPL# = H)
1 = Enable Total OCP function
Bit[2]: Per−phase OCP Control
0 = Disable Per−phase OCP function
1 = Enable Per−phase OCP function
Bit[1]: OVP Control
0 = Disable OVP function (VR_OVP# = H)
1 = Enable OVP function
Bit[0]: UVP Control
0 = Disable UVP function
1 = Enable UVP function
<table>
<tr><th></th><th>1Dh[5]</th><th>1Eh[4]</th></tr>
<tr><td>SVID</td><td>0</td><td>0</td></tr>
<tr><td>SVID</td><td>0</td><td>1</td></tr>
<tr><td>I^2C</td><td>1</td><td>0</td></tr>
<tr><td>I^2C</td><td>1</td><td>1</td></tr>
</table></td><td>R/W</td><td>0Fh</td></tr>
<tr><td>0x1E</td><td>Misc2[7:0]</td><td>Bit[7]: Spread Spectrum “0” to disable (default);
“1” to enable
Bit[6]: VOUT Voltage value select “0” for SVID register;
“1” actual A/D
Bit[5]: Output voltage offset control “0” to disable;
“1” to enable this bit with function after 0x1D[4] = “1”
Bit[4]: Auto phase function control “0” disable;
“1” to enable If Bit[4] is 0, follow IICP0 if 1D[5] = 1;
or follow SVID PS if 1D[5] = 0. This bit with function after 0x1D[5] = “1”
Bit[3]: DCM enable when in 1 phase “0” always CCM;
“1” DCM
Bit[2]: Loadline enable “0” disables LL; “1” enables (default)
Bit[1]: USM/PSM selection when in DCM “1” enables sonic mode
Bit[0]: OCP_L# enable control: “0” to disable; “1” to enable</td><td>R/W</td><td>0Ch</td></tr>
<tr><td>0x1F</td><td>WD[7:5]</td><td>Watchdog timer, (Note: I^2C watchdog timer expires, all I^2C registers return to default settings.)
Bit[7]: 1 = Enable; 0 = Disable
Bit[6]: Reset I^2C registers to default values (except for register 0x1F, this is independent of the watchdog timer).
Bit[5]: Timer
0 = 800 ms ; 1 = 1600 ms</td><td>R/W</td><td>00h</td></tr>
</table>

Table 12. SMBUS REGISTER MAP (continued)

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR V_{CORE}				
0x20	VRSD[7:4] VRSD Hys[3:0]	VR_SHDN# Threshold Setting Bit[7:4]: 16 steps, 2C/step VR_SHDN# = 111°C + Bit[7:4] Temp range = 111°C to 141°C. Default = 125°C Bit[3:0]: Reserved	R/W	70h
0x22	OTPBH[7] OTPEN[6] OCPTH[5] VRHOT#_EN[4] TEMP_VRHOT#[3:0]	Select Behavior or VR_SHDN# Bit[7]: OTP behavior selection 0 = VRSHDN# go low only; 1 = controller shutdown only Bit[6]: OTP function enable/disable 0 = Disable ; 1 = Enable Bit[5]: Total OCP threshold control 0 = Default; 1 = Double Bit[4]: VRHOT# “0” = Enable ; “1” = Disable Note: when VR_HOT is disabled ALERT will not assert and the Temp Status bit (SVID reg 0x10 bit) is not set. Bit[3:0]: SVID 0x12. Temp range from 91°C to 121°C, default = 106°C, 3°C/LSB 0000: No offset ; 0001: offset 1LSB ; 0010: offset 2LSB ; 0011: offset 3LSB; 0100: offset 4LSB ; 0101: offset 5LSB (default) ; 0110: offset 6LSB ; 0111: offset 7LSB ; 1000: offset 8LSB; 1001: offset 9LSB; 1010: offset 10LSB	R/W	05h
0x26	IMON_OFS[7:0]	IMON offset [7:0] (can be positive or negative) SVID 0x15 ± Bit[7:0] I^2C 0x16 ± Bit[7:0]	R/W	00h
0x27	DVID_OFS[7:0]	DVID offset function (positive and negative adjustment) Enable this register after 0x1D[4] = “1”	R/W	00h
0x28	SVID_IVID_En	Bit 7 is for the Core rail, default is IVIDI disable (bit7 = 0) Bit 3 is for the GT rail, default is IVIDI disable (bit3 = 0)	R/W	00h
0x41	Vboot[7:0]	Bit[7]: control setting function (VBOOT) “0” = Disable (follow H/W resistor setting); “1” = Enable (follow I^2C setting) Bit[6:0]: V_{BOOT} voltage from 0 V to 1.515 V, 10 mV/step If 0x41[6:0] = 0, V_{BOOT} = 0 V Others, V_{BOOT} = 255 mV + (0x41[6:0] − 1) * 10 mV	R/W	00h
0x43	TM[7:0]	I^2C Thermal Monitor Value Reading. Temperature reports in degree celsius (°C). To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resister in parallel. NTC uses 10 kΩ under 25°C and B25/50 approximates 3380. Use 732 Ω for parallel resister.	RO	–
0x45	RSVD[7:0]	Offset applied once you cross the high limit threshold in register 50h 5 mV/step, VOFS is 2’s compliment, Bit 7 is sign bit	R/W	00h
0x46	RSVD[7:0]	Offset applied once you cross the low limit threshold in register 51h 5 mV/step, VOFS is 2’s compliment, Bit 7 is sign bit	R/W	00h
0x50	RSVD[7:0]	High limit threshold used for I^2C offset function Refer to IMVP8 VID table.	R/W	00h
0x51	RSVD[7:0]	Low limit threshold used for I^2C offset function Refer to IMVP8 VID table.	R/W	00h
0x52	ROSC_OFFSET_CTRL[7:0]	Bit 7 = 1 (Enable Vcore offset function) Bit 3 = 1 (Enable GT offset function) Bit[6]: Control setting function (ROSC) “0” = Disable (follow H/W resistor setting) “1” = Enable (follow I2C setting) Bit[2]: Control setting function (ROSCA) “0” = Disable (follow H/W resistor setting) “1” = Enable (follow I2C setting)	R/W	00h

Table 12. SMBUS REGISTER MAP (continued)

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR VGT				
0x21	SVRSD[7:4] SVRSD Hys[3:0]	VR_SHDN# Threshold Setting Bit[7:4]: 16 steps, 2C/step VR_SHDN# = 111°C + Bit[7:4] Temp range = 111°C to 141°C. Default = 125°C Bit[3:0]: Reserved	R/W	70h
0x29	SVM0[7:0]	Current Threshold for SLCS0(SVM0) Resolution = (ICCMAX / 255) A/bit	R/W	00h
0x2A	SIICP1[1]; SIICP0[0]	No. of phases active in each I^2C state Bit[7:2]: Reserved Bit[1]: Phase Number of LCS1 Bit[0]: Phase Number of LCS0 0: 2 Phase, 1: 1 Phase	R/W	2Ah
0x2B	SVOFS0[7:0]	Offsets for I2C states LCS0 – LCS1 (5 mV/step) SVOFS is 2's compliment, Bit 7 is sign bit. Voltage change slew rate is SLOW.	R/W	00h
0x2C	SVOFS1[7:0]		R/W	00h
0x2D	SIICF0[7:4] SIICF1[3:0]	**Reg Value** / **Freq (kHz)** 0000 = 100% / 180 (default) 0001 = 125% / 225 0010 = 150% / 270 0011 = 175% / 315 0100 = 200% / 360 0101 = 225% / 405 0110 = 250% / 450 0111 = 275% / 495 1000 = 300% / 540 1001 = 350% / 630 1010 = 400% / 720 1011 = 450% / 810 1100 = 500% / 900 1101 = 550% / 990 1110 = 600% / 1080 1111 = 650% / 1170 SIICF0[7:4] = LCS0 operating frequency SIICF1[3:0] = LCS1 operating frequency	R/W	00h
0x2E	SIICLL0[7:4] SIICLL1[3:0]	DC Load Line Adjustment LL adjustment in each I^2C state LCS0LCS1 0% 93.75%, 6.25% steps Default = 50% of externally programmed LL	R/W	88h
0x2F	CB_EN[7] SPH1_IGAIN[6:4] SPH2_IGAIN[2:0]	Current Balance Gain Adjustment Adjustment CB_EN[7] = Enable/Disable current balance feature. Enable = 0 (default), Disable = 1. PH1_IGAIN[6:4] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit [3] = Unused PH2_IGAIN[2:0] = 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x33	SLCHVID[7:0]	Vgt Latch VID Register. Default = 1.1 V (Abh) Refer to IMVP8 SVID table. VDAC control by SLCHVID when 0x39[6] = "1"	R/W	ABh

Table 12. SMBUS REGISTER MAP (continued)

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR VGT				
0x34	SIOUT[7:0]	Reports Real Iout	RO	–
0x35	SVOUT[7:0]	Vgt Voltage Reading SVOUT = 2.5 V / 255 * 0x35[7:0] If 0x3A[6] = “0”, SVOUT = VDAC If 0x3A[6] = “1”, SVOUT = Real Sense Voltage	RO	–
0x36	SProtection Indicator[5:0]	Bit[5] : OCP Indicator “0” = Not Active “1” = Active Bit[4] : Per phase OCP Indicator “0” = Not Active “1” = Active Bit[3] : OVP Indicator “0” = Not Active “1” = Active Bit[2] : UVP Indicator “0” = Not Active “1” = Active Bit[1:0]: Per phase OCP indicator if Bit[4] = 1 Phase 1 = 01,phase 2 = 10, no fault = 00. Report value is valid only when Bit[4] = 1.	RO	
0x37	STotalSOCP[7:4]/ SOCP_L[3:1]/ SOCP_L Hys [0]	Total OCP threshold, OCP_L flag assertion level and hysteresis setting SOCP[7:4]: Total Current OCP Ratio of ILIM (Over Current Protection) 0000: 50%; 0001: 60%; 0010: 70%; 0011: 80%; 0100: 90% ; 0101: 100%; 0110: 110%; 0111: 120%; 1000: 130% (Default) 1001: 140%; 1010: 150%; 1011: 160%; 1100: 170%; 1101: 180%; 1110: 190%; 1111: 200% SOCP_L[3:1] : OCP_L Ratio of ILIM (Over Current Protection) 000: 65%; 001: 70%; 010: 75%; 011: 80%; 100: 85%; 101: 90% (Default); 110: 95%; 111: 100% SOCP_L_Hys[0]: OCP_L Hysteresis Ration of ILIM (Over Current Protection) 0: 10% (Default); 1: 20%	R/W	8Ah
0x38	SIMONOvR[7:6]/ SOC[5:4]/SUV[3:2]/ SOV [1:0	SIMONOvR[7]: Overwrite SVID 0x15h (SIMON) “1” = Enable; “0” = Disable SIMONOvR[6]: Overwrite SVID 0x15h (SIMON) “1” = 1/2; “0” = 1/4 SOCP[5:4] : Per Phase OCP 00 = 400 mV; 01 = 450 mV (Default); 10 = 600 mV; 11 = 800 mV The lowest threshold for each phase is 400 mV/amp gain. The default gain is 6 so this corresponds to ~ 65 mV across CSP/CSN. Bit[3:2] : UVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV Bit[1:0] : OVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV	R/W	50h

Table 12. SMBUS REGISTER MAP (continued)

<table>
<tr><th>Reg Addr</th><th>Register Name</th><th>Description</th><th>Access</th><th>Default</th></tr>
<tr><td colspan="5">REGISTERS FOR VGT</td></tr>
<tr><td>0x39</td><td>SMisc1[7:0]</td><td>Bit[7]:Reserved
Bit[6]: VDAC Control
0 = SVID 0x31 VDAC follow SVID
1 = SVID 0x31 VDAC ignore SVID. VDAC control by SLCHVID.
Bit[5]: PWR State Control
0 = SVID 0x32 PWR state follow SVID
1 = SVID 0x32 PWR state ignore SVID. Phase control by SMBus.
Bit[4]: OFS control
0 = SVID 0x33 Offset follow SVID
1 = SVID 0x33 Offset ignore SVID. Offset control by SMBus.
Bit[3]: Total OCP Control
0 = Disable Total OCP function (OCPL# = H)
1 = Enable Total OCP function
Bit[2]: Per−phase OCP Control
0 = Disable Per−phase OCP function
1 = Enable Per−phase OCP function
Bit[1]: OVP Control
0 = Disable OVP function (VR_OVP# = H)
1 = Enable OVP function
Bit[0]: UVP Control
0 = Disable UVP function
1 = Enable UVP function
<table>
<tr><th></th><th>39h[5]</th><th>3Ah[4]</th></tr>
<tr><td>SVID</td><td>0</td><td>0</td></tr>
<tr><td>SVID</td><td>0</td><td>1</td></tr>
<tr><td>I2C</td><td>1</td><td>0</td></tr>
<tr><td>I2C</td><td>1</td><td>1</td></tr>
</table>
</td><td>R/W</td><td>0Fh</td></tr>
<tr><td>0x3A</td><td>SMisc2[7:0]</td><td>Bit[7]: Spread Spectrum “0” to disable (default);
“1” to enable
Bit[6]: SVOUT Voltage value select “0” for SVID register;
“1” actual A/D
Bit[5]: Output voltage offset control “0” to disable;
“1” to enable. This bit with function after 0x39[4] = “1”
Bit[4]: Auto phase function control “0” disable;
“1” to enable. This bit with function after 0x39[5] = “1”
If Bit[4] is 0, follow SIICP0 if 39[5] = 1; or follow SVID PS if 39[5] = 0
Bit[3]: DCM enable when in 1 phase “0” always CCM;
“1” DCM
Bit[2]: Loadline enable “0” disables LL; “1” enables (default)
Bit[1]: USM/PSM selection when in DCM “1” enables sonic mode
Bit[0]: OCP_L# enable control: “0” to disable; “1” to enable”</td><td>R/W</td><td>0Ch</td></tr>
</table>

Table 12. SMBUS REGISTER MAP (continued)

Reg Addr	Register Name	Description	Access	Default
REGISTERS FOR VGT				
0x3B	SOTPBH[7] SOTPEN[6] SOCPTH[5] SVRHOT#_EN[4] STEMP_VRHOT#[3:0]	Select Behavior or VR_SHDN# Bit[7]: OTP behavior selection 0 = VRSHDN# go low only; 1 = controller shutdown only Bit[6]: OTP function enable/disable 0 = Disable ; 1 = Enable Bit[5]: Total OCP threshold control 0 = Default; 1 = Double Bit[4]: VRHOT# “0” = Enable ; “1” = Disable Note: when VR_HOT is disabled ALERT will not assert and the Temp Status bit (SVID reg 0x10 bit) is not set. Bit[3:0]: SVID 0x12. Temp range from 91°C to 121°C, default = 106°C, 3°C/LSB 0000: No offset ; 0001: offset 1LSB ; 0010: offset 2LSB ; 0011: offset 3LSB; 0100: offset 4LSB ; 0101: offset 5LSB (default) ; 0110: offset 6LSB ; 0111: offset 7LSB ; 1000: offset 8LSB ; 1001: offset 9LSB ; 1010: offset 10LSB	R/W	05h
0x3F	SIMON_OFS[7:0]	IMON offset [7:0] (can be positive or negative) SVID 0x15 ± Bit[7:0] I^2C 0x16 ± Bit[7:0]	R/W	00h
0x40	SDVID_OFS[7:0]	DVID offset function (positive and negative adjustment) Enable this register after 0x39[4] = “1”	R/W	00h
0x42	SV_{BOOT}[7:0]	Bit[7]: control setting function (VBOOTA) “0” = Disable (follow H/W resistor setting); “1” = Enable (follow I^2C setting) Bit[6:0]: Vboot voltage from 0 V to 1.515 V, 10 mV/step If 0x42[6:0] = 0, SV_{BOOT} = 0 V Others, SV_{BOOT} = 255 mV + (0x42[6:0] − 1) * 10 mV	R/W	00h
0x44	STM[7:0]	I^2C Thermal Monitor Value Reading. Temperature reports in degree celsius (°C). To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resister in parallel. NTC uses 10 kΩ under 25°C and B25/50 approximates 3380. Use 732 Ω for parallel resister.	RO	–
0x47	RSVD[7:0]	Offset applied once you cross the high limit threshold in register 53h. 5 mV/step, VOFS is 2’s compliment, Bit 7 is sign bit	R/W	00h
0x49	RSVD[7:0]	Offset applied once you cross the low limit threshold in register 54h 5 mV/step, VOFS is 2’s compliment, Bit 7 is sign bit	R/W	00h
0x53	RSVD[7:0]	High limit threshold used for I^2C offset function Refer to IMVP8 VID table.	R/W	00h
0x54	RSVD[7:0]	Low limit threshold used for I^2C offset function Refer to IMVP8 VID table.	R/W	00h
GENERAL REGISTERS				
0x48	Version ID		RO	00h
0xB2	Chip ID		RO	29h

Table 13. SVID REGISTER MAP

Index	Name	Description	Access	Default 00h	PSYS 0Dh
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	1Ah	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number	R	9Bh	0x33
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data	R	00h	0x00
05h	Protocol ID	Identifies the SVID Protocol the controller supports	R	05h	05h
06h	Capability	Informs the Master of the controller's Capabilities, 1 = supported, 0 = not supported	R	D7h	N/A
		Bit 7 = Iout_format. Bit 7 = 0 when 1A = 1LSB of Reg 15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1			
		Bit 6 = ADC Measurement of Temp Supported = 1			
		Bit 5 = ADC Measurement of Pin Supported = 0			
		Bit 4 = ADC Measurement of Vin Supported = 1			
		Bit 3 = ADC Measurement of Iin Supported = 0			
		Bit 2 = ADC Measurement of Pout Supported = 1			
		Bit 1 = ADC Measurement of Vout Supported = 1			
		Bit 0 = ADC Measurement of Iout Supported = 1			
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR	R	00h	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h	00h
12h	Temp zone	Data register showing temperature zones the system is operating in	R	00h	N/A
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max	R	01h	N/A
16h	V_out	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8 mV	R	01h	N/A
17h	VR_Temp	8 bit binary word ADC of voltage. Binary format in deg C, IE 100C = 64h. A value of 00h indicates this function is not supported. To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resister in parallel. NTC uses 10 kΩ under 25°C and B25/50 approximates 3380. Use 732 Ω for parallel resister.	R	00h	N/A
18h	P_out	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported	R	01h	N/A
1Ah	V_in	8 bit binary word ADC of voltage. Input voltage is (1Ah−2)/7, unit is Volt. Full scale voltage is approximate 36 V	R	00h	N/A
1Bh	Input Power	Required for Input Power Domain Address 0Dh	R	N/A	00h
1Ch	Status2_last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h	
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	00h	N/A

Table 13. SVID REGISTER MAP (continued)

Index	Name	Description	Access	Default 00h	PSYS 0Dh
22h	Temp_Max	Data register containing the max temperature the platform supports and the level (No Suggestions) asserts. This value defaults to 100°C and programmable over the SVID Interface	R/W	6Ah	N/A
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/μs.	R	10 mV/μs or 30 mV/μs	N/A
25h	SR_slow	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/us. FAST/2 is default for IMVP8	R	1/2 fast	N/A
26h	VBOOT	The VBOOT is resistor programmed at startup. The controller will ramp to VBOOT and hold at VBOOT until it receives a new SVID SetVID command to move to a different voltage	R	xxh	N/A
2Ah	SR_Slow selector	Fast_SR/2: Default	R/W	01h	N/A
		Fast_SR/4			
		Fast_SR/8			
		Fast_SR/16			
2Bh	PS4 exit latency	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp	R	8Ch	N/A
2Ch	PS3 exit latency	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state	R	55h	N/A
2Dh	EN to Ready for SVID command (TA)	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands	R	CAh	N/A
2Eh	PIN Max	Input Power max for input power sensor			
2Fh	Pin _Alert _Th	Input Power Alert Threshold			
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP8 VID format	RW	FBh	N/A
31h	VID setting	Data register containing currently programmed VID voltage. VID data format	RW	xxh	N/A
32h	Pwr State	Register containing the current programmed power state	RW	00h	N/A
33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 BITS are # VID steps for margin 2 s complement	RW	00h	N/A
		00h = no margin			
		01h = +1 VID step			
		02h = +2 VID steps			
		Ffh = −1 VID step			
		Feh = −2 VID steps			
34h	Multi VR config	Bit mapped data register that configures multiple VRs behavior on the same bus and can be programmed to reset behavior of VR_Ready under 0.0 V VID command	RW	00h	
35h	Set Reg Addrs	Write address pointer for main addr space	RW	35h	N/A
42h	IVID1_VID	VID for max current from IVID1_I	RW	00h	N/A

Table 13. SVID REGISTER MAP (continued)

Index	Name	Description	Access	Default 00h	PSYS 0Dh
43h	IVID1_I	Max current for IVID1_VID ≥ VID setting ≥ IVID2_VID	RW	00h	N/A
44h	IVID2_VID	VID for max current from IVID2_I	RW	00h	N/A
45h	IVID2_I	Max current for IVID2_VID ≥ VID setting ≥ IVID3_VID	RW	00h	N/A
46h	IVID3_VID	VID for max current from IVID3_I	RW	00h	N/A
47h	IVID3_I	Max current for IVID3_VID ≥ VID setting	RW	00h	N/A

IMVP8 VID TABLE

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	0.25	01
0	0	0	0	0	0	1	0	0.255	02
0	0	0	0	0	0	1	1	0.26	03
0	0	0	0	0	1	0	0	0.265	04
0	0	0	0	0	1	0	1	0.27	05
0	0	0	0	0	1	1	0	0.275	06
0	0	0	0	0	1	1	1	0.28	07
0	0	0	0	1	0	0	0	0.285	08
0	0	0	0	1	0	0	1	0.29	09
0	0	0	0	1	0	1	0	0.295	0A
0	0	0	0	1	0	1	1	0.3	0B
0	0	0	0	1	1	0	0	0.305	0C
0	0	0	0	1	1	0	1	0.31	0D
0	0	0	0	1	1	1	0	0.315	0E
0	0	0	0	1	1	1	1	0.32	0F
0	0	0	1	0	0	0	0	0.325	10
0	0	0	1	0	0	0	1	0.33	11
0	0	0	1	0	0	1	0	0.335	12
0	0	0	1	0	0	1	1	0.34	13
0	0	0	1	0	1	0	0	0.345	14
0	0	0	1	0	1	0	1	0.35	15
0	0	0	1	0	1	1	0	0.355	16
0	0	0	1	0	1	1	1	0.36	17
0	0	0	1	1	0	0	0	0.365	18
0	0	0	1	1	0	0	1	0.37	19
0	0	0	1	1	0	1	0	0.375	1A
0	0	0	1	1	0	1	1	0.38	1B
0	0	0	1	1	1	0	0	0.385	1C
0	0	0	1	1	1	0	1	0.39	1D
0	0	0	1	1	1	1	0	0.395	1E
0	0	0	1	1	1	1	1	0.4	1F
0	0	1	0	0	0	0	0	0.405	20
0	0	1	0	0	0	0	1	0.41	21
0	0	1	0	0	0	1	0	0.415	22
0	0	1	0	0	0	1	1	0.42	23
0	0	1	0	0	1	0	0	0.425	24
0	0	1	0	0	1	0	1	0.43	25
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	1	0.44	27
0	0	1	0	1	0	0	0	0.445	28
0	0	1	0	1	0	0	1	0.45	29

IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	1	0	1	0	0.455	2A
0	0	1	0	1	0	1	1	0.46	2B
0	0	1	0	1	1	0	0	0.465	2C
0	0	1	0	1	1	0	1	0.47	2D
0	0	1	0	1	1	1	0	0.475	2E
0	0	1	0	1	1	1	1	0.48	2F
0	0	1	1	0	0	0	0	0.485	30
0	0	1	1	0	0	0	1	0.49	31
0	0	1	1	0	0	1	0	0.495	32
0	0	1	1	0	0	1	1	0.5	33
0	0	1	1	0	1	0	0	0.505	34
0	0	1	1	0	1	0	1	0.51	35
0	0	1	1	0	1	1	0	0.515	36
0	0	1	1	0	1	1	1	0.52	37
0	0	1	1	1	0	0	0	0.525	38
0	0	1	1	1	0	0	1	0.53	39
0	0	1	1	1	0	1	0	0.535	3A
0	0	1	1	1	0	1	1	0.54	3B
0	0	1	1	1	1	0	0	0.545	3C
0	0	1	1	1	1	0	1	0.55	3D
0	0	1	1	1	1	1	0	0.555	3E
0	0	1	1	1	1	1	1	0.56	3F
0	1	0	0	0	0	0	0	0.565	40
0	1	0	0	0	0	0	1	0.57	41
0	1	0	0	0	0	1	0	0.575	42
0	1	0	0	0	0	1	1	0.58	43
0	1	0	0	0	1	0	0	0.585	44
0	1	0	0	0	1	0	1	0.59	45
0	1	0	0	0	1	1	0	0.595	46
0	1	0	0	0	1	1	1	0.6	47
0	1	0	0	1	0	0	0	0.605	48
0	1	0	0	1	0	0	1	0.61	49
0	1	0	0	1	0	1	0	0.615	4A
0	1	0	0	1	0	1	1	0.62	4B
0	1	0	0	1	1	0	0	0.625	4C
0	1	0	0	1	1	0	1	0.63	4D
0	1	0	0	1	1	1	0	0.635	4E
0	1	0	0	1	1	1	1	0.64	4F
0	1	0	1	0	0	0	0	0.645	50
0	1	0	1	0	0	0	1	0.65	51
0	1	0	1	0	0	1	0	0.655	52
0	1	0	1	0	0	1	1	0.66	53
0	1	0	1	0	1	0	0	0.665	54

IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	1	0	1	0	1	0.67	55
0	1	0	1	0	1	1	0	0.675	56
0	1	0	1	0	1	1	1	0.68	57
0	1	0	1	1	0	0	0	0.685	58
0	1	0	1	1	0	0	1	0.69	59
0	1	0	1	1	0	1	0	0.695	5A
0	1	0	1	1	0	1	1	0.7	5B
0	1	0	1	1	1	0	0	0.705	5C
0	1	0	1	1	1	0	1	0.71	5D
0	1	0	1	1	1	1	0	0.715	5E
0	1	0	1	1	1	1	1	0.72	5F
0	1	1	0	0	0	0	0	0.725	60
0	1	1	0	0	0	0	1	0.73	61
0	1	1	0	0	0	1	0	0.735	62
0	1	1	0	0	0	1	1	0.74	63
0	1	1	0	0	1	0	0	0.745	64
0	1	1	0	0	1	0	1	0.75	65
0	1	1	0	0	1	1	0	0.755	66
0	1	1	0	0	1	1	1	0.76	67
0	1	1	0	1	0	0	0	0.765	68
0	1	1	0	1	0	0	1	0.77	69
0	1	1	0	1	0	1	0	0.775	6A
0	1	1	0	1	0	1	1	0.78	6B
0	1	1	0	1	1	0	0	0.785	6C
0	1	1	0	1	1	0	1	0.79	6D
0	1	1	0	1	1	1	0	0.795	6E
0	1	1	0	1	1	1	1	0.8	6F
0	1	1	1	0	0	0	0	0.805	70
0	1	1	1	0	0	0	1	0.81	71
0	1	1	1	0	0	1	0	0.815	72
0	1	1	1	0	0	1	1	0.82	73
0	1	1	1	0	1	0	0	0.825	74
0	1	1	1	0	1	0	1	0.83	75
0	1	1	1	0	1	1	0	0.835	76
0	1	1	1	0	1	1	1	0.84	77
0	1	1	1	1	0	0	0	0.845	78
0	1	1	1	1	0	0	1	0.85	79
0	1	1	1	1	0	1	0	0.855	7A
0	1	1	1	1	0	1	1	0.86	7B
0	1	1	1	1	1	0	0	0.865	7C
0	1	1	1	1	1	0	1	0.87	7D
0	1	1	1	1	1	1	0	0.875	7E
0	1	1	1	1	1	1	1	0.88	7F

IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	0	0	0	0	0.885	80
1	0	0	0	0	0	0	1	0.89	81
1	0	0	0	0	0	1	0	0.895	82
1	0	0	0	0	0	1	1	0.9	83
1	0	0	0	0	1	0	0	0.905	84
1	0	0	0	0	1	0	1	0.91	85
1	0	0	0	0	1	1	0	0.915	86
1	0	0	0	0	1	1	1	0.92	87
1	0	0	0	1	0	0	0	0.925	88
1	0	0	0	1	0	0	1	0.93	89
1	0	0	0	1	0	1	0	0.935	8A
1	0	0	0	1	0	1	1	0.94	8B
1	0	0	0	1	1	0	0	0.945	8C
1	0	0	0	1	1	0	1	0.95	8D
1	0	0	0	1	1	1	0	0.955	8E
1	0	0	0	1	1	1	1	0.96	8F
1	0	0	1	0	0	0	0	0.965	90
1	0	0	1	0	0	0	1	0.97	91
1	0	0	1	0	0	1	0	0.975	92
1	0	0	1	0	0	1	1	0.98	93
1	0	0	1	0	1	0	0	0.985	94
1	0	0	1	0	1	0	1	0.99	95
1	0	0	1	0	1	1	0	0.995	96
1	0	0	1	0	1	1	1	1	97
1	0	0	1	1	0	0	0	1.005	98
1	0	0	1	1	0	0	1	1.01	99
1	0	0	1	1	0	1	0	1.015	9A
1	0	0	1	1	0	1	1	1.02	9B
1	0	0	1	1	1	0	0	1.025	9C
1	0	0	1	1	1	0	1	1.03	9D
1	0	0	1	1	1	1	0	1.035	9E
1	0	0	1	1	1	1	1	1.04	9F
1	0	1	0	0	0	0	0	1.045	A0
1	0	1	0	0	0	0	1	1.05	A1
1	0	1	0	0	0	1	0	1.055	A2
1	0	1	0	0	0	1	1	1.06	A3
1	0	1	0	0	1	0	0	1.065	A4
1	0	1	0	0	1	0	1	1.07	A5
1	0	1	0	0	1	1	0	1.075	A6
1	0	1	0	0	1	1	1	1.08	A7
1	0	1	0	1	0	0	0	1.085	A8
1	0	1	0	1	0	0	1	1.09	A9
1	0	1	0	1	0	1	0	1.095	AA

IMVP8 VID TABLE (continued)

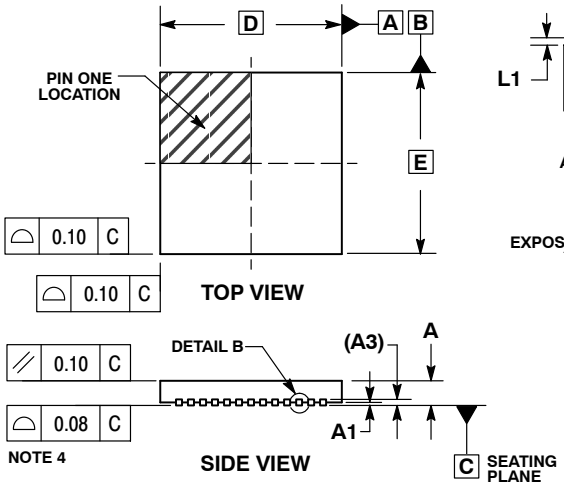
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	0	1	0	1	1	1.1	AB
1	0	1	0	1	1	0	0	1.105	AC
1	0	1	0	1	1	0	1	1.11	AD
1	0	1	0	1	1	1	0	1.115	AE
1	0	1	0	1	1	1	1	1.12	AF
1	0	1	1	0	0	0	0	1.125	B0
1	0	1	1	0	0	0	1	1.13	B1
1	0	1	1	0	0	1	0	1.135	B2
1	0	1	1	0	0	1	1	1.14	B3
1	0	1	1	0	1	0	0	1.145	B4
1	0	1	1	0	1	0	1	1.15	B5
1	0	1	1	0	1	1	0	1.155	B6
1	0	1	1	0	1	1	1	1.16	B7
1	0	1	1	1	0	0	0	1.165	B8
1	0	1	1	1	0	0	1	1.17	B9
1	0	1	1	1	0	1	0	1.175	BA
1	0	1	1	1	0	1	1	1.18	BB
1	0	1	1	1	1	0	0	1.185	BC
1	0	1	1	1	1	0	1	1.19	BD
1	0	1	1	1	1	1	0	1.195	BE
1	0	1	1	1	1	1	1	1.2	BF
1	1	0	0	0	0	0	0	1.205	C0
1	1	0	0	0	0	0	1	1.21	C1
1	1	0	0	0	0	1	0	1.215	C2
1	1	0	0	0	0	1	1	1.22	C3
1	1	0	0	0	1	0	0	1.225	C4
1	1	0	0	0	1	0	1	1.23	C5
1	1	0	0	0	1	1	0	1.235	C6
1	1	0	0	0	1	1	1	1.24	C7
1	1	0	0	1	0	0	0	1.245	C8
1	1	0	0	1	0	0	1	1.25	C9
1	1	0	0	1	0	1	0	1.255	CA
1	1	0	0	1	0	1	1	1.26	CB
1	1	0	0	1	1	0	0	1.265	CC
1	1	0	0	1	1	0	1	1.27	CD
1	1	0	0	1	1	1	0	1.275	CE
1	1	0	0	1	1	1	1	1.28	CF
1	1	0	1	0	0	0	0	1.285	D0
1	1	0	1	0	0	0	1	1.29	D1
1	1	0	1	0	0	1	0	1.295	D2
1	1	0	1	0	0	1	1	1.3	D3
1	1	0	1	0	1	0	0	1.305	D4
1	1	0	1	0	1	0	1	1.31	D5

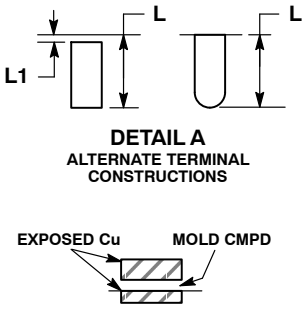
IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	1	0	1	1	0	1.315	D6
1	1	0	1	0	1	1	1	1.32	D7
1	1	0	1	1	0	0	0	1.325	D8
1	1	0	1	1	0	0	1	1.33	D9
1	1	0	1	1	0	1	0	1.335	DA
1	1	0	1	1	0	1	1	1.34	DB
1	1	0	1	1	1	0	0	1.345	DC
1	1	0	1	1	1	0	1	1.35	DD
1	1	0	1	1	1	1	0	1.355	DE
1	1	0	1	1	1	1	1	1.36	DF
1	1	1	0	0	0	0	0	1.365	E0
1	1	1	0	0	0	0	1	1.37	E1
1	1	1	0	0	0	1	0	1.375	E2
1	1	1	0	0	0	1	1	1.38	E3
1	1	1	0	0	1	0	0	1.385	E4
1	1	1	0	0	1	0	1	1.39	E5
1	1	1	0	0	1	1	0	1.395	E6
1	1	1	0	0	1	1	1	1.4	E7
1	1	1	0	1	0	0	0	1.405	E8
1	1	1	0	1	0	0	1	1.41	E9
1	1	1	0	1	0	1	0	1.415	EA
1	1	1	0	1	0	1	1	1.42	EB
1	1	1	0	1	1	0	0	1.425	EC
1	1	1	0	1	1	0	1	1.43	ED
1	1	1	0	1	1	1	0	1.435	EE
1	1	1	0	1	1	1	1	1.44	EF
1	1	1	1	0	0	0	0	1.445	F0
1	1	1	1	0	0	0	1	1.45	F1
1	1	1	1	0	0	1	0	1.455	F2
1	1	1	1	0	0	1	1	1.46	F3
1	1	1	1	0	1	0	0	1.465	F4
1	1	1	1	0	1	0	1	1.47	F5
1	1	1	1	0	1	1	0	1.475	F6
1	1	1	1	0	1	1	1	1.48	F7
1	1	1	1	1	0	0	0	1.485	F8
1	1	1	1	1	0	0	1	1.49	F9
1	1	1	1	1	0	1	0	1.495	FA
1	1	1	1	1	0	1	1	1.5	FB
1	1	1	1	1	1	0	0	1.505	FC
1	1	1	1	1	1	0	1	1.51	FD
1	1	1	1	1	1	1	0	1.515	FE
1	1	1	1	1	1	1	1	1.52	FF

PACKAGE DIMENSIONS

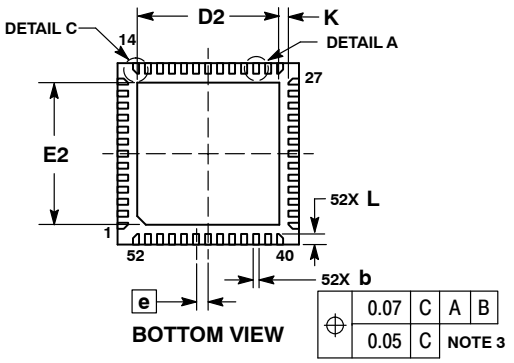
QFN52 6x6, 0.4P
CASE 485BE
ISSUE B

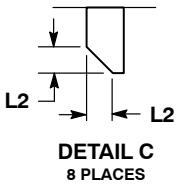




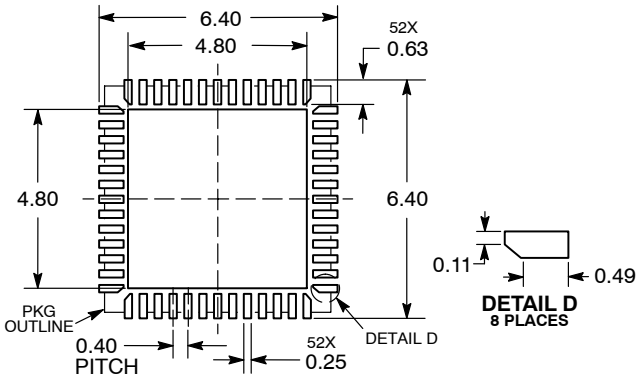
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	





SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MANUFACTURER AND ASSEMBLY INFORMATION

Device	Manufacturer	Assembly
ASP1900AMNTXG	AFSM	ASE/UTAC
ASP1900BMNTXG	AFSM	ASE/UTAC

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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