High-Speed DPDT Power-Off Protected Switch With Single Enable

FEATURES

- V_{CC}: 1.65V to 5.0V
- $V_{I/O}$ Accepts Signals Up to 5.5V Beyond Power Supply V_{CC}
- 1.8V Compatible Control Pin Inputs
- Low-Power When nOE is Disabled (1.0μA)
- R_{ON} is typically 4Ω at V_{CC} = 3.3V
- ΔR_{ON} is typically 0.5Ω at V_{CC} = 3.3V
- Channel On-Capacitance: 6pF Maximum
- Low Current Consumption I_{CC}: 75μA (typ.) at V_{CC} = 3.3V
- High Bandwidth: 1.3GHz Typically
- Operating Temperature: -40°C to +125°C
- ESD ⩾ 2kV Human-Body Model (HBM)
- Low Crosstalk: -40dB @ 250MHz
- Low Bit-to-Bit Skew: 50ps (typ.)
- Near-Zero Propagation Delay: 250ps
- Break-Before-Make Switching
- Power-Off Protection
- Packages: DFN10L-3.0x3.0 and MSOP10L

APPLICATIONS

- USB 2.0 Signal Routing
- MIPI Signal Routing
- Differential Signal Data Routing
- Servers
- Data Center switches & routers
- Wireless infrastructure
- PC & Notebooks

GENERAL DESCRIPTIONS

The ASW3221 is a high-bandwidth, double-pole double-throw (DPDT) analog switch that operates from a single 1.65V to 5.0V power supply. The device supports bidirectional analog and digital signals on the I/O pins and can pass signals above supply up to 5.5V.

The ASW3221 is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480Mbps). The wide bandwidth (1.3GHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs.

Power-Off Protection up to 5.5V on the I/O pins of the ASW3221 provides isolation when the supply voltage is removed (V_{CC} = 0V or floating). without this protection feature, switches can back-power the supply rail and cause potential damage to the system.

The ASW3221 is available in DFN10L-3.0x3.0 and MSOP10L packages. It operates over an ambient temperature range of -40°C to +125°C.

BLOCK DIAGRAM

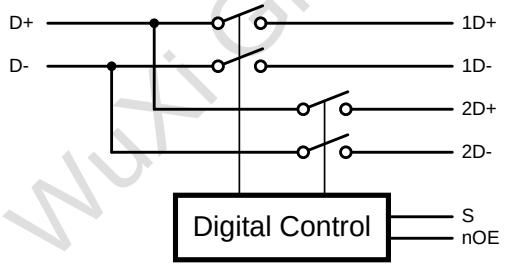
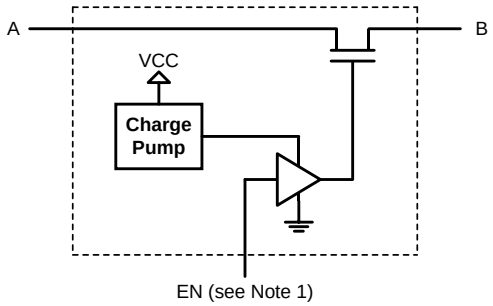


Figure 1, Block Diagram

Simplified Schematic, Each FET Switch (SW)



1. EN is the internal enable signal applied to the switch

Figure 2, Simplified Schematic, Each FET Switch (SW)

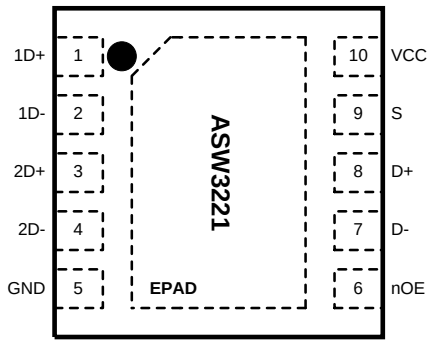
Revision History

Note: Page numbers for previous revisions may be different from page numbers in the current version.

VERSION	CHANGE DATE	CHANGE ITEMS
V01	2022/12	Initial version completed.
V02	2023/3	Add Eye Pattern.
V03	2023/4	Update DFN10L POD and Timing Characteristics.
V04	2023/9	Added humidity sensitivity level, Added DFN package tape and reel information.
V05	2024/2	Update 1.65V R_{ONFLAT}

PIN DIAGRAM

DFN10L-3.0x3.0



MSOP10L

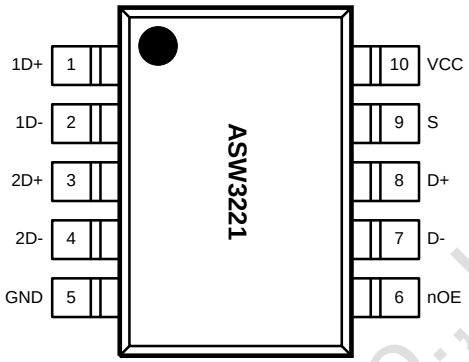


Figure 3, Pin Diagram (Top View)

PIN DESCRIPTIONS

PIN No.	PIN NAME	TYPE	DESCRIPTIONS
1	1D+	I/O	Data Signal Port 1, Positive.
2	1D-	I/O	Data Signal Port 1, Negative.
3	2D+	I/O	Data Signal Port 2, Positive.
4	2D-	I/O	Data Signal Port 2, Negative.
5	GND	GROUND	Ground.
6	nOE	I	Switch Enable Control Pin, Active Low.
7	D-	I/O	Data Signal Common Port, Negative.
8	D+	I/O	Data Signal Common Port, Positive.
9	S	I	Select Input.
10	VCC	POWER	Power Supply.
11	EPAD	--	Ground or Be Floating.

Note: The positive and negative pin labels are the name label distinction, and the chip does not distinguish between positive and negative.

FUNCTION TRUTH TABLE

nOE	S	1D+, 1D-	2D+, 2D-
0	0	ON (D+ connected to 1D+, D- connected to 1D-)	OFF (Hi-Z)
0	1	OFF (Hi-Z)	ON (D+ connected to 2D+, D- connected to 2D-)
1	X	OFF (Hi-Z)	OFF (Hi-Z)

Absolute Maximum Ratings

Stress exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Power Supply Voltage	-0.3	5.5	V
$V_{I/O}$	Switch Input/Output Voltage (nD+, nD-)	-0.3	5.5	V
	Switch Input/Output Voltage (D+, D-)	-0.3	5.5	V
V_{IN}	Control Input Voltage (S, nOE)	-0.3	5.5	V
$I_{I/O}$	On-State Switch Continuous DC Current	±100		mA
$I_{I/O-PK}$(1)	On-State Switch Peak Current, 10% Duty Cycle, t_{ON} = 100mS	±150		mA
I_{INK}	Control Input Clamp Current	-50		mA
ESD_{HBM}	Human-Body Model	±2000		V
ESD_{CDM}	Charge-Device Model	±1000		K
T_{STG}	Storage Temperature	-65	+150	°C

Notes:
1. Defined as 10% ON, 90% OFF Duty Cycle.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Power Supply Voltage	1.65	5.0	V
V_{IN}	Control Input Voltage (S, nOE)	0	5.0	V
$V_{I/O}$	Switch Input/Output Voltage (1D+, 1D-, 2D+, 2D-)	0	5.0	V
	Switch Input/Output Voltage (D+, D-)	0	5.0	
T_A	Operating Temperature	-40	+125	°C

DC ELECTRICAL CHARACTERISTICS

(All typical values are at V_{CC} = 3.3V, T_A = 25°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	V_{CC} (V)	T_A = -40°C to 125°C			UNIT
				MIN	TYP	MAX	
DIGITAL INPUTS (S, nOE)							
V_{IH}(1)	Control Input Voltage High	S, nOE	1.65	1.3			V
			3.3	1.4			
			5.0	1.5			
V_{IL}(1)	Control Input Voltage Low	S, nOE	1.65			0.4	V
			3.3			0.4	
			5.0			0.4	
I_{IN}(1)	Control Input Leakage Current	V_{IN} = V_{CC} or GND	1.65 - 5.0			±1.0	µA
SUPPLY AND SWITCH I/O LEAKAGE CURRENT							
I_{CC}	Quiescent Supply Current	$V_{I/O}$ = 0V to 5.0V, nOE = 0V, S = V_{CC} or 0V	1.65		45	70	µA
			3.3		75	115	
			5.0		100	150	
I_{CCZ}	Quiescent Supply Current Under Low-Power Mode	$V_{I/O}$ = 0V to 5.0V, nOE = V_{CC}, S = V_{CC} or 0V	5.0			1.0	µA
I_{OFF}	Power OFF Leakage Current (All I/O Ports)	$V_{I/O}$ = 0V to 5.0V, nOE = 0V	0			±2.0	µA
I_{OZ}(1)	Switch Off-State Leakage for Open Data Paths	$V_{I/O}$ = 0V to 5.0V, nOE = V_{CC}	5.0			±1.0	µA
I_{CL}(1)	Switch On-State Leakage for Closed Data Paths	$V_{I/O}$ = 0V to 5.0V, nOE = 0V	5.0		±2.5	±5.0	µA
SWITCH ON RESISTANCE							
R_{ON}	On-Resistance, (Figure 4)	$I_{I/O}$ = 8mA, V_{IN} = 0V to 5.0V	1.65, 3.3, 5.0		4.0	7.0	Ω
R_{ONFLAT}(2)	On-Resistance Flatness (Figure 4)	$I_{I/O}$ = 8mA, V_{IN} = 0V to 5.0V	1.65		0.85	1.3	Ω
			3.3, 5.0		0.5	0.8	Ω
ΔR_{ON}(3)	On-Resistance match between channels (Figure 4)	$I_{I/O}$ = 8mA, $V_{I/O1}$ = 0.5V; $I_{I/O}$ = 8mA, $V_{I/O2}$ = 0.5V;	1.65, 3.3, 5.0		0.2	0.5	Ω
		$I_{I/O}$ = 8mA, $V_{I/O1}$ = 1.5V; $I_{I/O}$ = 8mA, $V_{I/O2}$ = 1.5V;	1.65, 3.3, 5.0		0.2	0.5	Ω
		$I_{I/O}$ = 8mA, $V_{I/O1}$ = 3.0V; $I_{I/O}$ = 8mA, $V_{I/O2}$ = 3.0V;	1.65, 3.3, 5.0		0.2	0.5	Ω
		$I_{I/O}$ = 8mA, $V_{I/O1}$ = 4.5V; $I_{I/O}$ = 8mA, $V_{I/O2}$ = 4.5V;	1.65, 3.3, 5.0		0.2	0.5	Ω
CAPACITANCE (Typical: V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω, C_L = 5pF, f = 1MHz)							
C_{IN}	Control Inputs Capacitance	$V_{I/O}$ = 0V or 3.3V, f = 1MHz	3.3		1.0		pF
$C_{I/O(ON)}$	Switch ON Capacitance	$V_{I/O}$ = 0V or 3.3V, f = 1MHz, nOE = 0V, Switch ON	3.3		5.0		pF
$C_{I/O(OFF)}$	Switch OFF Capacitance	$V_{I/O}$ = 0V or 3.3V, f = 1MHz, nOE = 0V, Switch OFF	3.3		3.0		pF

Notes:

1. V_{IN} and I_{IN} refer to control inputs. $V_{I/O}$ and $I_{I/O}$ refer to all switch I/O pins.
2. Flatness is defined as the difference between the maximum and minimum value of on−resistance as measured over the specified analog signal ranges.
3. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ between 1D+ and 1D- or 2D+ and 2D-.

AC ELECTRICAL CHARACTERISTICS

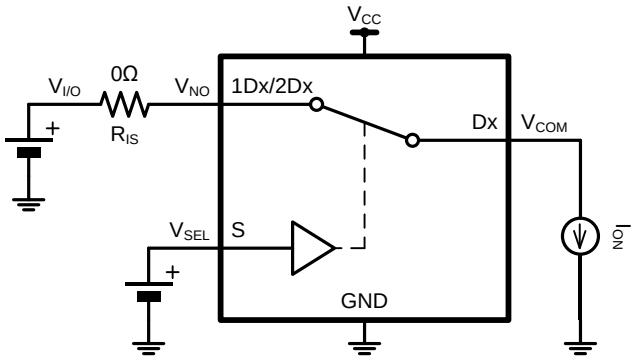
(All typical values are at V_{CC} = 3.3V, T_A = 25°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	V_{CC} (V)	T_A = -40°C to 125°C			UNIT
				MIN	TYP	MAX	
TIMING CHARACTERISTICS							
t_{PD}	Propagation Delay(4)	R_L = 50Ω, C_L = 35pF	1.65 - 5.0		60		ps
t_{ON}	Turn-On Time, S toggles between H and L (Figure 5)	R_L = 50Ω, C_L = 35pF, $V_{I/O}$ = 0.6V	1.65 - 5.0		5		µs
t_{OFF}	Turn-Off Time, S toggles between H and L (Figure 5)	R_L = 50Ω, C_L = 35pF, $V_{I/O}$ = 0.6V	1.65 - 5.0		300	500	ns
t_{EN}	Enable Time, nOE toggles from H to L (Figure 5)	R_L = 50Ω, C_L = 35pF, $V_{I/O}$ = 0.6V	1.65 - 5.0		16	50	µs
t_{DIS}	Disable Time, nOE toggles from L to H (Figure 5)	R_L = 50Ω, C_L = 35pF, $V_{I/O}$ = 0.6V	1.65 - 5.0		310	500	ns
t_{BBM}	Break-Before-Make Delay (Figure 6)	R_L = 50Ω, C_L = 35pF, $V_{I/O}$ = 0.6V	1.65 - 5.0		4.7		µs
$t_{SK(P)}$	Skew betwwen Opposite Transitions of the Same Output(4)		3.3		6	12	ps
FREQUENCY CHARACTERISTICS							
BW	-3dB Bandwidth (Figure 7)	R_L = 50Ω, C_L = 5pF	3.3		1.3		GHz
DIL	Differential Insertion Loss	R_L = 50Ω, f = 10MHz	3.3		0.3		dB
		R_L = 50Ω, f = 250MHz	3.3		0.8		dB
DRL	Differential Return Loss	R_L = 50Ω, f = 10MHz	3.3		-30		dB
		R_L = 50Ω, f = 250MHz	3.3		-14		dB
O_{ISO}	Differential Off-Isolation (Figure 8)	R_L = 50Ω, f = 10MHz	3.3		-73		dB
		R_L = 50Ω, f = 250MHz	3.3		-44		dB
X_{TALK}	Differential Non-Adjacent Channel Crosstalk (Figure 9)	R_L = 50Ω, f = 10MHz	3.3		-63		dB
		R_L = 50Ω, f = 250MHz	3.3		-36		dB

Notes:

4. Guaranteed by Characterization.

TEST CIRCUITS



Channel ON,
$R_{ON} = (V_{NO} - V_{COM}) / I_{ON}$
$V_{SEL} = V_{IH}$ or V_{IL}

Figure 4, ON Resistance (R_{ON})

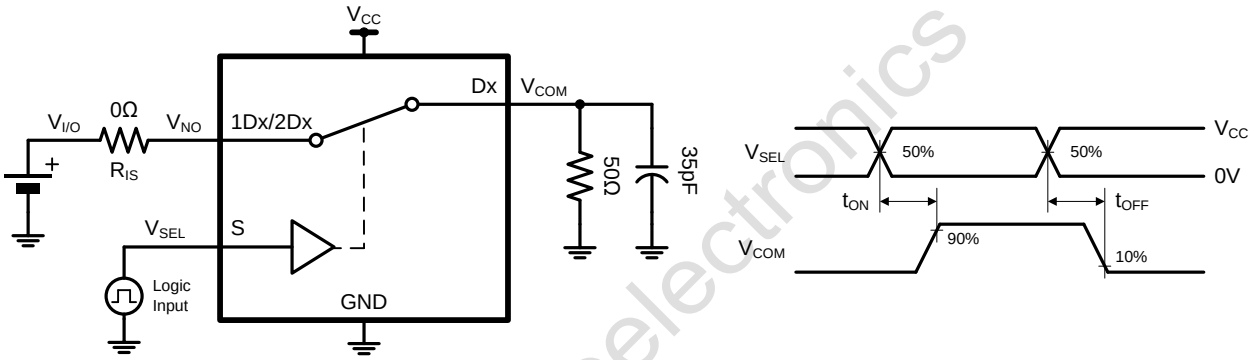


Figure 5, Turn-On and Turn-Off Time (t_{ON}/t_{OFF})

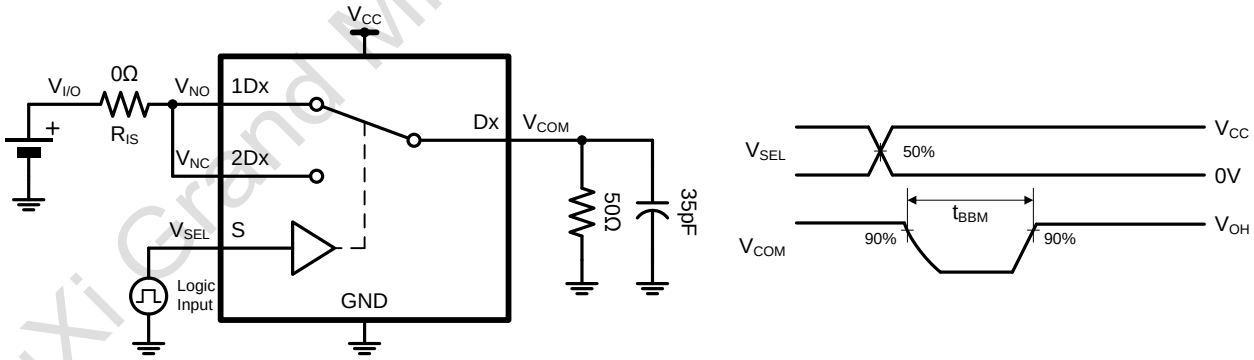
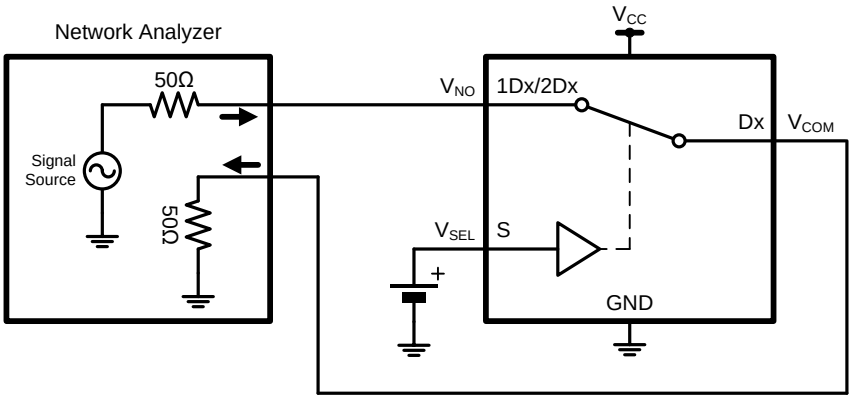


Figure 6, Break-Before-Make Time (t_{BBM})

TEST CIRCUITS (CONTINUED)

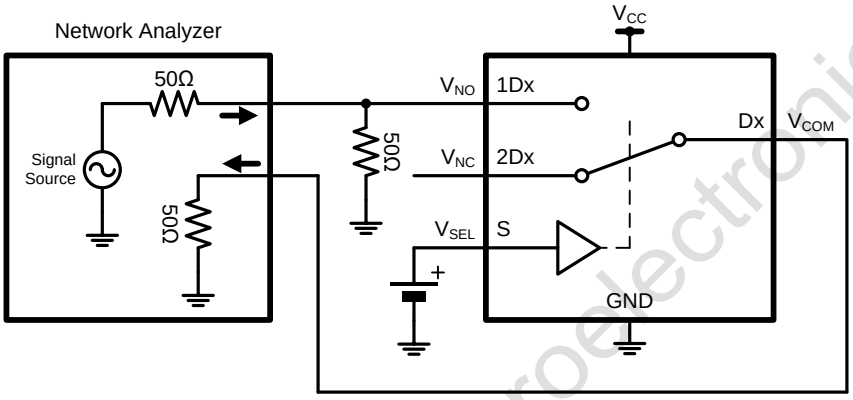


Channel ON: 1Dx/2Dx to Dx
V_{SEL} = V_{IH} or V_{IL}

Network Analyzer Setup

Source Power = 0dBm
(632mV P-P at 50Ω load)
DC Bias = 350mV

Figure 7, ON Channel -3dB Bandwidth (BW)

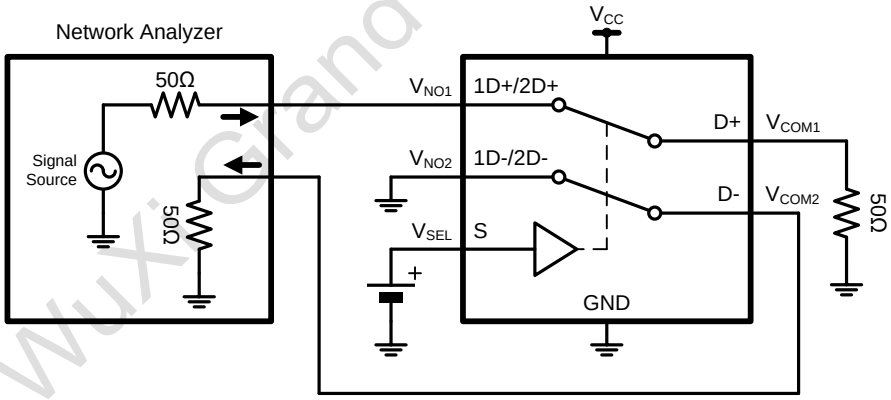


Channel OFF: 1Dx/2Dx to Dx
V_{SEL} = V_{IH} or V_{IL}

Network Analyzer Setup

Source Power = 0dBm
(632mV P-P at 50Ω load)
DC Bias = 350mV

Figure 8, OFF Isolation (O_{ISO})



Channel ON:1D+/2D+ to D+
Channel ON: 1D-/2D- to D-
V_{SEL} = V_{IH} or V_{IL}

Network Analyzer Setup

Source Power = 0dBm
(632mV P-P at 50Ω load)
DC Bias = 350mV

Figure 9, Chanel-to-Chanel Crosstalk (X_{TALK})

TYPICAL PERFORMANCES

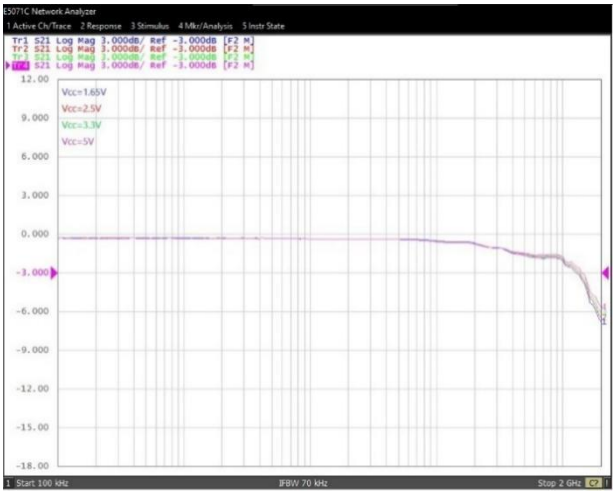


Figure 10, -3dB Bandwidth

Figure 11, OFF Isolation vs. Frequency

Figure 12, Crosstalk vs. Frequency

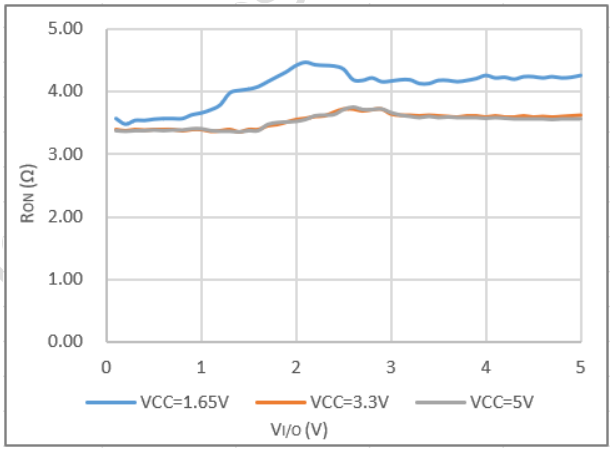


Figure 13, R_{ON} vs. $V_{I/O}$ ($I_{I/O}$ = 8mA)

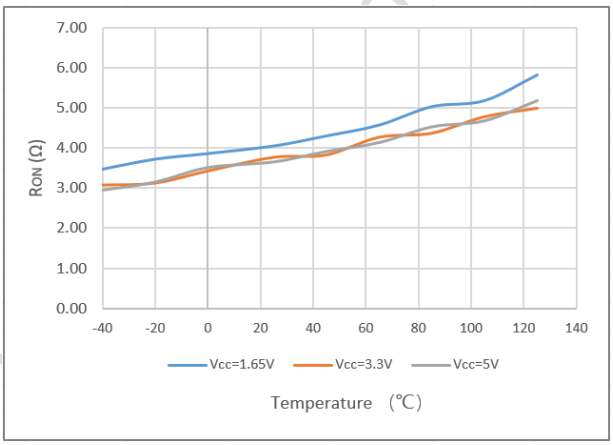


Figure 14, R_{ON} vs. Temperature

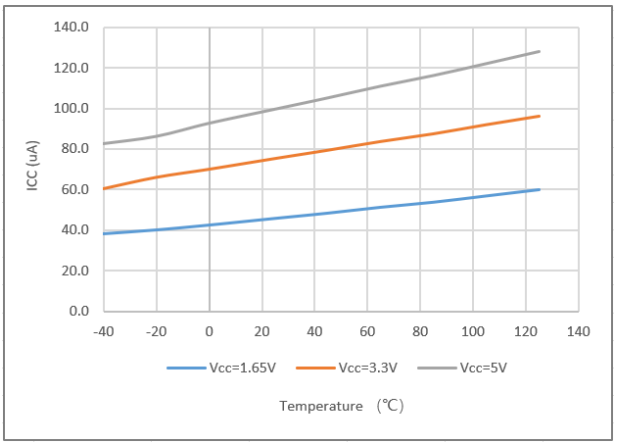


Figure 15, I_{CC} vs. Temperature

TYPICAL PERFORMANCES (CONTINUED)

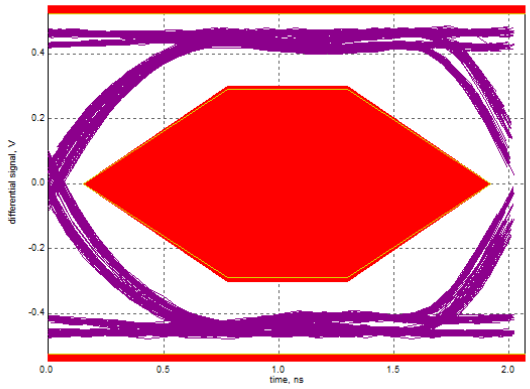


Figure 16, Eye Pattern: USB2.0 test, 1 Data Lane, No Device through Path

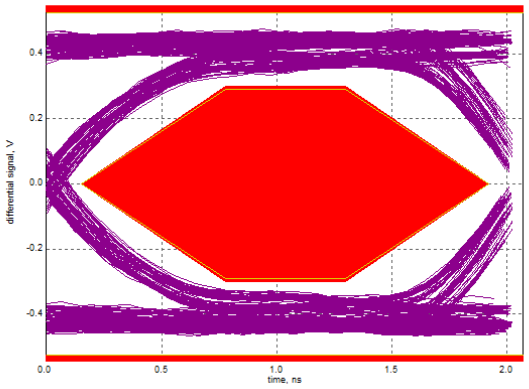


Figure 17, Eye Pattern: USB2.0 test, 1 Data Lane, With Device

APPLICATION INFORMATION

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The ASW3221 solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller. ASW3221 can also be used to connect a single controller to two USB connectors.

It is recommended that the digital control pins S and nOE be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin. The ASW3221 may be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50Ω resistor to prevent signal reflections back into the device.

The typical application diagram is shown in figure 16 below.

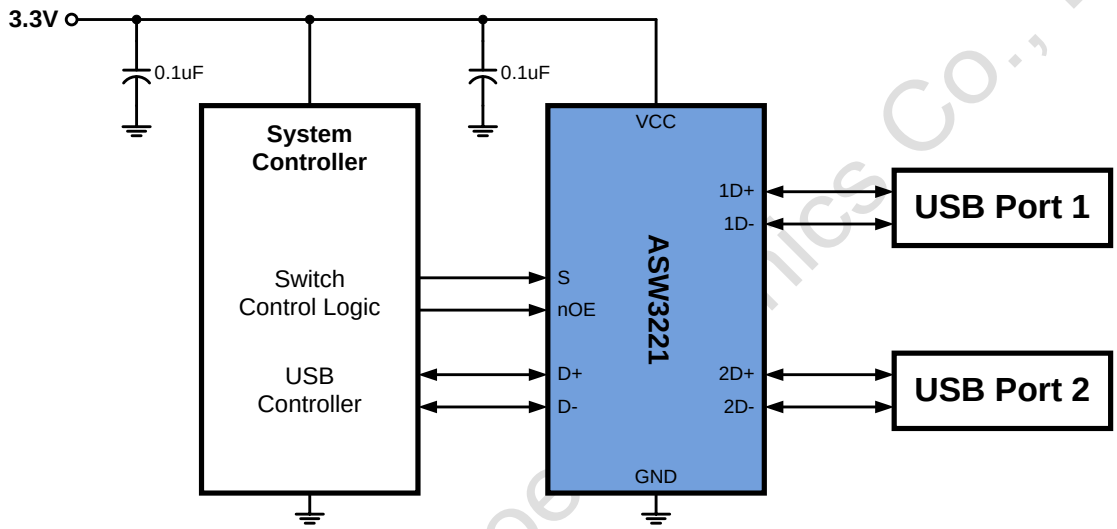
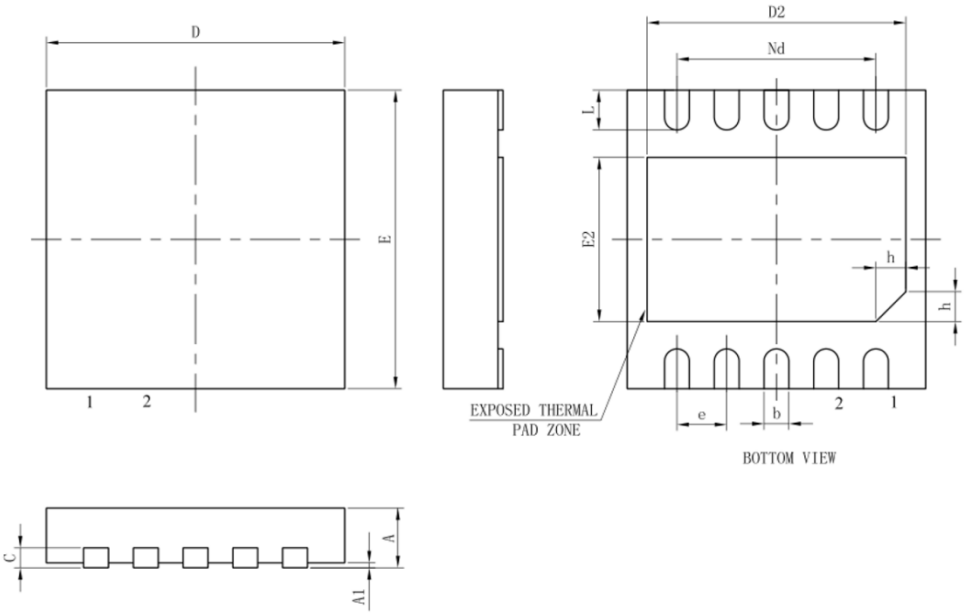


Figure 18, Typical Application Diagram

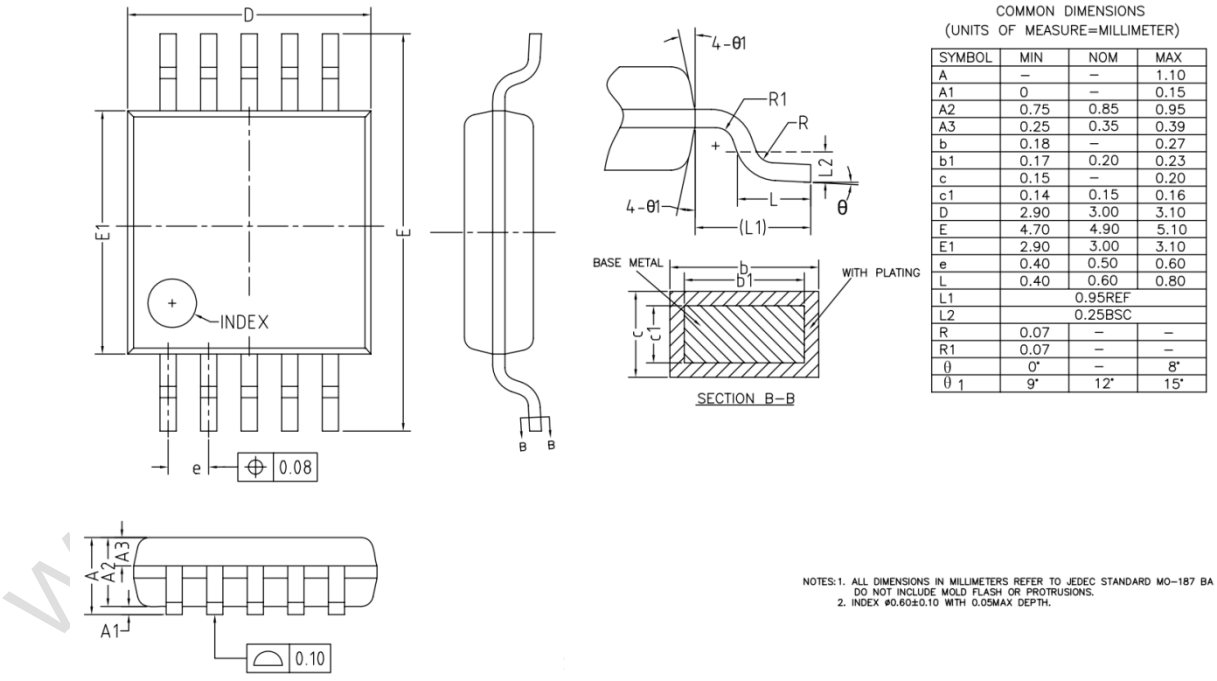
PACKAGE OUTLINE (DFN10L-3.0x3.0)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30
L/F载体尺寸 (mil)	106*75		

PACKAGE OUTLINE (MSOP10L)

10-Pin MSOP Package Outine Diagram



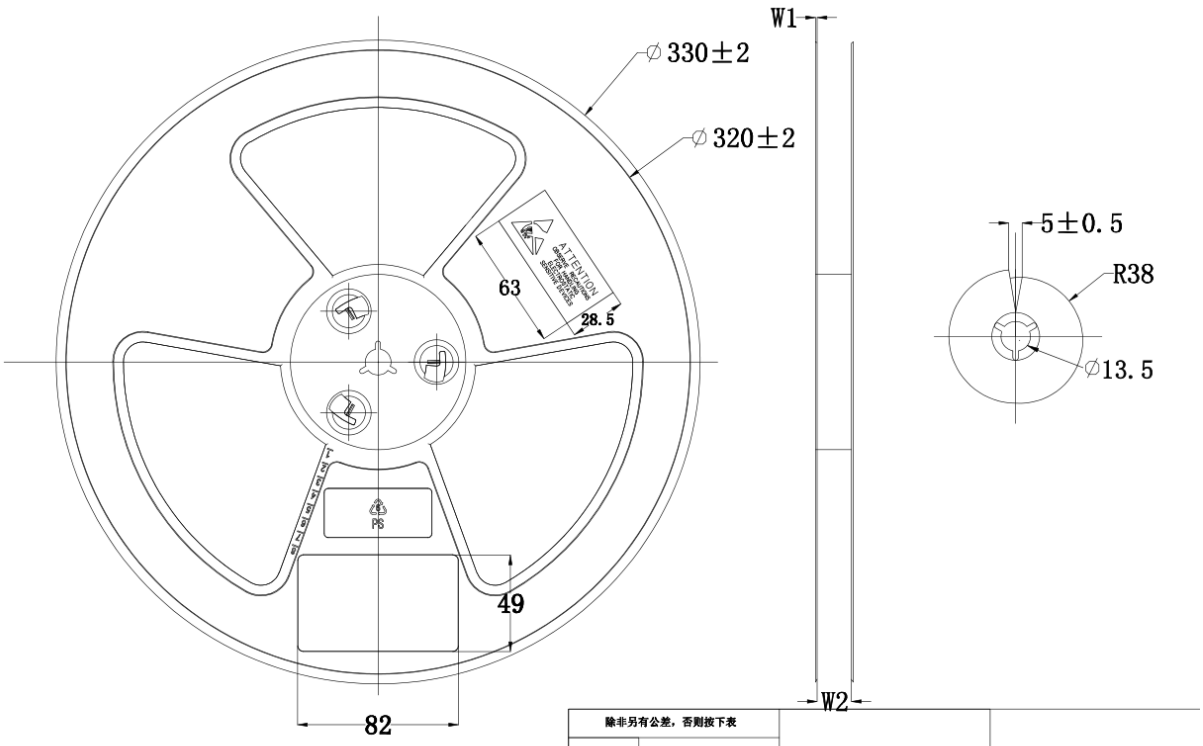
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0	–	0.15
A2	0.75	0.85	0.95
A3	0.25	0.35	0.39
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.40	0.50	0.60
L	0.40	0.60	0.80
L1	0.95REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ 1	9°	12°	15°

NOTES:1. ALL DIMENSIONS IN MILLIMETERS REFER TO JEDEC STANDARD MO-187 BA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. INDEX ø0.60±0.10 WITH 0.05MAX DEPTH.

TAPE AND REEL INFORMATION（DFN10L-3.0x3.0）

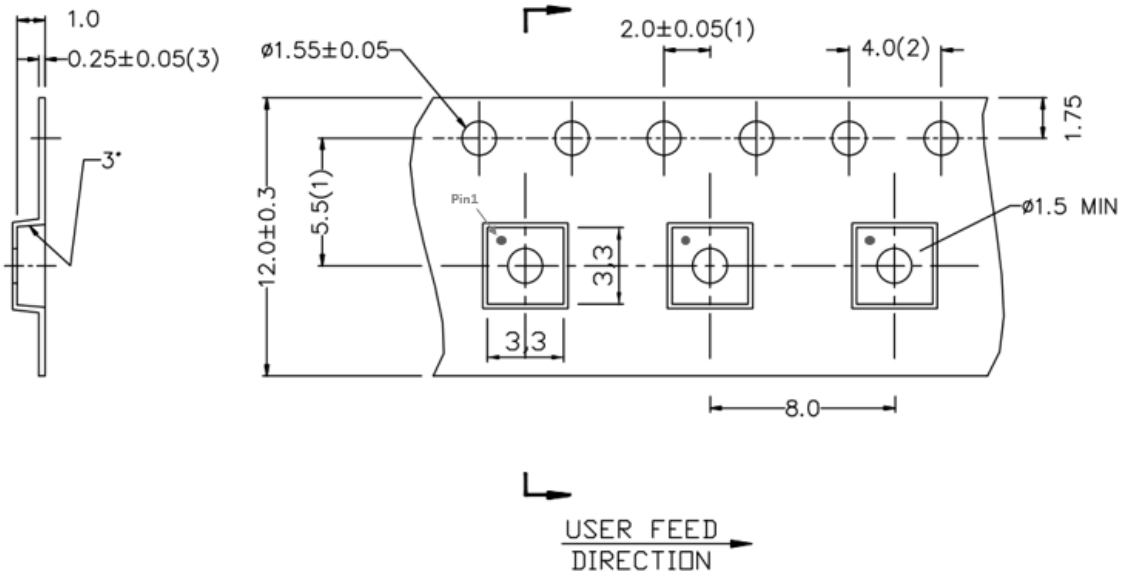
REEL



名称	W1	W2
13x12	1.8±0.2	12.7±0.2
13x16	1.8±0.2	16.3±0.2
13x24	1.8±0.2	24.1±0.2

除非另有公差，否则按下表								
尺寸标注	公差		13侧片					
	长度	角度						
X.	±0.5	0						
X.X	±0.3	0	型号		材料	聚苯乙烯	抗静电值	
X.X.X	±0.25	0	图号		颜色	浅蓝	用量	
设计			文件位置					
审核			版本	A	比例		单位	MM	图幅	A4
批准			第三角度投影				第1张共1张	

TAPE



产品订购信息

器件编号	产品丝印	工作温度范围	封装信息	湿敏等级	环保信息	包装方法
ASW3221DNG	A3221D XXXXXX(1) YYWW(2)ZZ(3)	-40°C 至 +125°C	DFN10L- 3.0x3.0	MSL-3	RoHS & Green	卷带和卷盘 (每卷 5000 只)
ASW3221MSOG	A3221M XXXXXX(1) YYWW(2)ZZ(3)	-40°C 至 +125°C	MSOP10L	MSL-3	RoHS & Green	卷带和卷盘 (每卷 3000 只)

备注：(1) XXXXXX 表示批次号，可变。(2) YYWW 表示年周号，可变。(3) ZZ 表示制造厂代码。
(2) ASW3221MSOG 暂无样品。