4 路差分 1:2 或 2:1 双向多路复用器/多路解复用器

特征

1) 开关类型：2:1 或 1:2
2) 动态特性
   - 差分带宽（-3dB）
     - 端口 A：典型值 9.5GHz
     - 端口 B：典型值 9.5GHz
   - 串扰（1.7GHz 时）：-30dB
   - 隔离（1.7GHz 时）：-31dB
   - 插入损耗（DC）
     - 端口 A：-0.5dB
     - 端口 B：-0.5dB
   - 回波损耗（1.7GHz 时）：-20dB
   - 对内（位-位）偏斜
     - 端口 A：2ps
     - 端口 B：6ps
   - R_{ON}
     - 端口 A：6.0 Ω
     - 端口 B：6.0 Ω
   - C_{ON}（1GHz 时）：典型值 0.5pF
3) V_{CC} 范围：1.65V 至 5.0V
4) 高速开关 I/O 电压范围：0V 至 2.0V
5) 带关断功能
6) 静电放电（ESD）性能
   - 2kV 人体放电模式
   - 1kV 组件充电模式
7) 42 引脚超薄型四方扁平无引线（LGA）封装
   - 9mm * 3.5mm，0.5mm 间距

应用

- PCIE 3.0 信号开关，8.0GT/s
- PCIE 4.0 信号开关，16.0GT/s
- 通用高速信号开关

描述

ASW3810 是一款 4 路差分 1:2 或 2:1 双向多路复用器/多路解复用器。ASW3810 可由 1.65V 至 5.0V 的电源供电，适用于电池供电的应用。该器件的导通电阻（R_{ON}）较低并且 I/O 电容较小，能够实现典型值高达 9.5GHz 的带宽。该器件虽然专为 PCIe 3.0 或 4.0 应用而设计，不过也支持多种差分幅值 小于 $2V_{PP}$ 且共模电压小于 2V 的其他高速数据协议，如 USB 3.2 和 DP 1.4 等。

ASW3810 具有断电模式，该模式下所有通道均具有高阻抗（Hi-Z）并且功耗极低。

简化的功能框图

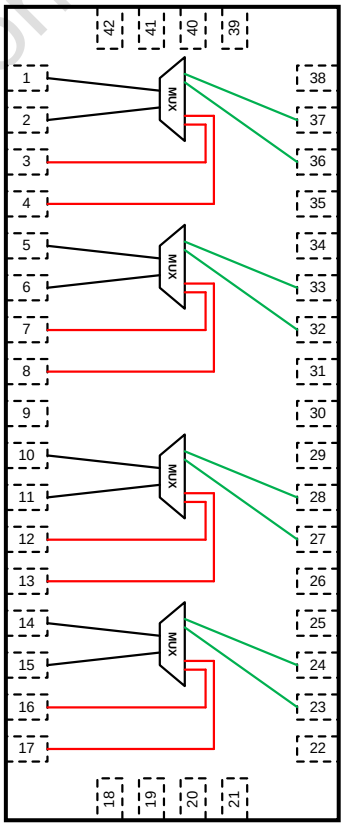


图 1, 简化的功能框图

修改历史记录

注：之前版本的页码可能与当前版本有所不同。

版本	修改日期	修改内容
V01	2022/1/30	初始版本完成。
V02	2022/5/2	1、 增加卷带和卷盘的信息； 2、 增加焊盘布局和焊锡膏示意图 1 和焊锡膏示意图 2。
V03	2022/8/9	更新 Differential Bandwidth (-3dB)、XTALK、OISO 的测试图及对应的测试数据。
V04	2023/2	更新丝印信息。
V05	2023/4	1、更新 Differential Bandwidth 、T_{SWITCH}和 T_{on}。 2、增加湿敏等级和卷盘 Pin1 脚位置说明。
V06	2023/6	增加 PCIe3.0 眼图测试图。
V07	2023/7	增加 PCIe4.0 眼图测试图。
V08	2023/12	1、增加 PCIe3.0/ PCIe4.0 治具(Bert)眼图测试图； 2、更新了产品订购信息中的器件编号和丝印信息； 3、更新了 t_{SKEW} 的描述；

PIN DIAGRAM

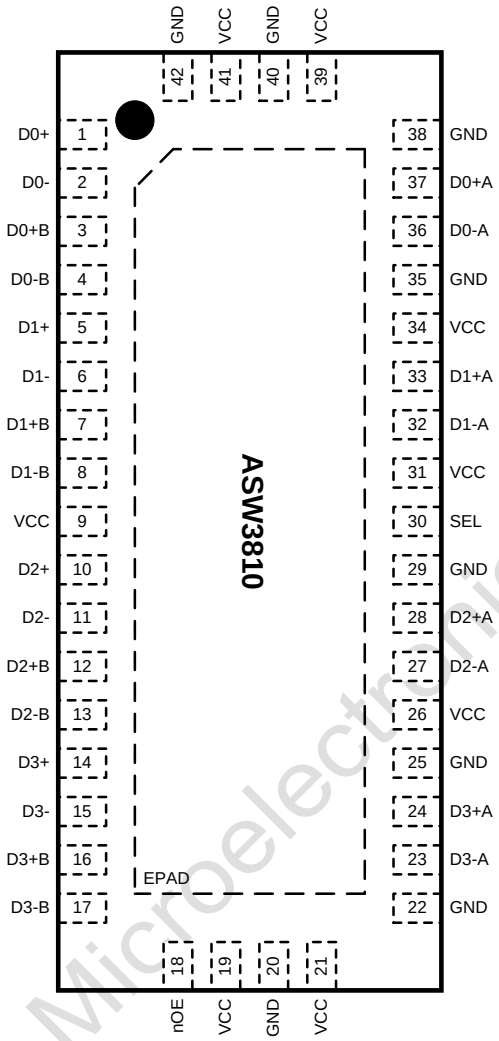


Figure 2，Pin Diagram (Top View)

PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	PIN DESCRIPTIONS
1	D0+	IN/OUT	Common Port, Channel 0, High-Speed Positive Signal
2	D0-	IN/OUT	Common Port, Channel 0, High-Speed Negative Signal
3	D0+B	IN/OUT	Port B, Channel 0, High-Speed Positive Signal
4	D0-B	IN/OUT	Port B, Channel 0, High-Speed Negative Signal
5	D1+	IN/OUT	Common Port, Channel 1, High-Speed Positive Signal
6	D1-	IN/OUT	Common Port, Channel 1, High-Speed Negative Signal
7	D1+B	IN/OUT	Port B, Channel 1, High-Speed Positive Signal
8	D1-B	IN/OUT	Port B, Channel 1, High-Speed Negative Signal
9	VCC	Power	Power Supply Voltage
10	D2+	IN/OUT	Common Port, Channel 2, High-Speed Positive Signal
11	D2-	IN/OUT	Common Port, Channel 2, High-Speed Negative Signal
12	D2+B	IN/OUT	Port B, Channel 1, High-Speed Positive Signal
13	D2-B	IN/OUT	Port B, Channel 1, High-Speed Negative Signal
14	D3+	IN/OUT	Common Port, Channel 3, High-Speed Positive Signal
15	D3-	IN/OUT	Common Port, Channel 3, High-Speed Negative Signal
16	D3+B	IN/OUT	Port B, Channel 3, High-Speed Positive Signal
17	D3-B	IN/OUT	Port B, Channel 3, High-Speed Negative Signal
18	nOE	IN	Output Enable, Active Low
19	VCC	Power	Power Supply Voltage
20	GND	Ground	Ground
21	VCC	Power	Power Supply Voltage
22	GND	Ground	Ground
23	D3-A	IN/OUT	Port A, Channel 3, High-Speed Negative Signal
24	D3+A	IN/OUT	Port A, Channel 3, High-Speed Positive Signal
25	GND	Ground	Ground
26	VCC	Power	Power Supply Voltage
27	D2-A	IN/OUT	Port A, Channel 2, High-Speed Negative Signal
28	D2+A	IN/OUT	Port A, Channel 2, High-Speed Positive Signal
29	GND	Ground	Ground
30	SEL	IN	Select Input
31	VCC	Power	Power Supply Voltage
32	D1-A	IN/OUT	Port A, Channel 1, High-Speed Negative Signal
33	D1+A	IN/OUT	Port A, Channel 1, High-Speed Positive Signal
34	VCC	Power	Power Supply Voltage
35	GND	Ground	Ground
36	D0-A	IN/OUT	Port A, Channel 0, High-Speed Negative Signal
37	D0+A	IN/OUT	Port A, Channel 0, High-Speed Positive Signal
38	GND	Ground	Ground
39	VCC	Power	Power Supply Voltage
40	GND	Ground	Ground
41	VCC	Power	Power Supply Voltage
42	GND	Ground	Ground
0	EPAD	Ground	Ground

Note: The positive and negative pin labels are the name label distinction, and the chip does not distinguish between positive and negative.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETERS	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	-0.5	5.5	V
V_{SW-HS}	High Speed Switch I/O Voltage Range	-0.5	2.1	V
V_{IN}	Digital Input Voltage Range (SEL, nOE)	-0.5	5.5	V
$I_{I/OK}$	Analog Port Diode Current, $V_{I/O}$ < 0V		-50	mA
I_{IK}	Digital Input Clamp Current, V_{IN} < 0V		-50	mA
I_{SW}	On-State Switch Current	-128	128	mA
ESD	HBM Model		±2.0	KV
	CDM Model		±1.0	KV
T_{STG}	Storage Temperature	-65	+150	°C

Note:
(1) The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
(2) V_{SW} refers to analog data switch paths.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. GrandMicro does not recommend exceeding them ot designing to Absolute Maximum Ratings.

SYMBOL	PARAMETERS	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	1.65	5.0	
$t_{RAMP(VCC)}$	Power Supply Slew Rate	100	1000	μs/V
V_{IN}	Control Input Voltage (SEL, nOE)(3)	0	5.0	V
V_{SW-HS}	High Speed Switch I/O Voltage	0	2.0	V
T_A	Operating Temperature	-40	+85	°C

Note:
(3) The control inputs must be held HIGH or LOW, they must not float.

DC ELECTRICALS

All typical values are at T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITION(4)	MIN	TYP	MAX	UNIT
PORT A							
R_{ON}	ON-state Resistance	D0 to D3	V_{CC} = 3V, 1.5V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40mA		6.0	9.5	Ω
$R_{ON(flat)}$(5)	ON-state resistance flatness	D0 to D3	V_{CC} = 3V, 1.5V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40mA		0.9		Ω
$\triangle R_{ON}$(6)	ON-state resistance match between high-speed channels	D0 to D3	V_{CC} = 3V, 1.5V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40mA		0.2	0.5	Ω
I_{OFF}	Leakage under power off	D0 to D3	V_{CC} = 0V, $V_{I/O}$ = 0V to 3.6V, V_{IN} = 0V to 5.5V			±1	μA
PORT B							
R_{ON}	ON-state Resistance	D0 to D3	V_{CC} = 3V, 1.5V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40mA		6.0	9.5	Ω
$R_{ON(flat)}$(5)	ON-state resistance flatness	D0 to D3	V_{CC} = 3V, 1.5V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40mA		0.9		Ω
$\triangle R_{ON}$(6)	ON-state resistance match between high-speed channels	D0 to D3	V_{CC} = 3V, 1.5V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40mA		0.2	0.5	Ω
I_{OFF}	Leakage under power off	D0 to D3	V_{CC} = 0V, $V_{I/O}$ = 0V to 3.6V, V_{IN} = 0V to 5.5V			±1	μA
DIGITAL INPUTS (SEL, nOE)							
V_{IH}	Control Input Voltage High	SEL, nOE		1.4			V
V_{IL}	Control Input Voltage Low	SEL, nOE				0.5	V
I_{IH}	Digital Input High Leakage Current	SEL, nOE	V_{CC} = 3.6V, V_{IN} = V_{CC}			±1	μA
I_{IL}	Digital Input Low Leakage Current	SEL, nOE	V_{CC} = 3.6V, V_{IN} = GND			±1	μA
SUPPLY							
I_{CC}	VCC Supply Current		V_{CC} = 3.6V, $I_{I/O}$ = 0, Normal Operation Model, nOE = L		25		μA
$I_{CC,PD}$	VCC Supply Current in Power-Down Mode		V_{CC} = 3.6V, $I_{I/O}$ = 0, Power-Down Model, nOE = H		0.1	1	μA

Note:
(4) V_I, V_O, I_I and I_O refer to I/O pins, and V_{IN} refers to the control pins.
(5) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(6) $\triangle R_{ON}$ is the difference of R_{ON} from center port to any other ports.

AC ELECTRICALS

All typical values are at T_A=25°C,V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Digital Input Capacitance		f = 1MHz, V_{IN} = 0V		6		pF
C_{OFF}	Switch OFF Capacitance		f = 1GHz, $V_{I/O}$ = 0V, Output is open, Switch is OFF		0.3		pF
C_{ON}	Switch ON Capacitance		f = 1GHz, $V_{I/O}$ = 0V, Output is open, Switch is ON		0.5		pF
X_{TALK}	Differential Crosstalk		R_L = 50 Ω at 1.7GHz, See Figure 20		-30		dB
			R_L = 50 Ω at 2.7GHz, See Figure 20		-28.5		
			R_L = 50 Ω at 4.05GHz, See Figure 20		-30		
O_{ISO}	Differential OFF Isolation		R_L = 50 Ω at 1.7GHz, See Figure 21		-31		dB
			R_L = 50 Ω at 2.7GHz, See Figure 21		-25.5		
			R_L = 50 Ω at 4.05GHz, See Figure 21		-22.5		
IL	Insertion Loss		Port A at DC		-0.5		dB
			Port B at DC		-0.5		
BW	Differential Bandwidth (-3dB)	Port A	R_L = 50 Ω, All Channels, See Figure 22		9.5		GHz
		Port B	R_L = 50 Ω, All Channels, See Figure 22		9.5		

SWITCHING ELECTRICALS

All typical values are at T_A=25°C, V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}(7)	Switch Turn-ON Time		All I/O	See Figure 17		19		µs
t_{SWITCH}(8)	Switching time between channels		All I/O	See Figure 18		250		ns
t_{pd}	Propagation Delay	Port A	D0 to D3	See Figure 19		30		ps
		Port B	D0 to D3			30		
t_{SKEW}	Inter-pair Skew	Port A	D0 to D3	Bit-to-Bit Skew Within Same Differential Pair		2		ps
		Port B				2		
	Intra-pair Skew	Port A		Between channel 0, 1, 2, 3		2		
		Port B				6		

Note:
(7) t_{ON} is the time it takes the output to recover after enabling switches.
(8) t_{SWITCH} is the time it takes for the output to recover after the state us changed.

TYPICAL PERFORMANCES

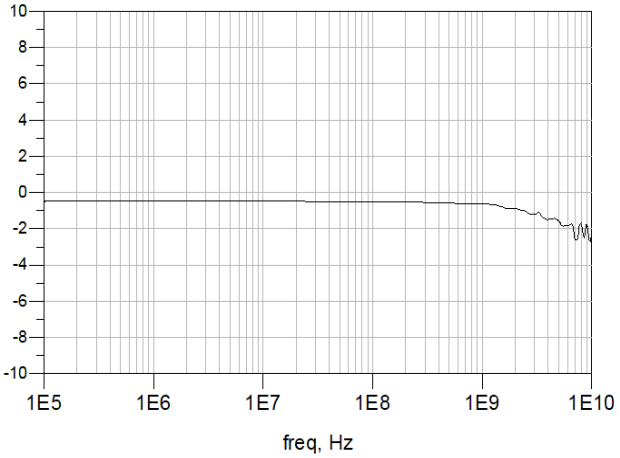


Figure 3, Differential S21 vs Frequency

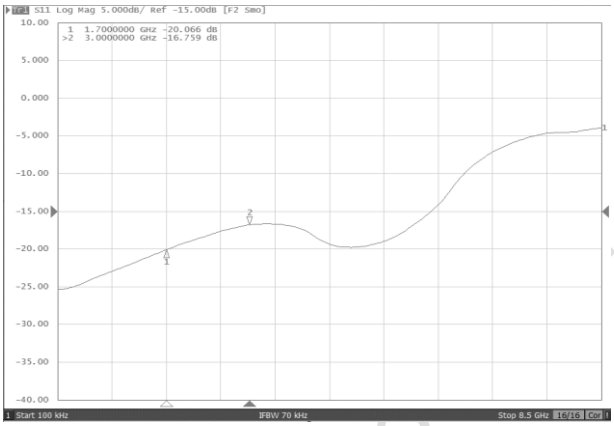


Figure 4, Return Loss

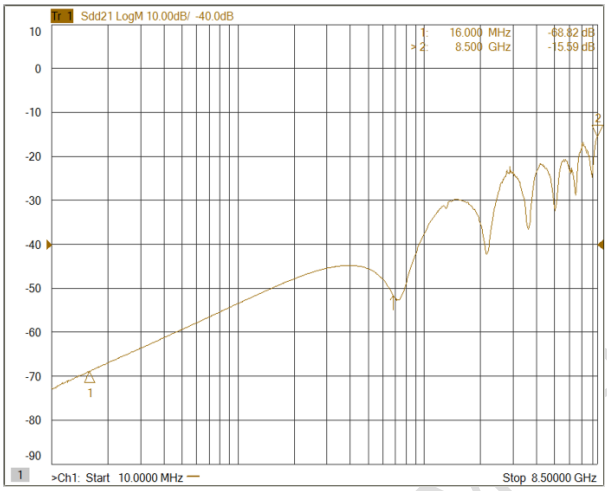


Figure 5, XTALK for Port A

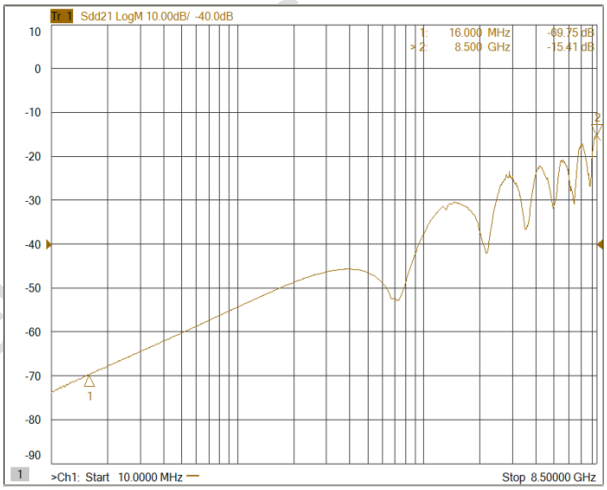


Figure 6, XTALK for Port B

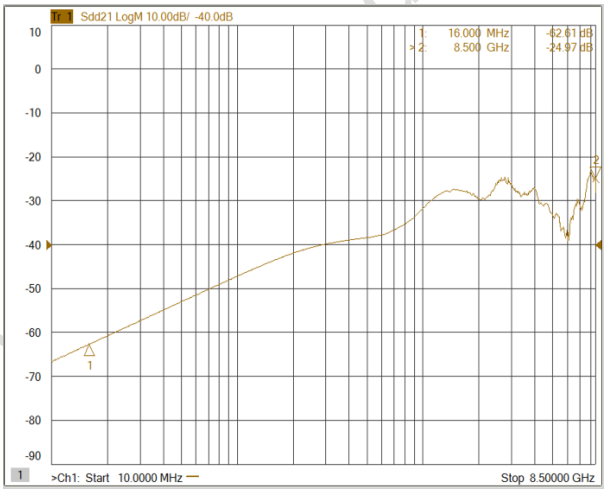


Figure 7, Off-State Isolation (OISO) for Port A

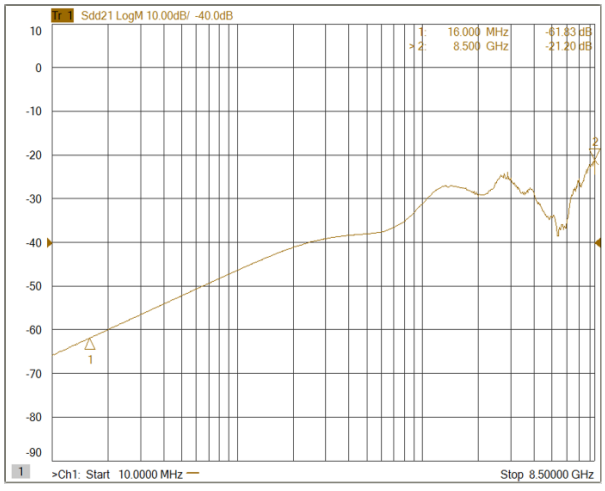


Figure 8, Off-State Isolation (OISO) for Port B

Figure 9, PCIe3.0 Eye diagram test,
8Gbps, Vpp=1V, No Device through Path

Figure 10, PCIe3.0 Eye diagram test,
8Gbps, Vpp=1.3V, No Device through Path

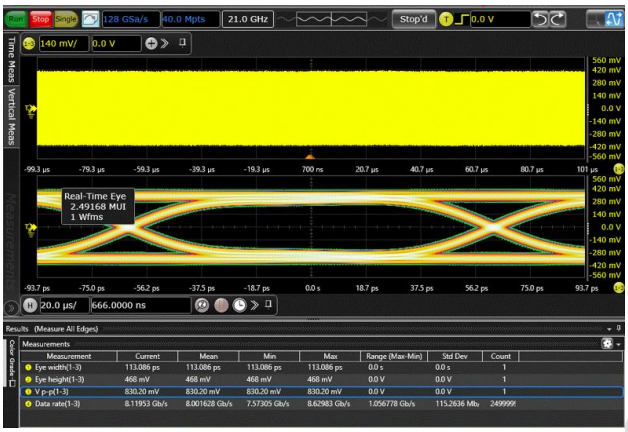


Figure 11, PCIe3.0 Eye diagram test,
8Gbps,Vpp=1V, With Device

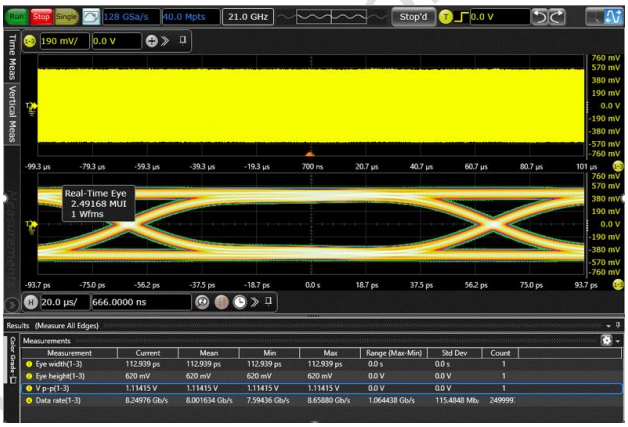


Figure 12, PCIe3.0 Eye diagram test,
8Gbps,Vpp=1.3V, With Device

Figure 13, PCIe4.0 Eye diagram test, 16Gbps, Vpp=1V, No Device through Path

Figure 14, PCIe4.0 Eye diagram test, 16Gbps, Vpp=1.3V, No Device through Path

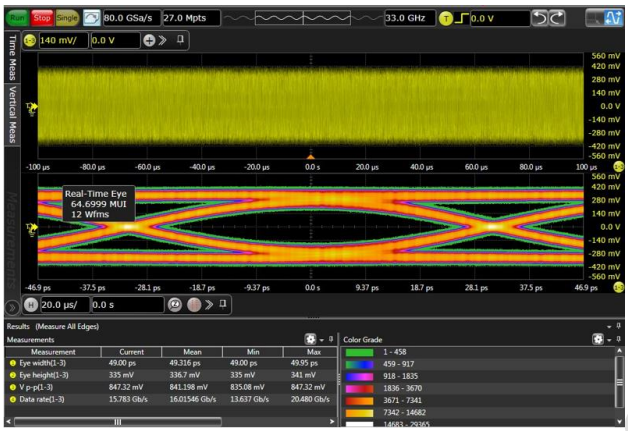


Figure 15, PCIe4.0 Eye diagram test, 16Gbps,Vpp=1V, With Device

Figure 16, PCIe4.0 Eye diagram test, 16Gbps,Vpp=1.3V, With Device

TEST CIRCUITS

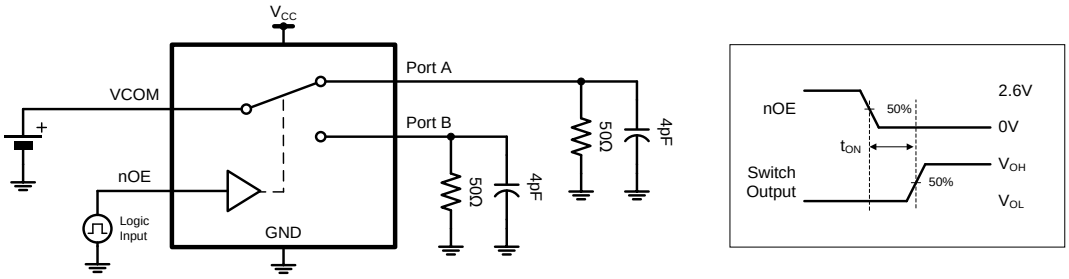


Figure 17, Switch Turn-On Time (t_{ON})

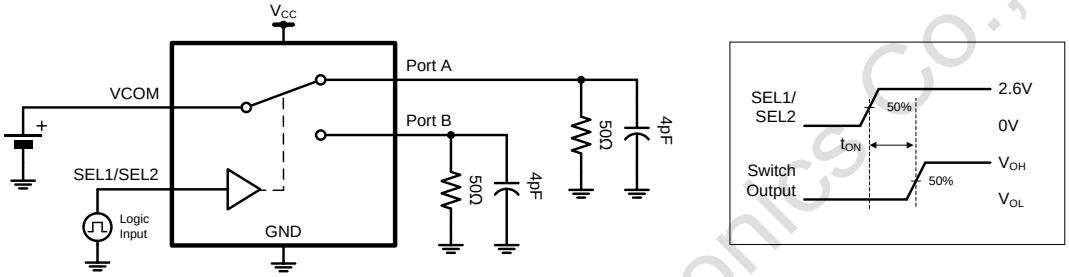
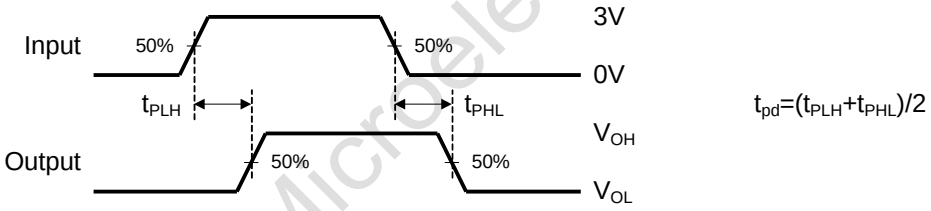


Figure 18, Switching Time between Channels (t_{SWITCH})



$t_{pd}=(t_{PLH}+t_{PHL})/2$

Figure 19, Propagation Delay (t_{pd})

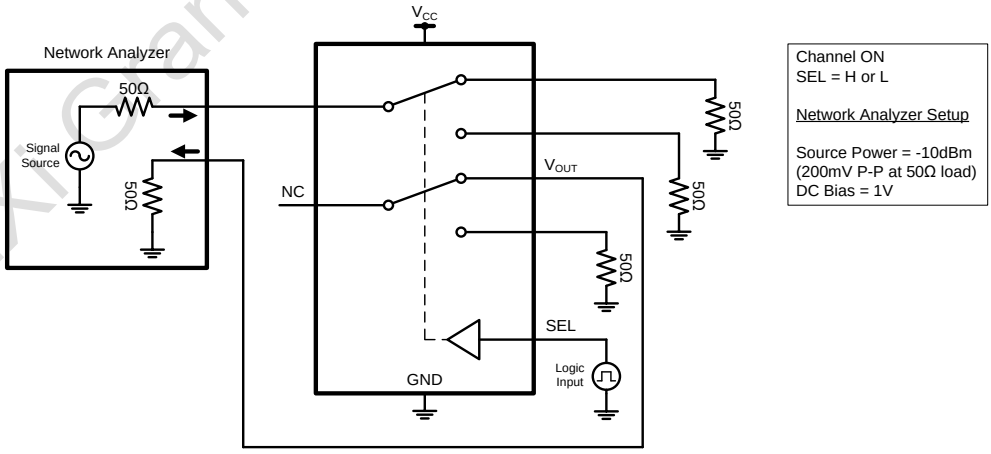


Figure 20, Crosstalk (X_{TALK})

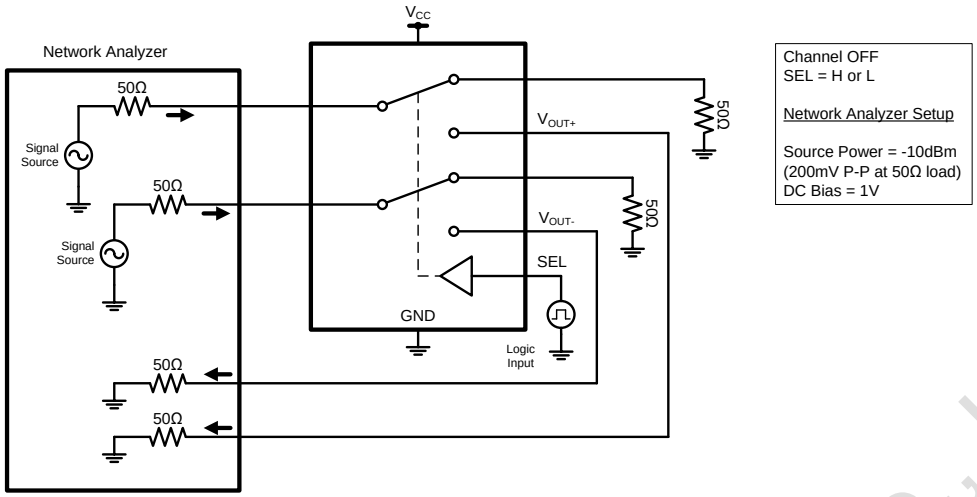


Figure 21, Differential Off-Isolation (O_{ISO})

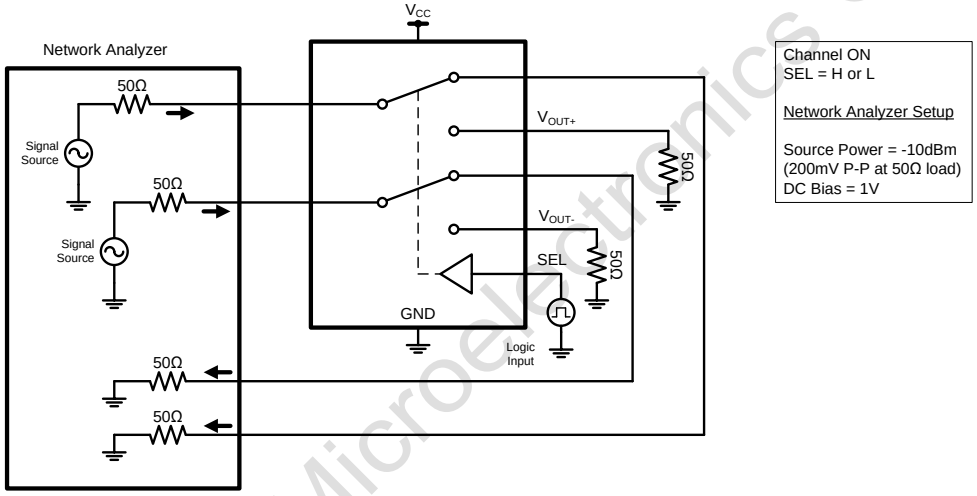


Figure 22, Differential Bandwidth (BW)

FUNCTION DESCRIPTIONS

1. Overview

ASW3810 is a 8-channel 1:2 or 2:1 bidirectional multiplexer/de-multiplexer. The ASW3810 operates from a 1.65V to 5.0V supply, making it suitable for battery-powered applications. It offers low and flat on-state resistance as well as low I/O capacitance which allows it to achieve a typical bandwidth of up to 9.5GHz. The device provides the high bandwidth necessary for PCIe 3.0 or PCIe 4.0 applications.

2. Functional Block Diagram

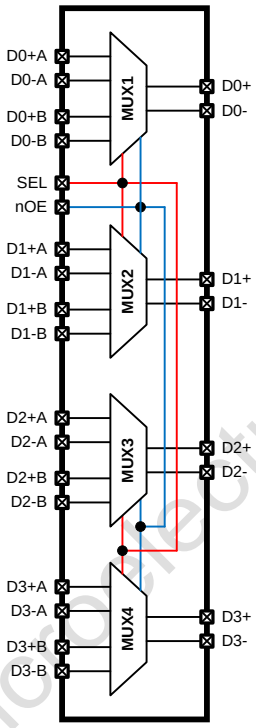


Figure 23, Functional Block Diagram

3. Feature Description

The ASW3810 uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. ASW3810 has 8-channel bidirectional switches with a high bandwidth (~9.5GHz). ASW3810 uses an extremely low power technology and uses only 24μA I_{CC} in active mode. The device has integrated ESD that can support up to 2kV Human-Body-Model (HBM) and 1kV Charge Device Model (CDM). ASW3810 can support high-speed analog I/O signal in 0V to 2.0V range. ASW3810 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature prevents leakage current in the device. The ASW3810 is not designed for passing signals with negative swings; the high-speed signals need to be properly DC biased (usually ~1V) before being passed to the ASW3810. The differential S_{21} characteristics as a function of frequency for Port A and Port B are shown in Figure 3, respectively. The figures show a differential bandwidth of 9.5GHz for Port A and Port B. The return loss characteristics (S_{11}) are shown in Figure 4. The cross-talk (X_{TALK}) characteristics as a function of frequency are shown in Figure 5 and Figure 6, respectively. The off-state isolation (O_{ISO}) characteristics for Port A and Port B are shown in Figure 7 and Figure 8 respectively.

4. Device Functional Models

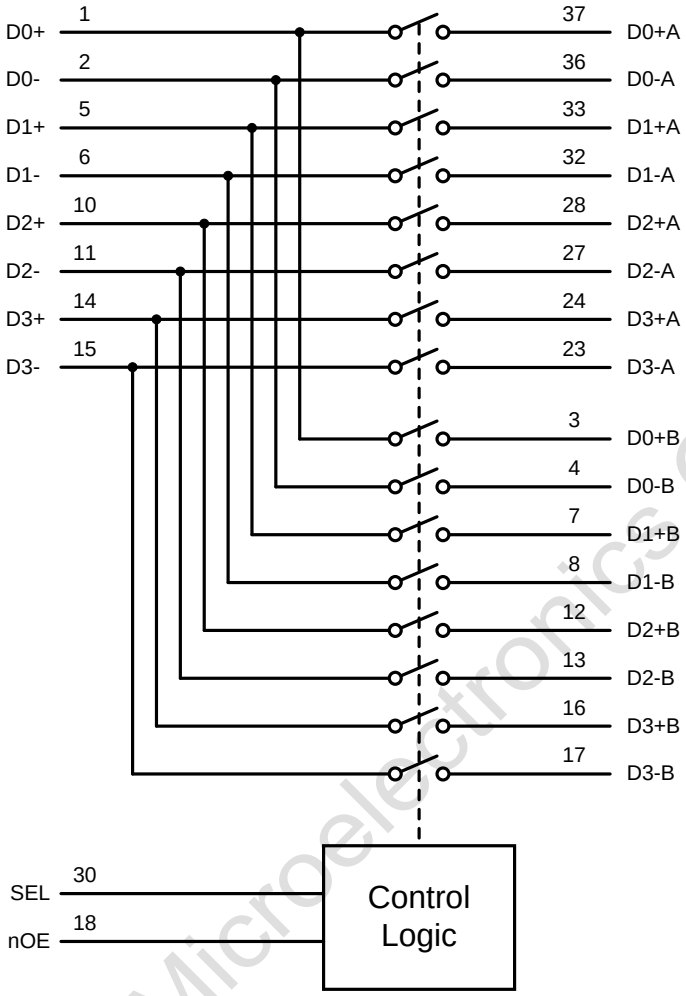


Figure 24, Logic Diagram

Table 1 lists the device functions for the ASW3810 device.

Table 1, Functional Table

nOE	SEL	FUNCTION
H	X	Switch disabled. All channels are Hi-Z.
L	L	All A channels are enabled. All B channels are Hi-Z.
L	H	All B channels are enabled. All A channels are Hi-Z.

TYPICAL APPLICATION DIAGRAM

1. AC Couple Caps

The ASW3810 does not drive out a fixed DC common mode voltage, but it can support 0V to 2V common mode range on 16Gbps high speed signals. According to the specification, the PCI Express bus should be AC-Coupling signals and AC couple
capacitors are requested on Transmitter signals.

For the compatibility, how to use the AC couple capacitors is very important in mux switch application. It depends on the matching of common mode working range between two components.

The ASW3810 is a high-speed mux chip and requests to be forced a DC common mode within working range on differential pair. It can be forced by the component which is connecting to ASW3810, but the DC common mode range of this component has to meet the common mode range of ASW3810. When the DC common mode level of component and ASW3180 are requested. The pull-down resistors on the path of mux are necessary, once both side of ASW3810 mux signals use the AC couple capacitors.

There are several examples described as below. (Here it is assumed the transmitter of all devices design as AC-coupling mode)

1) When PCIE host drives the DC common mode within the range ASW3810's spec, it uses the DC coupling circuit between PCIE host and the ASW3810. Other buses of ASW3810 must be AC coupling circuit.

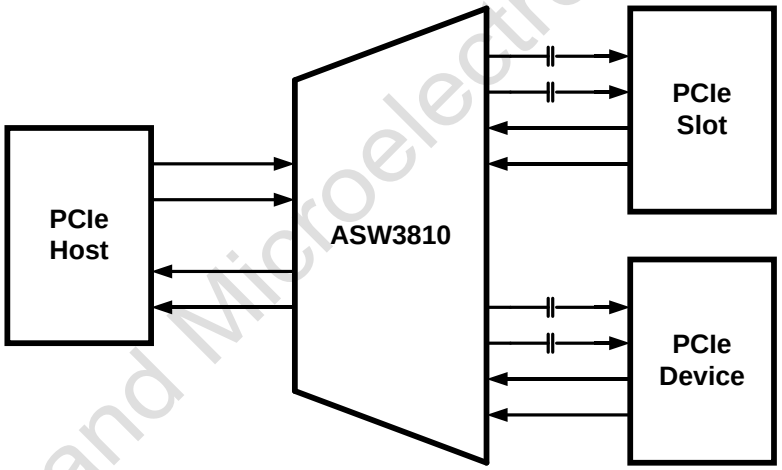


Figure 25，Example 1, PCIe Hosts DC common mode within ASW3810 range

2) Or both of host controllers force the DC common mode on ASW3810 when the DC common mode level is within the ASW3810's range.

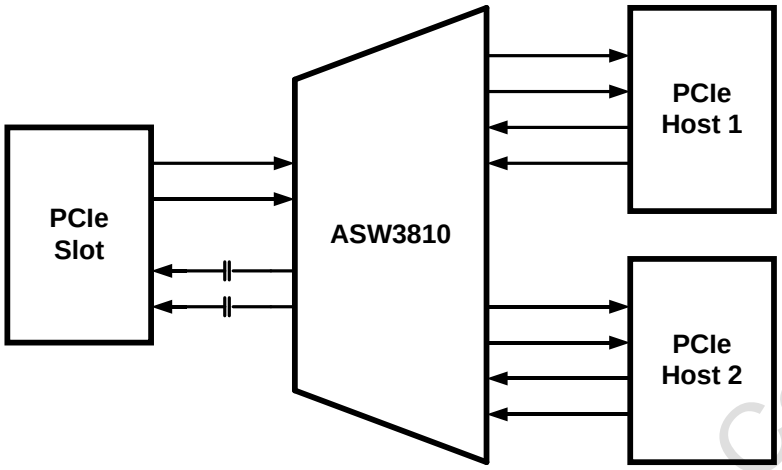


Figure 26，Example 2, DC common mode of both controllers within ASW3810 range

3) When PCIE host drives the DC common mode over the range of ASW3810's spec, it uses the AC coupling on all buses of ASW3810. A biasing voltage of less than 2V is required in this case.

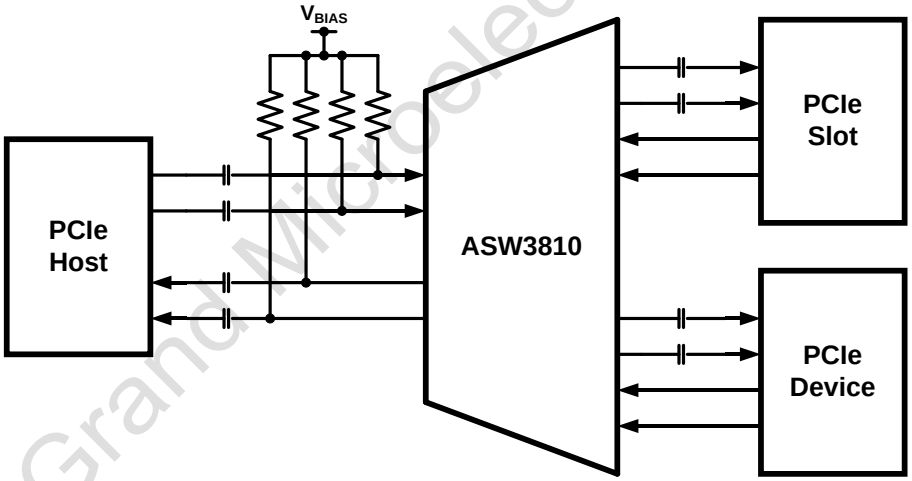
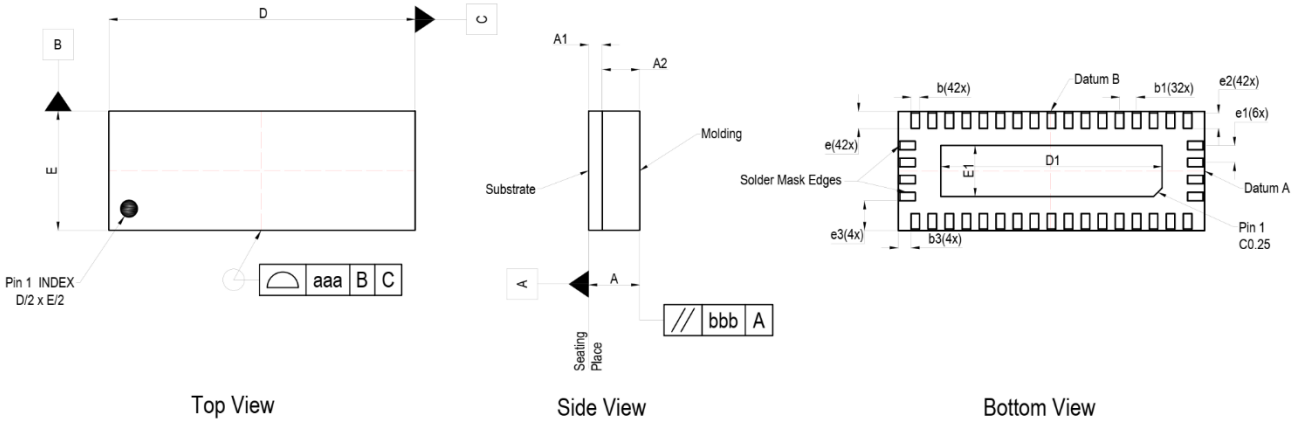


Figure 27，Example 3, PCIe host DC common mode level out of ASW3810 range

PACKAGE OUTLINES (LGA42-3.5x9.0x0.75)



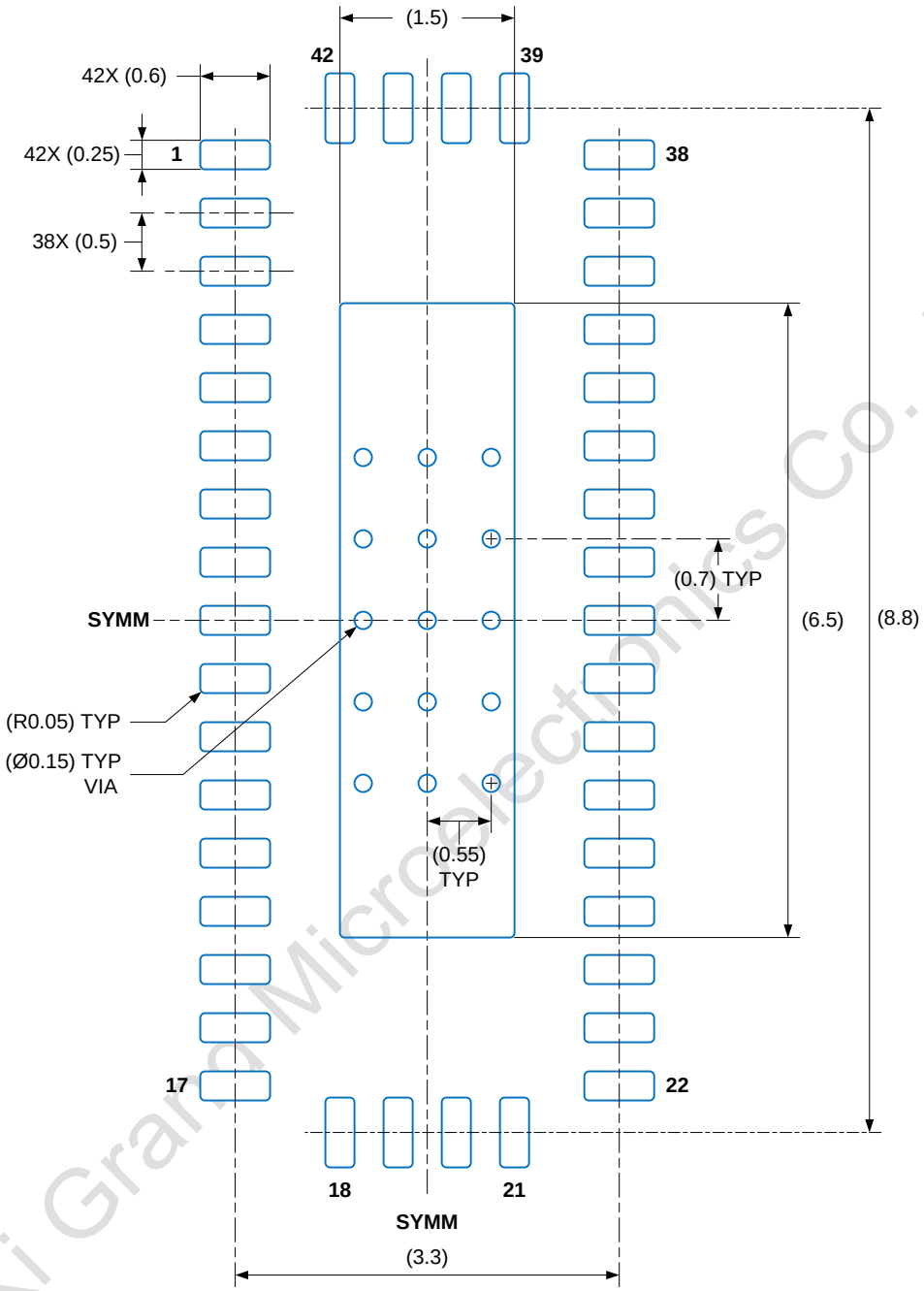
Top View　　Side View　　Bottom View

Dimensional References　　unit: mm

Ref.	MIN	NOR	MAX	Ref.	MIN	NOR	MAX
A	0.700	0.750	0.800	b	0.200	0.250	0.300
A1	0.170	0.200	0.230	e	0.450	0.500	0.550
A2	0.500	0.550	0.600	b1	0.450	0.500	0.550
D	8.900	9.000	9.100	e1	0.450	0.500	0.550
E	3.400	3.500	3.600	e2	0.400	0.450	0.500
D1	6.400	6.500	6.600	b3	0.325	0.375	0.425
E1	1.400	1.500	1.600	e3	0.825	0.875	0.925
aaa		0.100		bbb		0.200	

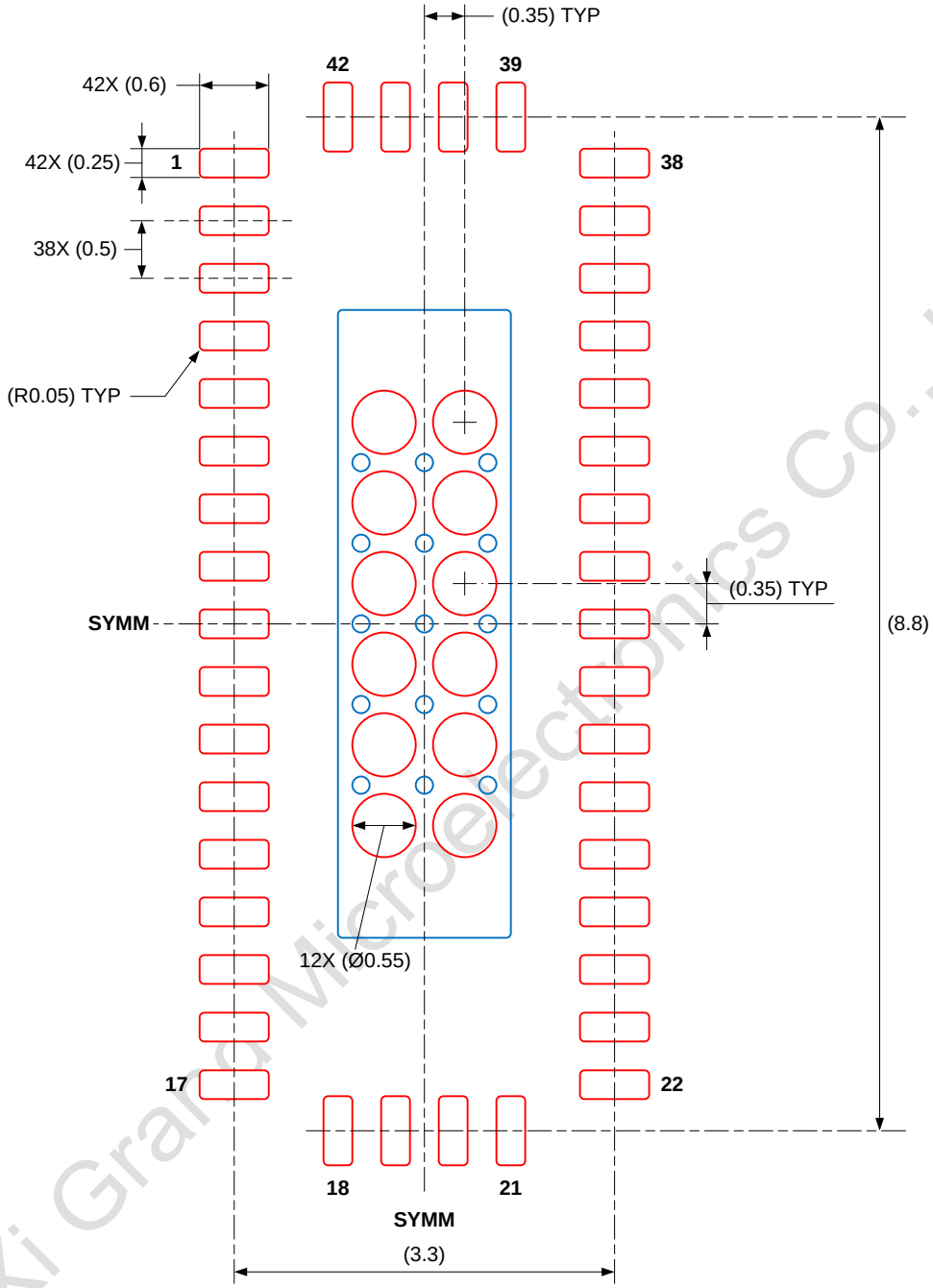
Note:
1. All dimension are in millimeter.
2. Dimension 'A' includes package warpage.
3. Exposed metallized pads are Cu pads with surface finish protection.

LAND PATTERN EXAMPLE



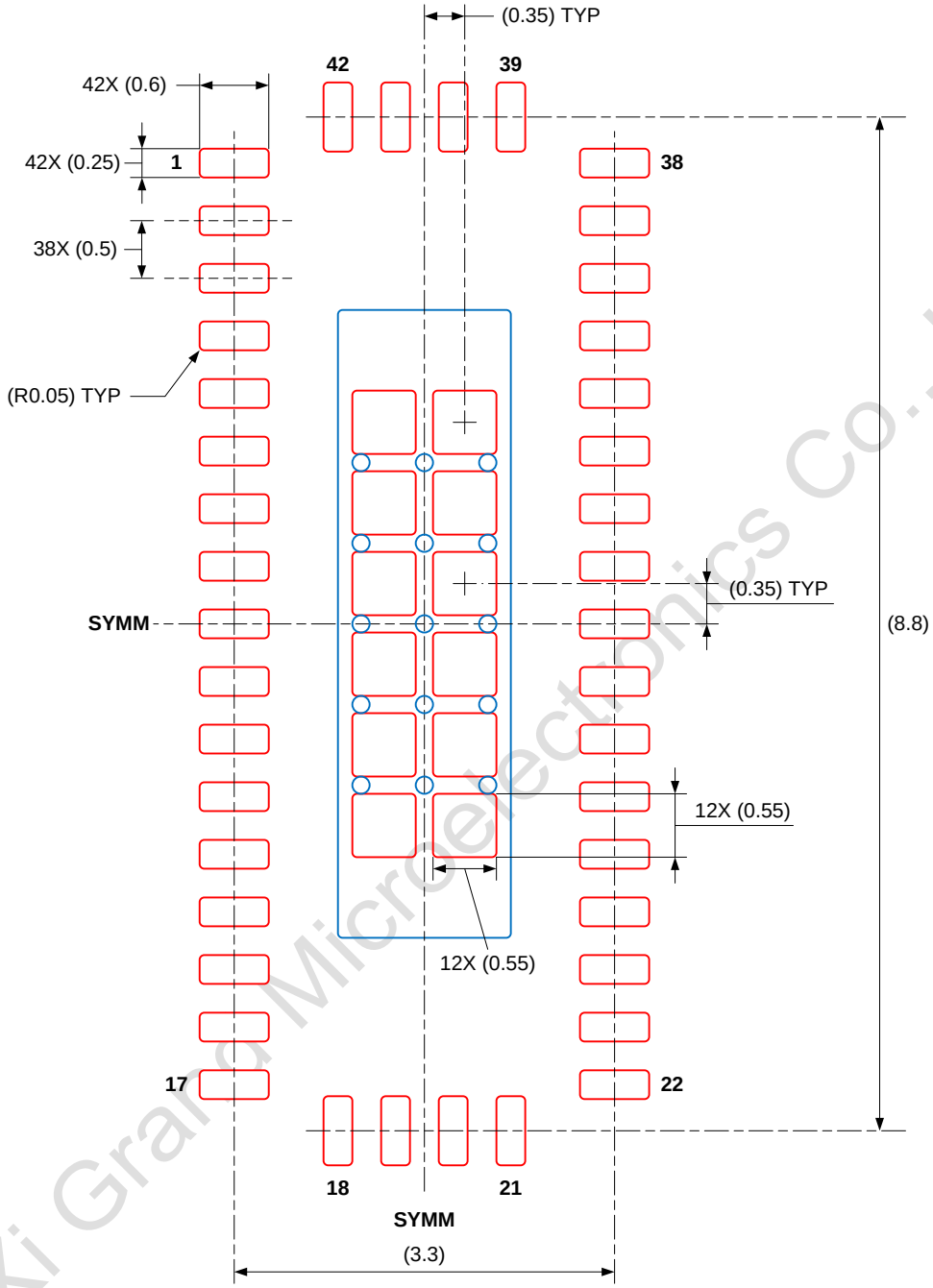
Notes:
1. All dimensions are in millimeters.
2. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE 1



Notes:
3. All dimensions are in millimeters.

SOLDER PASTE EXAMPLE 2

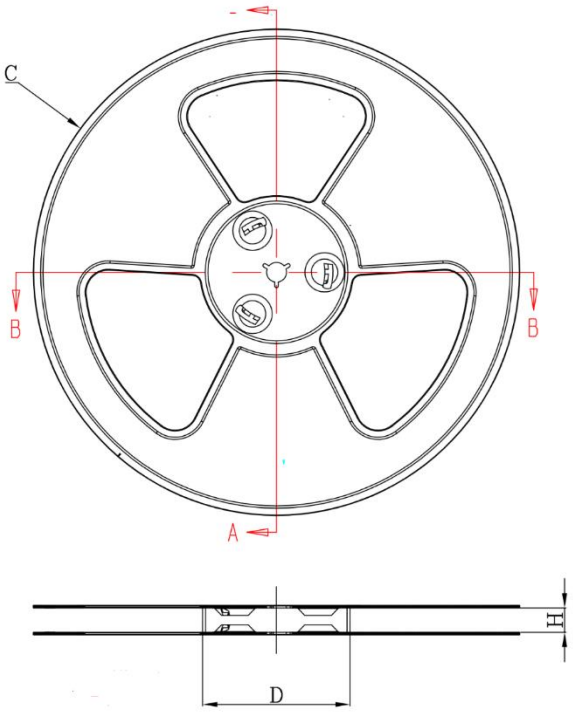


Notes:
4. All dimensions are in millimeters.

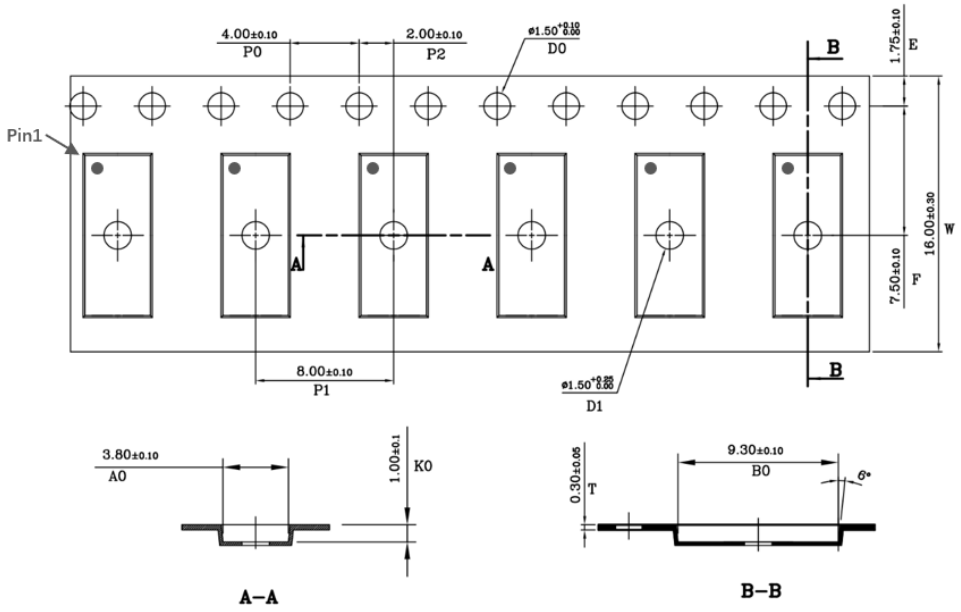
TAPE AND REEL INFORMATION

REEL

尺 寸 规 格 (UNIT:mm)									
项 目	H	D	C						
标 准	$16.50^{+0.4}_{-0.4}$	ø100±2.0	ø330±1.0						



TAPE



Note:

1. All Dimension Unit in mm.

PRODUCT ORDERING INFORMATIONS

Part Number	Package Drawing	Operating Temperature	Package Information	Moisture Sensitivity Level	ECO	Package Method
ASW3810 LGA42	ASW3810 LGA42G YYWWZZ(*)	-40°C to +85°C	LGA42-3.5x9.0	MSL-3	RoHS & Green	Tape & Reel (3000 Per Tape)

Note: (*)YY means Year, WW means Week, ZZ means manufacture code.