

## High-Speed USB 2.0 (480Mbps) DPDT Switch

### FEATURES

- $R_{ON}$  is typically  $6\Omega$  at  $V_{CC} = 3.3V$
- $V_{CC}$ : 1.65V to 4.5V
- Low Crosstalk:  $-45dB$  @ 250MHz
- Low Bit-to-Bit Skew: 50ps (typ.)
- Low Current Consumption:  $1.0\mu A$
- Near-Zero Propagation Delay: 250ps
- Channel On-Capacitance:  $3.5pF$  (typ.)
- Typical Bandwidth:  $> 750MHz$
- Break-Before-Make Switching
- Packages: QFN10-1.8x1.4 and MSOP10

### APPLICATIONS

- USB 2.0 Signal Routing
- Differential Signal Data Routing
- Digital Cameras and Camcorders
- Portable Instrumentation
- Set-Top Box
- PADS

### GENERAL DESCRIPTIONS

The ASW7227 is a high-speed, low-power double-pole double-throw (DPDT) analog switch that operates from a single 1.65V to 4.5V power supply.

The ASW7227 is designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os.

The ASW7227 has low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480Mbps). Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs.

The ASW7227 contains special circuitry on the D+/D- pins which allows the device to withstand a  $V_{BUS}$  short to D+ or D- when the USB devices are either powered off or powered on.

The ASW7227 is available in MSOP10 and UTQFN10L-1.4x1.8 packages. It operates over an ambient temperature range of  $-40^{\circ}C$  to  $+85^{\circ}C$ .

### BLOCK DIAGRAM

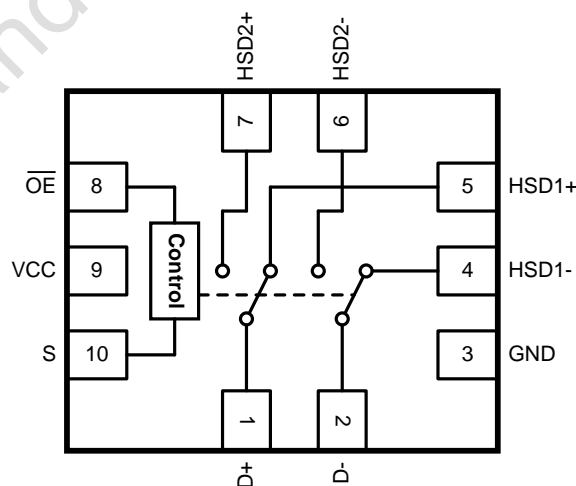


Figure 1, Block Diagram

## Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	CHANGE DATE	CHANGE ITEMS
V01	2021/3	Initial version completed.
V02	2021/10/1	Update Mark Information.
V03	2023/8/15	Update Pin Diagram. Add Tape and Reel information.

## PIN DIAGRAM

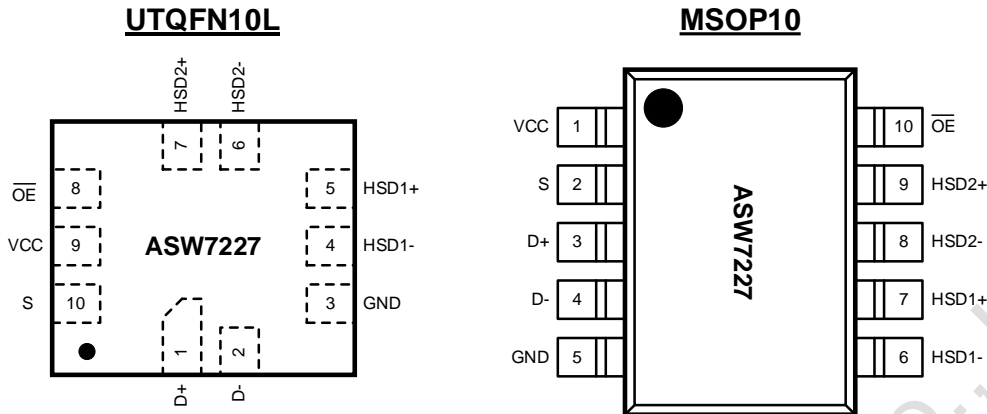


Figure 2, Pin Diagram (Top View)

## PIN DESCRIPTIONS

PIN No.		PIN NAME	TYPE	DESCRIPTIONS
UTQFN10L	MSOP10			
1	3	D+	I/O	USB Data Bus
2	4	D-	I/O	USB Data Bus
3	5	GND	GROUND	Ground
4	6	HSD1-	I/O	Multiplexed Source Inputs
5	7	HSD1+	I/O	Multiplexed Source Inputs
6	8	HSD2-	I/O	Multiplexed Source Inputs
7	9	HSD2+	I/O	Multiplexed Source Inputs
8	10	$\overline{\text{OE}}$	I	Output Enable, Active Low
9	1	VCC	POWER	Power Supply
10	2	S	I	Select Input

## FUNCTION TRUTH TABLE

c	S	HSD1+, HSD1-	HSD2+, HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	X	OFF	OFF

## Absolute Maximum Ratings

Stress exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{CC}$	Power Supply Voltage	-0.3	5.5	V
$V_{IS}$	Analog Input Voltage (HSDn+, HSDn-)	-0.3	$V_{CC} + 0.3$	V
	Analog Input Voltage (D+, D-)	-0.3	$V_{CC} + 0.3$	V
$V_{IN}$	Digital Select Input Voltage (S, $\overline{OE}$ )	-0.3	$V_{CC} + 0.3$	V
$I_{ANA1}$	Continuous DC Current from Dn to HSDn	$\pm 100$		mA
$I_{ANA-PK1}^{(1)}$	Peak Current from Dn to HSDn, 10% Duty Cycle $t_{ON} = 100\text{ms}$	$\pm 150$		mA
$I_{IN}$	Control Input Current, Output Enable Current	$\pm 20$		mA
ESD	HBM Model	$\pm 8$		KV
$T_{STG}$	Storage Temperature	-65	+150	$^{\circ}\text{C}$

**Notes:**

(1) Defined as 10% ON, 90% OFF Duty Cycle.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{CC}$	Power Supply Voltage	1.65	4.5	V
$V_{IN}$	Digital Select Input Voltage (S, $\overline{OE}$ )	0	$V_{CC}$	V
$V_{IS}$	Analog Input Voltage (HSD1+, HSD1-, HSD2+, HSD2-)	0	$V_{CC}$	V
	Analog Input Voltage (D+, D-)	0	4.5	
$T_A$	Operating Temperature	-40	+85	$^{\circ}\text{C}$

## ELECTRICAL CHARACTERISTICS

(All typical values are at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$  unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	$V_{CC}$ (V)	$T_A = 25^\circ C$			UNIT
				MIN	TYP	MAX	
<b>DIGITAL INPUTS</b>							
$V_{IH}$	Control Input Voltage High	S, $\overline{OE}$	2.7	1.3			V
			3.3	1.4			
			4.2	1.6			
$V_{IL}$	Control Input Voltage Low	S, $\overline{OE}$	2.7			0.4	V
			3.3			0.4	
			4.2			0.5	
$I_{IN}$	Control Input Leakage Current	$V_{IS} = V_{CC}$ or GND	1.65 - 4.5			$\pm 1.0$	$\mu A$
<b>SUPPLY AND LEAKAGE CURRENT</b>							
$I_{CC}$	Quiescent Supply Current	$V_{IS} = V_{CC}$ or GND, $I_{ON} = 0A$	1.65 - 4.5			1.0	$\mu A$
$I_{OFF}$	Power OFF Leakage Current	$V_{IS} = V_{CC}$ or GND	0			1.0	$\mu A$
$I_{OZ}$	OFF State Current	$V_{IS} = V_{CC}$ or GND, $\overline{OE} = V_{CC}$	1.65 - 4.5			1.0	$\mu A$
<b>LIMITED <math>V_{IN}</math> SWING ON RESISTANCE</b>							
$R_{ON}^{(1)}$	On-Resistance, (Figure 3)	$I_{ON} = 8mA$ , $V_{IS} = GND$ to 0.4V	3.3		6.0	10	$\Omega$
$R_{ONFLAT}^{(2)}$	On-Resistance Flatness (Figure 3)	$I_{ON} = 8mA$ , $V_{IS} = GND$ to 0.4V	3.3		0.5		$\Omega$
$\Delta R_{ON}^{(3)}$	On-Resistance match between channels (Figure 3)	$I_{ON} = 8mA$ $V_{IS1} = 1.5V$ ; $I_{ON} = 8mA$ $V_{IS2} = 1.5V$	3.3		0.2		$\Omega$
<b>TIMING/FREQUENCY (Typical: <math>V_{CC} = 3.3V</math>, <math>T_A = 25^\circ C</math>, <math>R_L = 50\Omega</math>, <math>C_L = 35pF</math>, <math>f = 1MHz</math>)</b>							
$t_{ON}$	Turn-On Time (Figure 4)	$V_{IS} = 0.8V$ , Closed to Open	1.65 - 4.5		14	30	ns
$t_{OFF}$	Turn-Off Time (Figure 4)	$V_{IS} = 0.8V$ , Open to Closed	1.65 - 4.5		10	20	ns
$t_{BBM}$	Break-Before-Make Delay (Figure 5)	$V_{IS} = 0V$ to $V_{CC}$ , $I_{ON} = 8mA$	1.65 - 4.5		2.45		ns
BW	-3dB Bandwidth (Figure 6)	$C_L = 5pF$	1.65 - 4.5		550		MHz
<b>ISOLATION (Typical: <math>V_{CC} = 3.3V</math>, <math>T_A = 25^\circ C</math>, <math>R_L = 50\Omega</math>, <math>C_L = 5pF</math>)</b>							
$O_{ISO}$	Off-Isolation (Figure 7)	$f = 250MHz$	1.65 - 4.5		-30		dB
$X_{TALK}$	Non-Adjacent Channel Crosstalk (Figure 8)	$f = 250MHz$ , HSDn+ to HSDn-	1.65 - 4.5		-45		dB
<b>CAPACITANCE (Typical: <math>V_{CC} = 3.3V</math>, <math>T_A = 25^\circ C</math>, <math>R_L = 50\Omega</math>, <math>C_L = 5pF</math>, <math>f = 1MHz</math>)</b>							
$C_{IN}$	Control Pin, Output Enable Input Capacitance	$V_{CC} = 0V$ , $f = 1MHz$			1.5		pF
$C_{ON}$	ON Capacitance (D+ to HSD1+ or HSD2+)	$V_{CC} = 3.3V$ , $f = 1MHz$ , $\overline{OE} = 0V$ , S = 0V or $V_{CC}$			3.5		pF
$C_{OFF}$	OFF Capacitance (HSD1n or HSD2n)	$V_{CC} = 3.3V$ , $f = 1MHz$ , $\overline{OE} = V_{CC}$ , S = 0V or $V_{CC}$			2.0		pF

### Notes:

1. Guaranteed by design.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
3.  $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$  between HSD1+ and HSD1- or HSD2+ and HSD2-.

TEST CIRCUITS

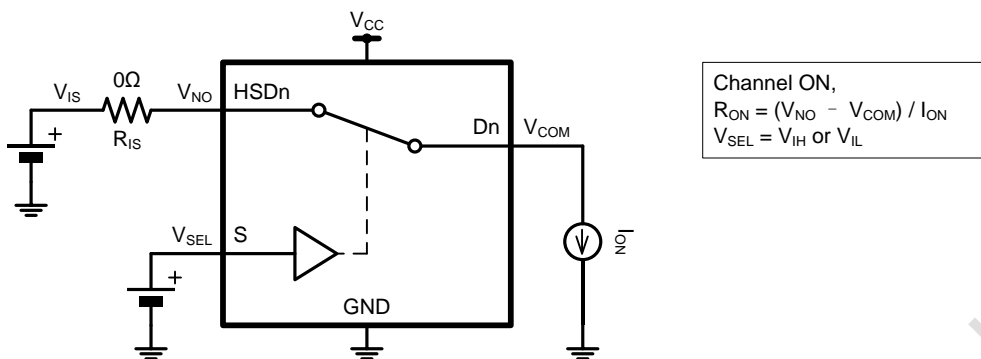


Figure 3, ON Resistance ( $R_{ON}$ )

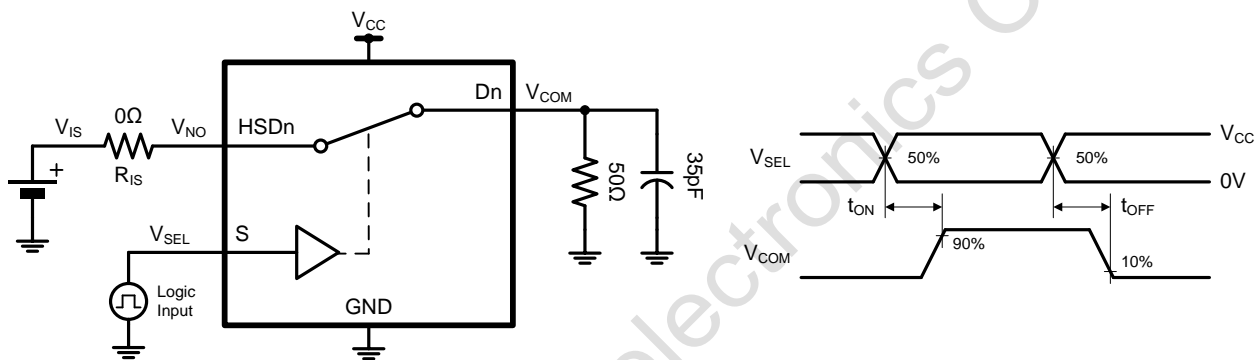


Figure 4, Turn-On and Turn-Off Time ( $t_{ON}/t_{OFF}$ )

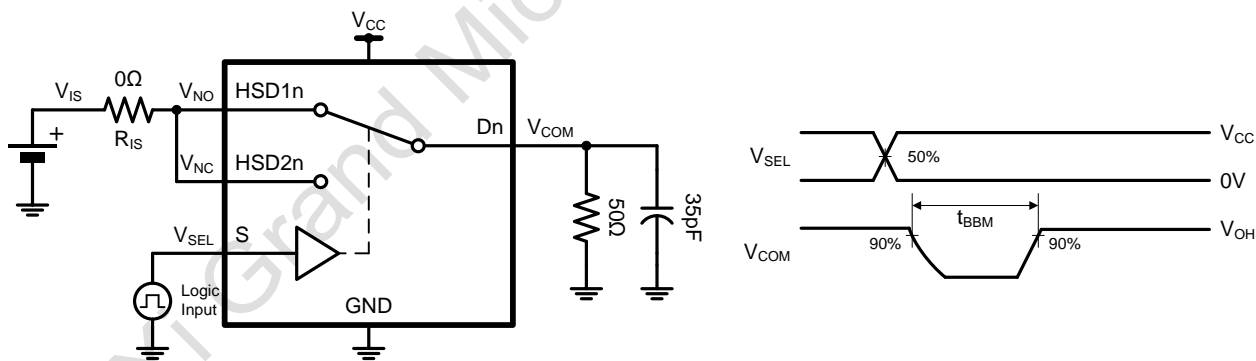
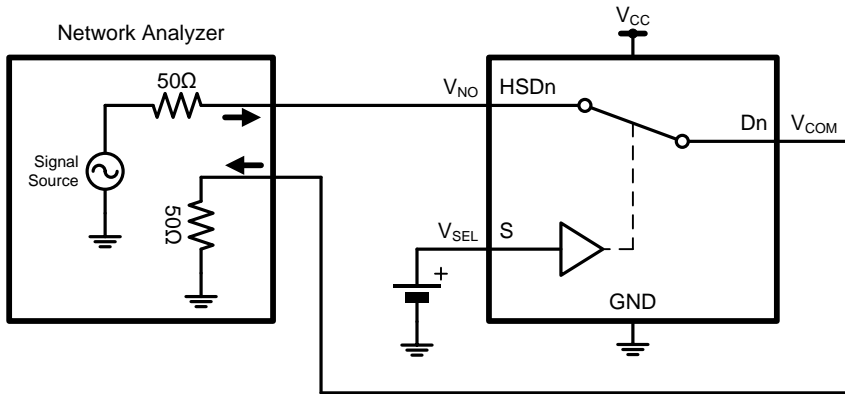


Figure 5, Break-Before-Make Time ( $t_{BBM}$ )

## TEST CIRCUITS (CONTINUED)

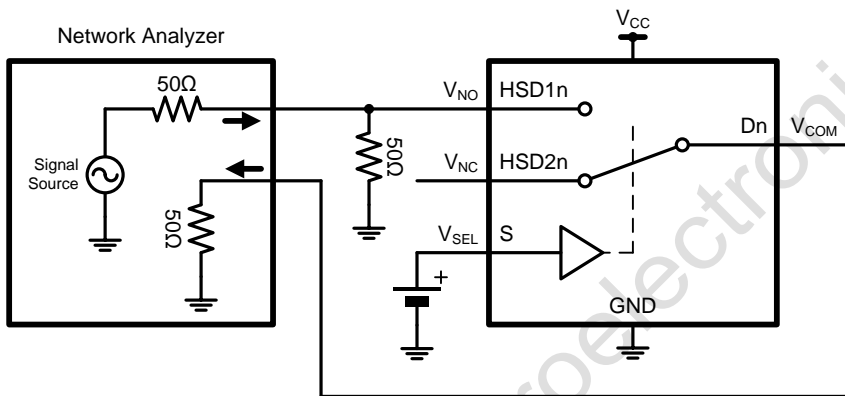


Channel ON: HSDn to Dn  
 $V_{SEL} = V_{IH}$  or  $V_{IL}$

### Network Analyzer Setup

Source Power = 0dBm  
(632mV P-P at 50Ω load)  
DC Bias = 350mV

Figure 6, ON Channel -3dB Bandwidth (BW)

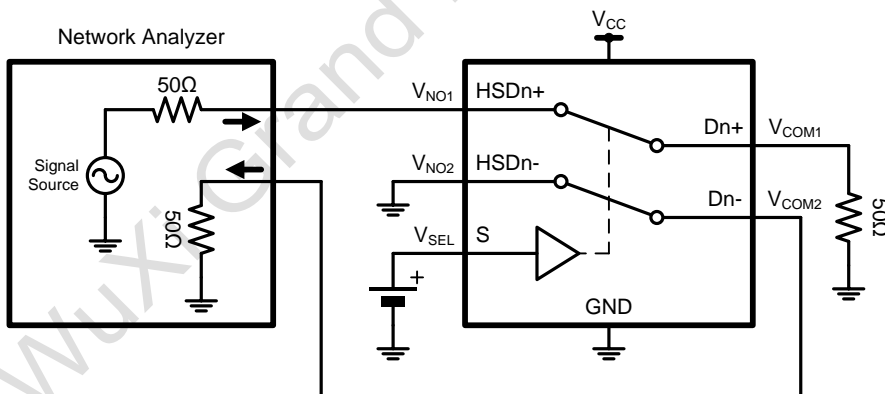


Channel OFF: HSD1n to Dn  
 $V_{SEL} = V_{IH}$  or  $V_{IL}$

### Network Analyzer Setup

Source Power = 0dBm  
(632mV P-P at 50Ω load)  
DC Bias = 350mV

Figure 7, OFF Isolation ( $O_{iso}$ )



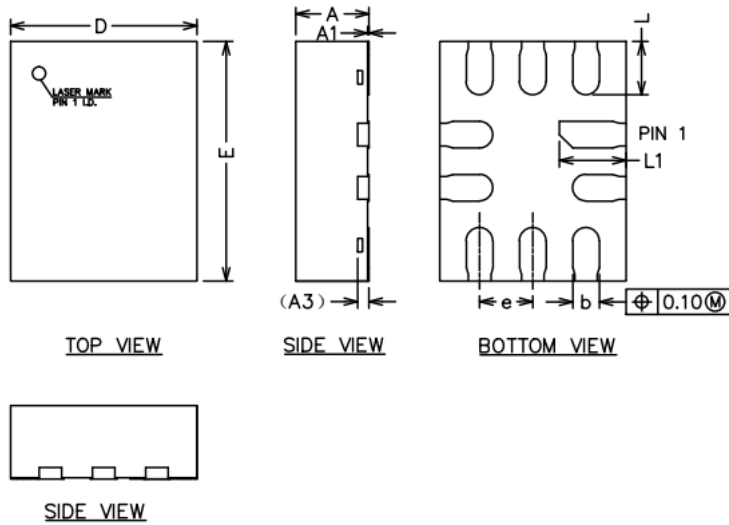
Channel ON: HSDn+ to Dn+  
Channel ON: HSDn- to Dn-  
 $V_{SEL} = V_{IH}$  or  $V_{IL}$

### Network Analyzer Setup

Source Power = 0dBm  
(632mV P-P at 50Ω load)  
DC Bias = 350mV

Figure 8, Channel-to-Channel Crosstalk ( $X_{TALK}$ )

## PACKAGE OUTLINE (UTQFN10-1.8x1.4)

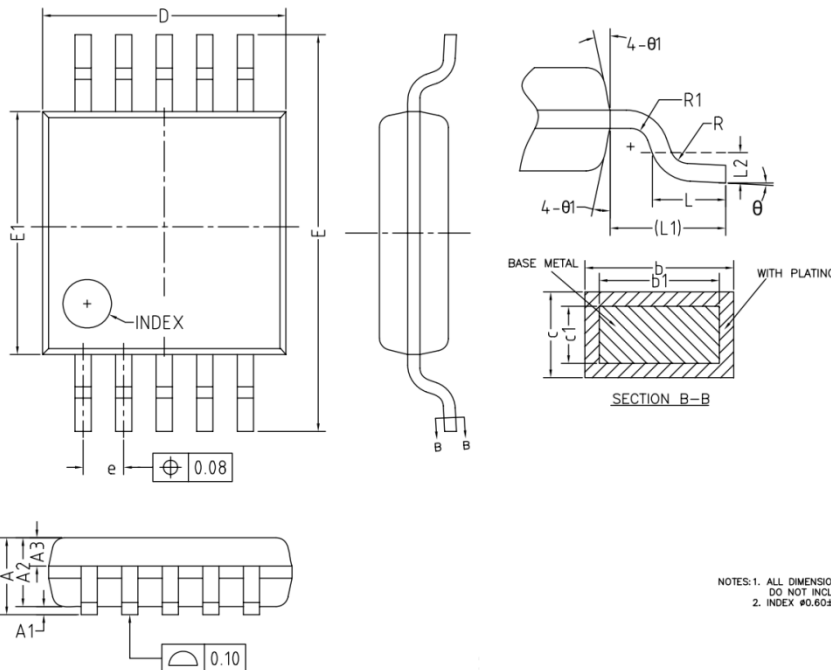


(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.152REF		
b	0.15	0.20	0.25
D	1.30	1.40	1.50
E	1.70	1.80	1.90
e	0.30	0.40	0.50
L	0.35	0.40	0.45
L1	0.45	0.50	0.55

## PACKAGE OUTLINE (MSOP10)

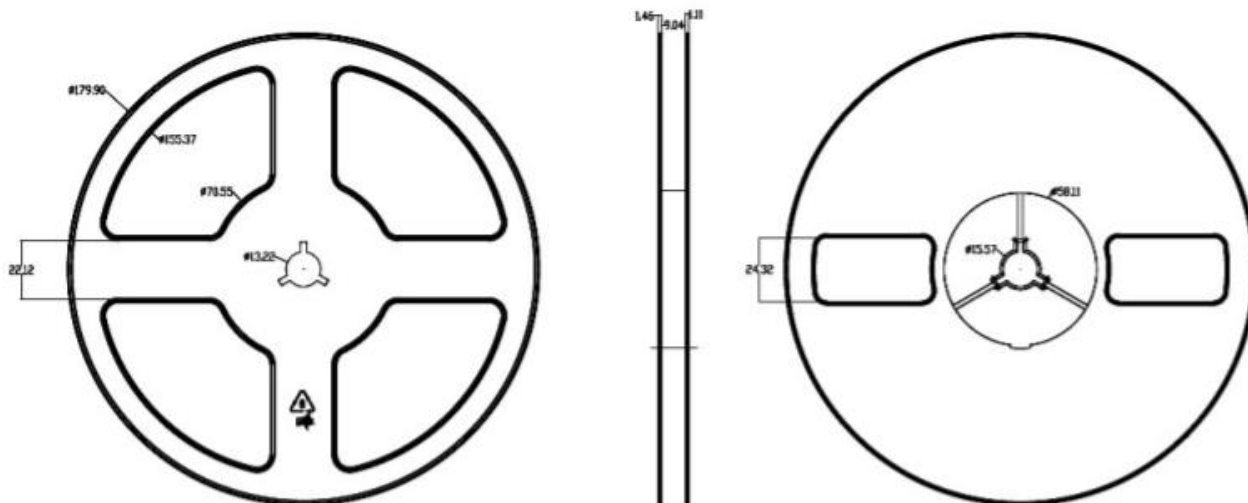
10-Pin MSOP Package Outline Diagram



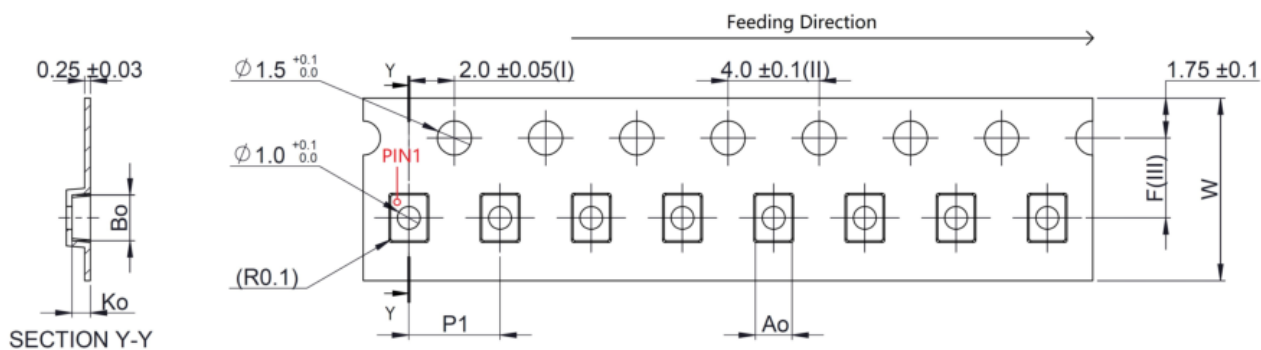


## TAPE AND REEL INFORMATION (UTQFN10-1.8x1.4)

### REEL



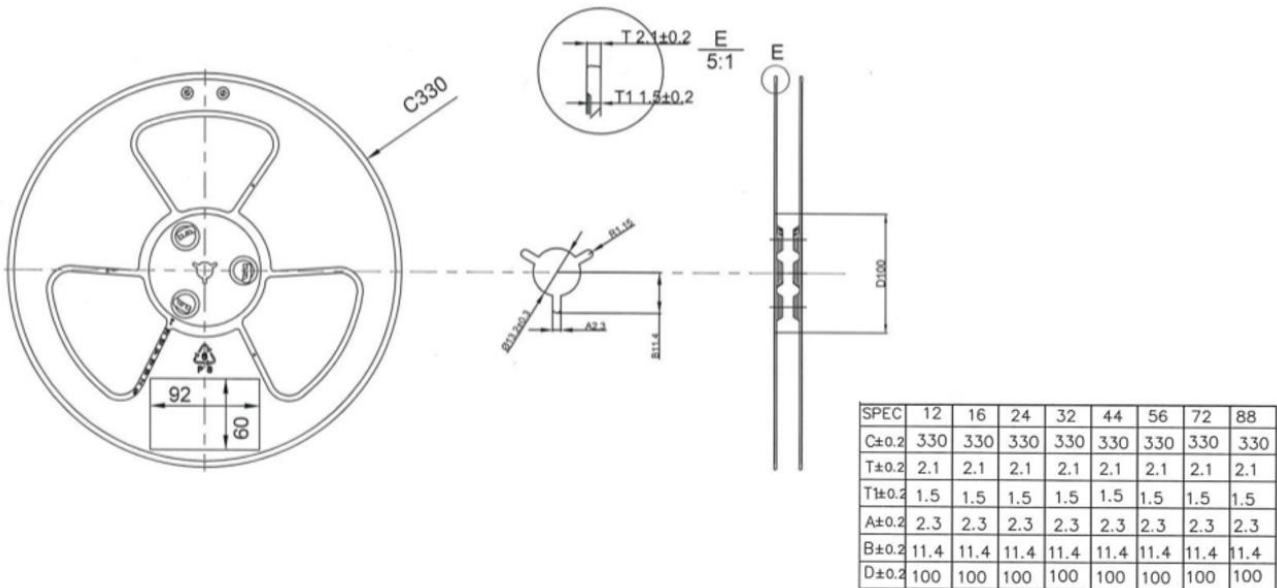
### TAPE



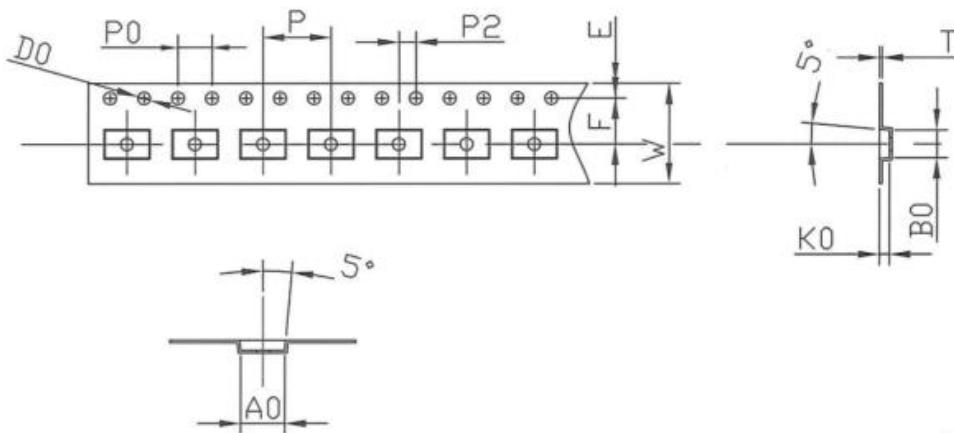
Ao	1.60	+/- 0.05
Bo	2.00	+/- 0.05
Ko	0.80	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.1
W	8.00	+0.3/-0.1

## TAPE AND REEL INFORMATION (MSOP10)

### REEL



### TAPE



ITEM	W	A0	A1	B0	B1	K0	K1	E	F	P	P0	P2	D0	D1	T
DIM	12.0	5.20	0.00	3.30	0.00	1.20	0.00	1.75	5.50	8.0	4.0	2.0	1.50	1.50	0.30
TOLE	+0.30 -0.30	±0.10	±0.00	±0.10	±0.00	±0.10	±0.00	±0.10	±0.05	±0.10	±0.10	±0.05	+0.10 -0.00	+0.10 -0.00	±0.05

## 产品订购信息

器件编号	产品丝印	工作温度范围	封装信息	包装方法
ASW7227QN	7228x(*)	-40°C 至 +85°C	UTQFN10-1.8x1.4x0.5	卷带和卷盘 (每卷 3000 只)
ASW7227MS	7228M xxxx(**)	-40°C 至 +85°C	MSOP10	卷带和卷盘 (每卷 4000 只)

注: (\*) x 表示生产信息, 可变。(\*\*)xxxx 表示生产信息, 可变。