

**Features**

- Provides bias for GaAs and HEMT FETs
- Drives up to three FETs
- Dynamic FET protection
- Drain current set by external resistor
- Regulated negative rail generator requires only 2 external capacitors
- Choice in drain voltage
- Wide supply voltage range
- Polarisation switch for LNBS - supporting zero volt gate switching topology.
- 22kHz tone detection for band switching
- Compliant with ASTRA control specifications
- SSOP surface mount package

**Applications**

- Satellite receiver LNBS
- Private mobile radio (PMR)
- Cellular telephones

**Description**

The AT1511 includes bias circuits to drive up to three external FETs. A control input to the device selects either one of two FETs as operational using 0V gate switching methodology, the third FET is permanently active. This feature is particularly used as an LNB polarisation switch. Also specific to LNB applications is the enhanced 22kHz tone detection and logic output feature which is used

to enable high and low band frequency switching. The detector has been specifically designed to reject interference such as low frequency signals and DiSEqC™ tone bursts - without the use of additional external components.

Drain current setting of the AT1511 is user selectable over the range 0 to 15mA, this is achieved with the addition of a single resistor. The series also offers the choice of FET drain voltage, the AT1511 gives 2 volts.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

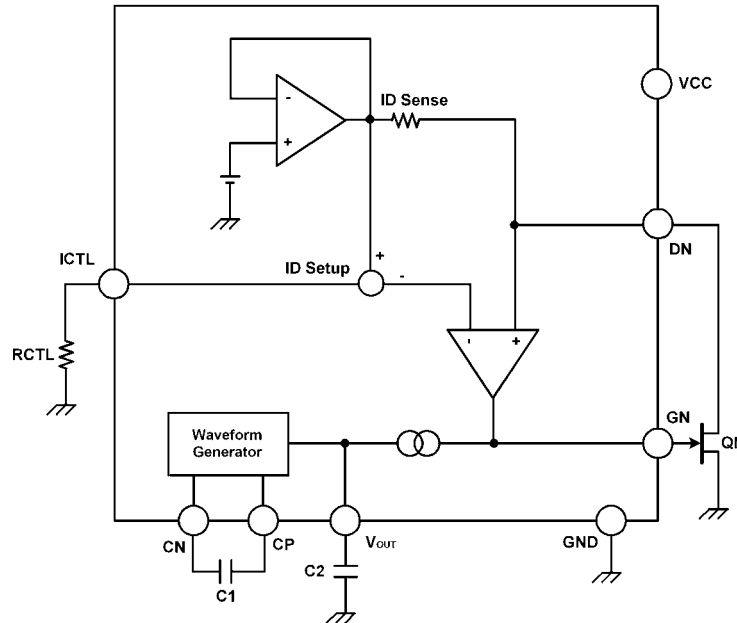
In order to protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.5V to 1V. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The AT1511 are available in SSOP20 for the minimum in device size. Device operating temperature is -40 to 70°C to suit a wide range of environmental conditions.

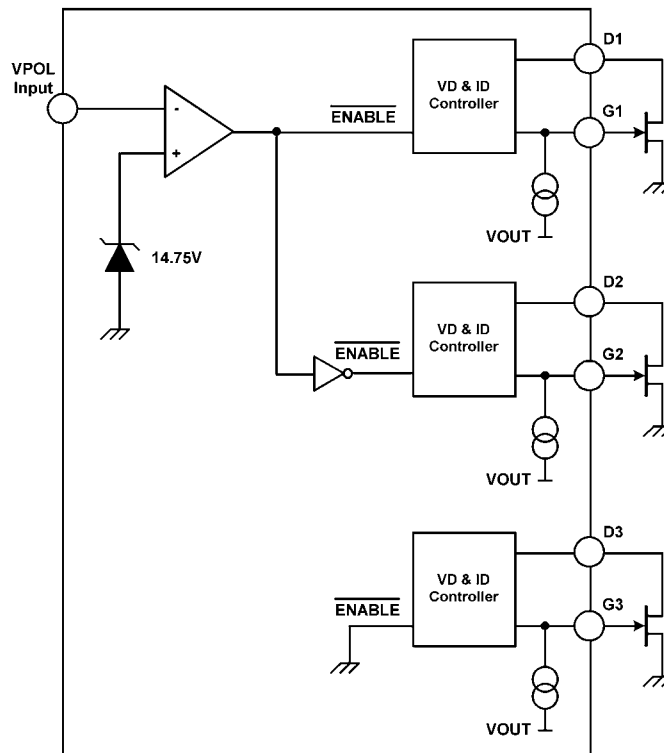
<b>Aimtron reserves the right without notice to change this circuitry and specifications.</b>
---

**Block Diagram**

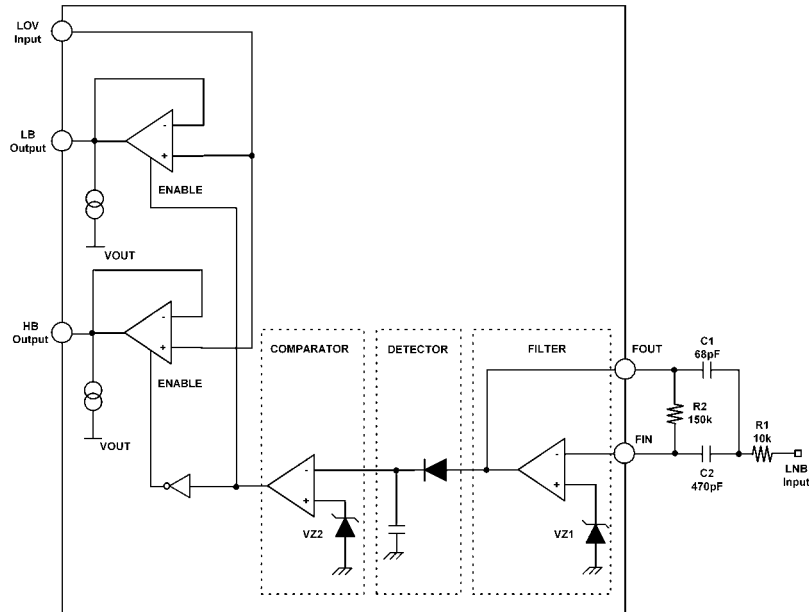
**(a) Drain Voltage & Current Controller**



**(b) Polarisation Switch**



**(c) Tone Detection**



**Pin Descriptions**

Pin No.	Pin name	Function
1	G1	1st Gate output voltage Pin
2	D1	1st Drain output voltage Pin
3	G2	2nd Gate output voltage Pin
4	D2	2nd Drain output voltage Pin
5	G3	3rd Gate output voltage Pin
6	D3	3rd Drain output voltage Pin
7	GND	Ground Pin
8	CP	Positive OSC output Pin
9	CN	Negative OSC output Pin
10	N.C.	No connect Pin
11	VOUT	Negative voltage output Pin
12	LB	Error Amplifier output Pin
13	HB	Error Amplifier inverted output Pin
14	LOV	Error Amplifier input Pin
15	FOUT	Filter input Pin
16	N.C.	No connect Pin
17	FIN	Filter output Pin
18	VPOL	Polarisation switch controller Pin
19	ICTL	Drain Current set Resistor connect Pin
20	VCC	Supply voltage Pin

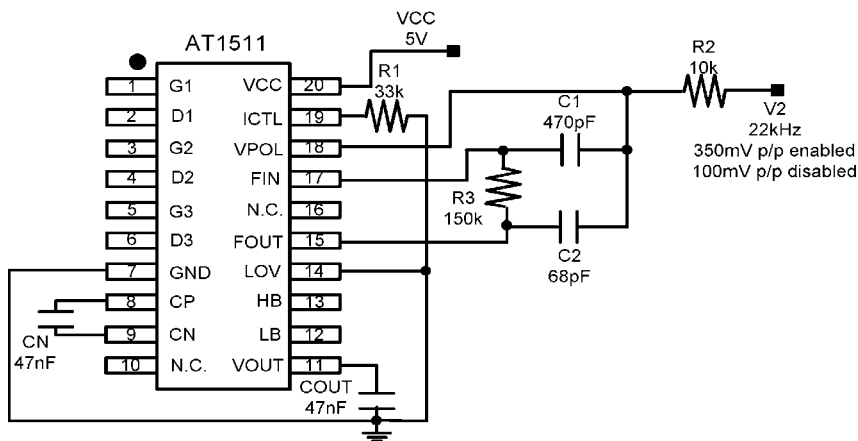
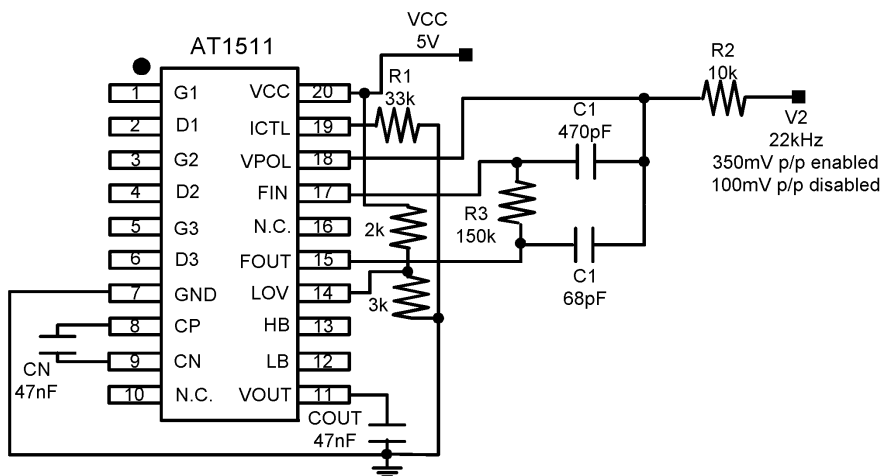


**Electrical characteristics**

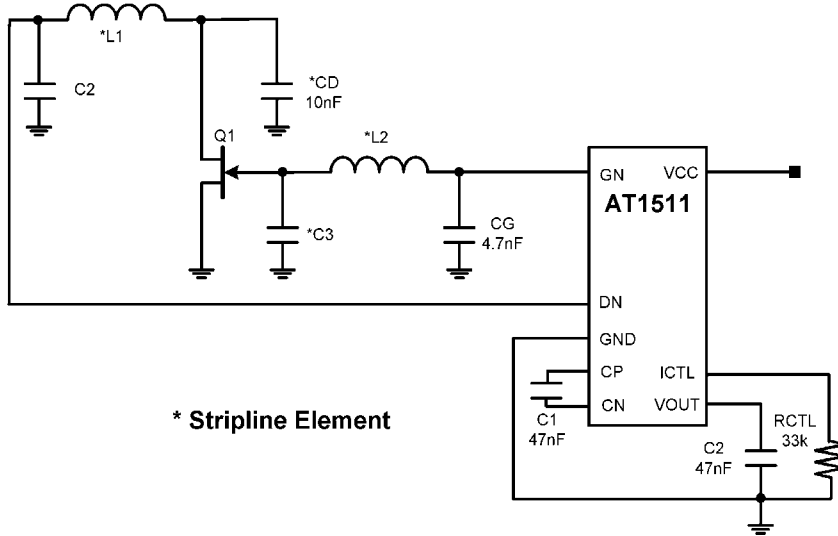
 (Unless otherwise stated,  $T_a=25^{\circ}\text{C}$ ,  $V_{CC}=5\text{V}$ ,  $I_D=10\text{mA}$ ,  $R_{CTL}=33\text{k}\Omega$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	$V_{CC}$	5	--	10	V	
Supply Current	$I_{CC}$	--	6	10	mA	$I_{D1}$ to $I_{D3}=0$
		--	25	35	mA	$I_{D1}=0, I_{D2}$ to $I_{D3}=10\text{mA}$ , $V_{POL}=14\text{V}$
		--	25	35	mA	$I_{D2}=0, I_{D1}$ to $I_{D3}=10\text{mA}$ , $V_{POL}=15.5\text{V}$
		--	16	25		$I_{D1}$ to $I_{D3}=0$ , $I_{LB}=10\text{mA}$
		--	16	25	mA	$I_{D1}$ to $I_{D3}=0$ , $I_{HB}=10\text{mA}$
Negative Voltage	$V_{OUT}$	-3.5	-3.0	-2.5	V	$I_{OUT}=0$
		--	--	-2.4	V	$I_{OUT}=-200\mu\text{A}$
Drain Output Noise Voltage	$E_{ND}$	--	--	0.02	$V_{PP}$	$C_G=4.7\text{nF}$ , $C_D=10\text{nF}$
Gate Output Noise Voltage	$E_{NG}$	--	--	0.005	$V_{PP}$	$C_G=4.7\text{nF}$ , $C_D=10\text{nF}$
Oscillator Freq.	$f_o$	200	350	800	kHz	
<b>DRAIN</b>						
Drain Current	$I_D$	8	10	12	mA	
Drain Current Charge with $V_{CC}$	$\Delta I_{DV}$	--	0.5	--	%/V	$V_{CC}=5$ to $10\text{V}$
Drain Current Charge with $T_i$	$\Delta I_{DT}$	--	0.05	--	%/ $^{\circ}\text{C}$	$T_i=-40$ to $+70^{\circ}\text{C}$
Drain Voltage	$V_{D1}$	1.8	2.0	2.2	V	$I_{D1}=10\text{mA}$ , $V_{POL}=15.5\text{V}$
	$V_{D2}$	1.8	2.0	2.2	V	$I_{D2}=10\text{mA}$ , $V_{POL}=14\text{V}$
	$V_{D3}$	1.8	2.0	2.2	V	$I_{D3}=10\text{mA}$
Drain Voltage Charge with $V_{CC}$	$\Delta V_{DV}$	--	0.5	--	%/V	$V_{CC}=5$ to $12\text{V}$
Drain Voltage Charge with $T_i$	$\Delta V_{DT}$	--	50	--	ppm	$T_i=-40$ to $+70^{\circ}\text{C}$
Leakage Current	$I_{L1}$	--	--	10	$\mu\text{A}$	$V_{D1}=0.5\text{V}$ , $V_{POL}=14\text{V}$
	$I_{L2}$	--	--	10	$\mu\text{A}$	$V_{D2}=0.5\text{V}$ , $V_{POL}=15.5\text{V}$
<b>GATE</b>						
Gate Output Current Range	$I_{GO}$	-30	--	2000	$\mu\text{A}$	
Gate1 Output Voltage	$V_{G10}$	-0.05	0	0.05	V	$I_{D1}=0$ , $V_{POL}=14\text{V}$ , $I_{GO1}=0$
	$V_{G1L}$	-3.5	-2.9	-2.0	V	$I_{D1}=12\text{mA}$ , $V_{POL}=15.5\text{V}$ , $I_{GO1}=-10\mu\text{A}$
	$V_{G1H}$	0.4	0.75	1.0	V	$I_{D1}=8\text{mA}$ , $V_{POL}=15.5\text{V}$ , $I_{GO1}=0$
Gate2 Output Voltage	$V_{G20}$	-0.05	0	0.05	V	$I_{D2}=0$ , $V_{POL}=15.5\text{V}$ , $I_{GO2}=0$
	$V_{G2L}$	-3.5	-2.9	-2.0	V	$I_{D2}=12\text{mA}$ , $V_{POL}=14\text{V}$ , $I_{GO2}=-10\mu\text{A}$
	$V_{G2H}$	0.4	0.75	1.0	V	$I_{D2}=8\text{mA}$ , $V_{POL}=14\text{V}$ , $I_{GO2}=0$
Gate3 Output Voltage	$V_{G3L}$	-3.5	-2.9	-2.0	V	$I_{D3}=12\text{mA}$ , $I_{GO3}=-10\mu\text{A}$
	$V_{G3H}$	0.4	0.75	1.0	V	$I_{D3}=8\text{mA}$ , $I_{GO3}=0$
<b>TONE DETECTION</b>						
Input Bias Current	$I_B$	0.02	0.07	0.25	$\mu\text{A}$	$R_{F1}=150\text{k}\Omega$
Output Voltage	$V_{OUT}$	1.75	1.95	2.05	V	$R_{F1}=150\text{k}\Omega$
Output Current	$I_{OUT}$	400	520	650	$\mu\text{A}$	$V_{OUT}=1.96\text{V}$ , $V_{FIN}=2.1\text{V}$
Voltage Gain	$G_V$	--	46	--	dB	$f=22\text{kHz}$ , $V_{IN}=1\text{mV}$
Rejection Frequency	$f_R$	1.0	7.5	--	kHz	$V_{(AC)in}=1\text{V p/p sq.w}$
LOV Volt. Range	$V_{LOV}$	-0.5	--	$V_{CC}-1.8$	V	$I_L=50\text{mA}$ (LB or HB)
LOV Bias Current	$I_{LOV}$	0.02	0.15	1.0	$\mu\text{A}$	$V_{LOV}=0$
LB Output Low	$V_{LBL}$	-3.5	-2.75	-2.5	V	$V_{LOV}=0$ , $I_L=-10\mu\text{A}$ , Enabled
		-0.01	0	0.01	V	$V_{LOV}=3\text{V}$ , $I_L=0$ , Enabled

LB Output High	$V_{LBH}$	-0.025	0	0.025	V	$V_{LOV}=0, I_L=10mA, Disabled$
		2.9	3.0	3.1	V	$V_{LOV}=3V, I_L=50mA, Disabled$
HB Output Low	$V_{HBL}$	-3.5	-2.75	-2.5	V	$V_{LOV}=0, I_L=-10\mu A, Disabled$
		-0.01	0	0.01	V	$V_{LOV}=3V, I_L=0, Disabled$
HB Output High	$V_{HBH}$	-0.025	0	0.025	V	$V_{LOV}=0, I_L=10mA, Enabled$
		2.9	3.0	3.1	V	$V_{LOV}=3V, I_L=50mA, Enabled$
<b>POLARITY SWITCH</b>						
Input Current	$I_{POL}$	10	20	40	$\mu A$	$V_{POL}=25V$ (Applied via $R_{POL}=10k\Omega$ )
Threshold Voltage	$V_{TPOL}$	14	14.75	15.5	V	$V_{POL}=25V$ (Applied via $R_{POL}=10k\Omega$ )
Switching Speed	$T_{SPOL}$	--	--	100	ms	$V_{POL}=25V$ (Applied via $R_{POL}=10k\Omega$ )

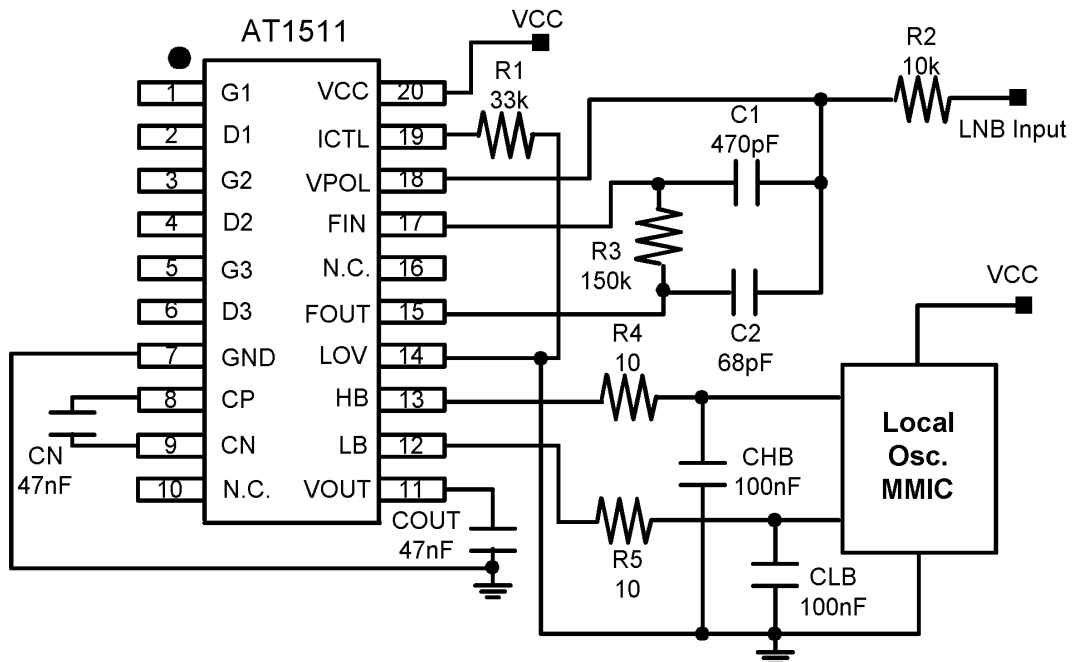
**Test Circuit**
**(a)  $L_{OV}$  Connected to ground**

**(b)  $L_{OV}$  Connected to  $V_{osc}$** 


**Application Circuit**

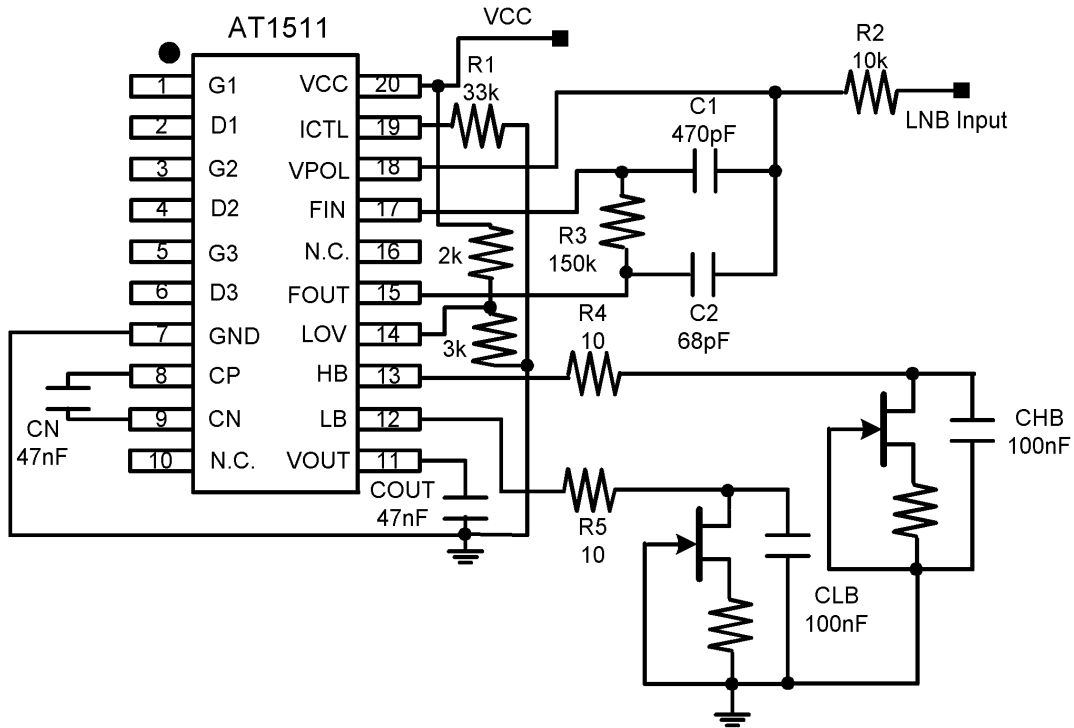


**Application Information**

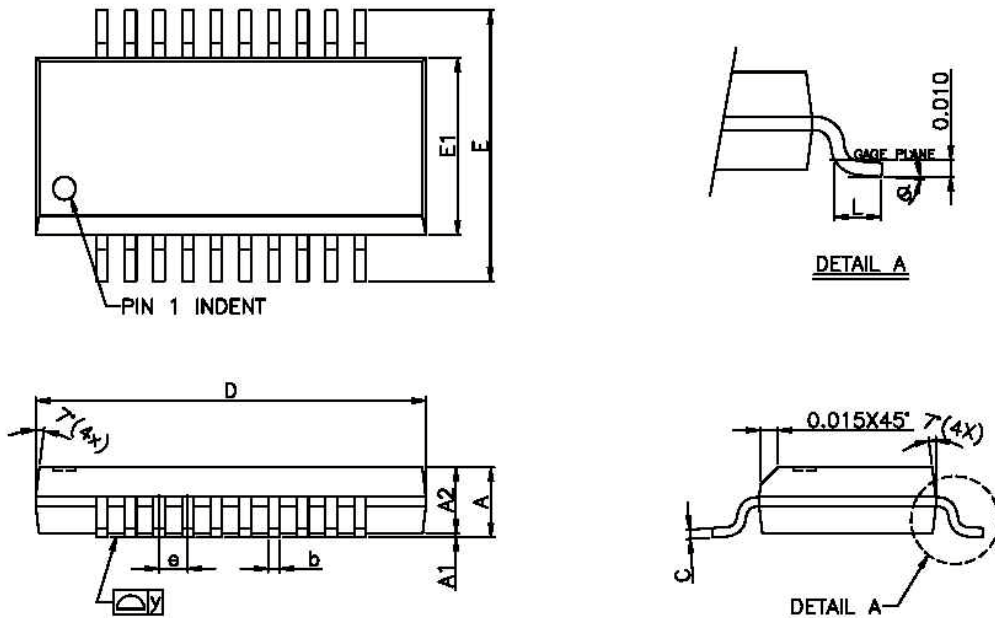
**(a)  $L_{OV}$  Connected to ground**



(b)  $L_{OV}$  Connected to  $V_{OSC}$





**Package Outlines : 20-pin SSOP**


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	1.37	1.45	1.52	0.054	0.057	0.060
b	0.23	0.25	0.36	0.009	0.010	0.014
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	8.53	8.64	8.74	0.336	0.340	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.38	0.71	1.27	0.015	0.028	0.050
e	-	0.64	-	-	0.025	-
y	-	-	0.076	-	-	0.003
$\theta$	0°		8°	0°		8°