1MHz, All-Ceramic, 3.2A PWM Buck DC/DC Converter

Features

- **Ceramic Input and Output Capacitors**
- **Efficiency Up to 94%**
- **Operate from 2.5V to 6V supply**
- **Adjustable Output from 0.8V to V_{IN}**
- **Internal Soft-Start**
- **Short-Circuit and Thermal-Overload Protection**
- **Input Over Voltage Protection**
- **RoHS Compliant**

Applications

- **ASIC/DSP/µP/FPGA Core and I/O Voltages**
- **Set-Top Boxes**
- **Cellular Base Stations**
- **Networking and Telecommunications**

General Description

The AT1529 high-efficiency, DC/DC buck converter delivers up to 3.2A of output current. The device operates from an input voltage of 2.5V to 6V and provides an output voltage from 0.8V to V_{IN}, making the AT1529 ideal for on-board post-regulation applications.

The AT1529 operate at a fixed frequency of 1MHz with an efficiency of up to 94%. The high operating frequency minimizes the size of external components. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protections improve design reliability.

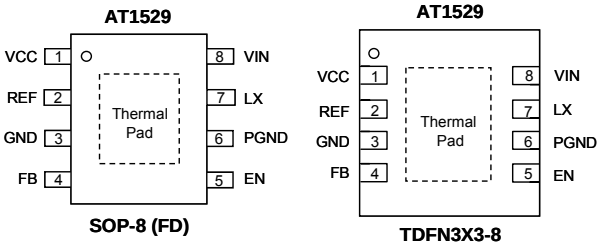
The AT1529 are available in a space-saving SOP-8 and TDFN3X3-8 package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
AT1529F11U	A1529	-40°C to +85°C	SOP-8 (FD)
AT1529RD1U	A1529	-40°C to +85°C	TDFN3X3-8

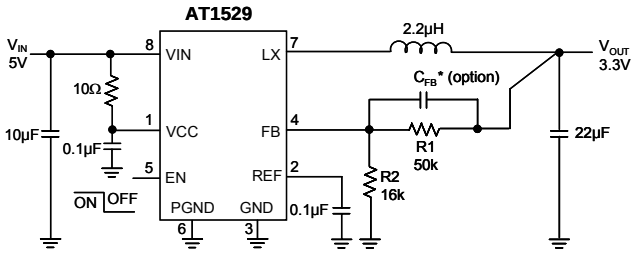
Note: F1:SOP-8 (FD) RD: TDFN3X3-8
1: Bonding Code
U: Tape & Reel

Pin Configuration



Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application Circuit



$V_{OUT} = 0.8V \times (1 + \frac{R1}{R2})$

Absolute Maximum Ratings

VIN, VCC, REF to GND . . . . . -0.3V to +7V
LX to PGND . . . . . -1V to (VIN+1V)
EN, FB to GND. . . . . -0.3V to (VCC + 0.3V)
VIN to VCC . . . . . -0.3V to +0.3V
PGND to GND . . . . . -0.3V to +0.3V
Thermal Resistance Junction to Ambient, (θ_{JA}) *
SOP-8 (FD) . . . . . 108°C/W
TDFN3X3-8 . . . . . 98°C/W
Continuous Power Dissipation (T_A = +25°C) *
SOP-8 (FD). 1.2W
TDFN3X3-8 . . . . . 1.4W
Thermal Resistance Junction to Case, (θ_{JC})
SOP-8 (FD) . . . . . 12°C/W
TDFN3X3-8 . . . . . 30°C/W
Operating Temperature Range . . . . . -40°C to 85°C
Maximum Junction Temperature. . . . . 150°C
Storage Temperature Range. . . . . -65°C to 165°C
Reflow Temperature (soldeing,10 sec) . . . . . 260°C

* Please refer to 1in^2 of 1oz PCB Layout Section.
Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Electrical Characteristics

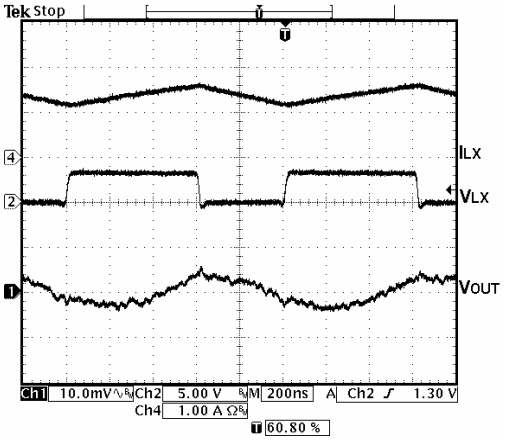
(V_{IN}= V_{CC}= 3.3V, PGND = GND, FB in regulation, C_{REF}= 10nF, T_A= -40°C to +85°C, unless otherwise noted. Typical values are at T_A= +25°C.)

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
IN Voltage Range			2.5	---	6	V
Supply Current	No switching (EN=V_{CC})	V_{IN} = 5V	---	450	---	µA
	Shutdown (EN=0V)		---	20	---	µA
V_{CC} Undervoltage Lockout Threshold	When LX starts/stops switching		---	2.3	---	V
REF Voltage	I_{REF} = 0, V_{IN} = 2.5V to 5V		---	0.8	---	V
EN Enable Threshold	Logic High		2	---	---	V
	Logic Low		---	---	0.4	V
Output Voltage Range	When using external feedback resistors to drive FB		0.8	---	V_{IN}	V
Output Voltage Line Regulation	V_{IN} = 3V to 5V		---	0.08	---	%/V
Output Voltage Load Regulation	0A<I_{LOAD}<3A		---	0.12	---	%/A
FB Regulation Voltage (Error Amp Only)		V_{IN} = 2.5V to 5V	0.784	0.8	0.816	V
FB Input Bias Current			-0.1	---	0.1	µA
LX On-Resistance, PMOS	V_{IN} = 5V		---	116	---	mΩ
LX On-Resistance, NMOS	V_{IN} = 5V		---	93	---	mΩ
LX Current-Limit Threshold	Duty cycle = 100%, V_{IN} = 2.5V to 5V	High side	4.1	4.8	---	A
		Low side	---	0	---	
LX Leakage Current	V_{IN} = 5V	V_{LX} = 5V	---	---	10	µA
		LX = GND	-10	---	---	
LX Switching Frequency	V_{IN} = 2.5V to 5V		---	1	---	MHz
LX Maximum Duty Cycle	V_{COMP} = 1.5V, LX = high-Z, V_{IN} = 2.5V to 5V		100	---	---	%
LX Minimum Duty Cycle	V_{COMP} = 1V, V_{IN} = 2.5V to 5V		---	15	---	%
Thermal-Shutdown Threshold	When LX starts/stops switching	T_J rising	---	160	---	°C
		T_J falling	---	145	---	
Maximum Duty Cycle			100	---	---	%
Minimum On Time			---	---	0	ns

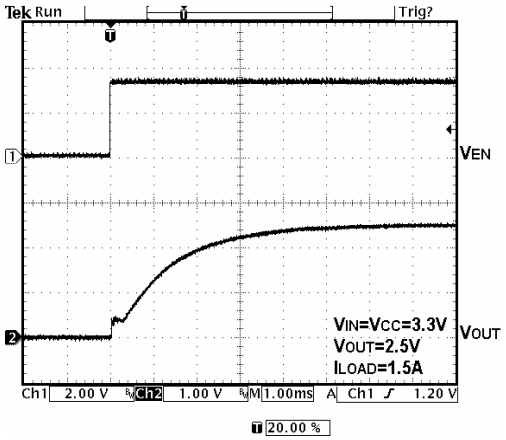
Typical Performance Characteristics

C_{VIN}=10µF, C_{VOUT}=10µF, L=2.2µH, T_A=25°C, unless otherwise noted.

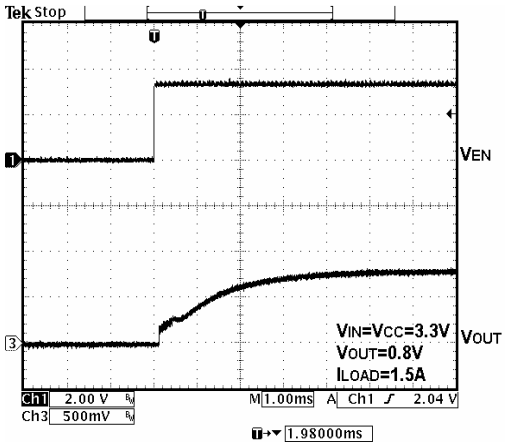
Switching Waveform



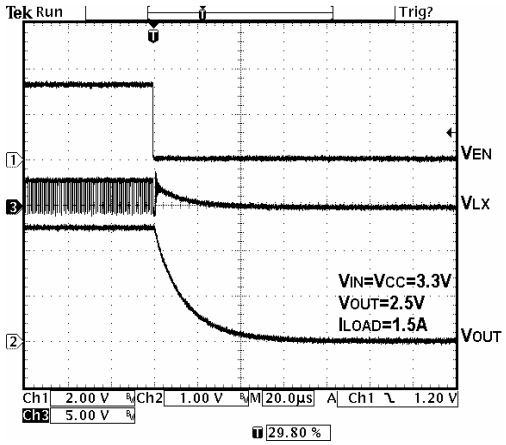
Soft Start Waveform



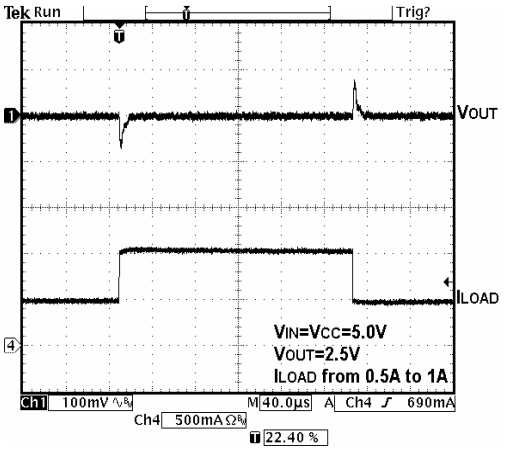
Soft Start Waveform



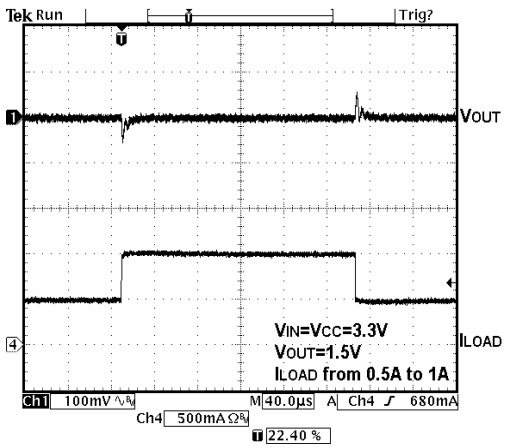
Shutdown Waveform



Load Transient Response

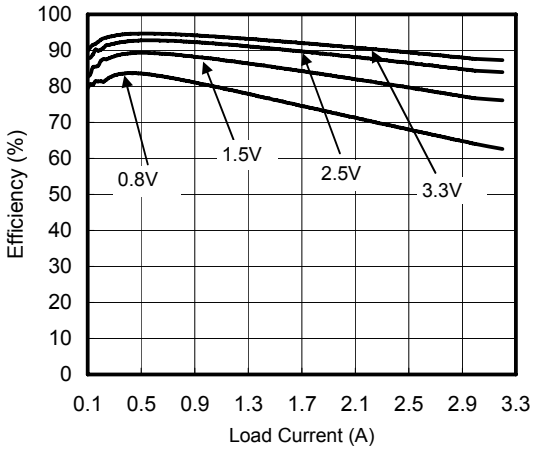


Load Transient Response

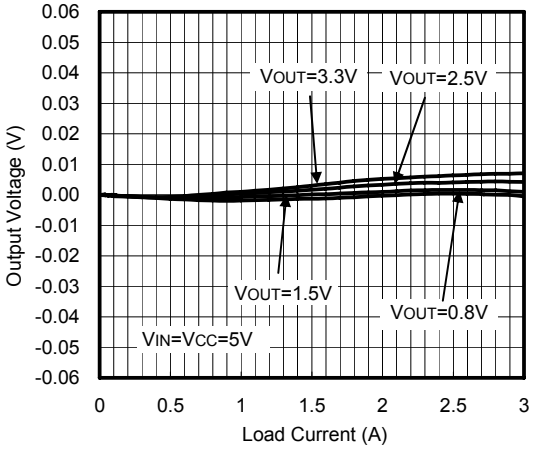


Typical Performance Characteristics (continued)

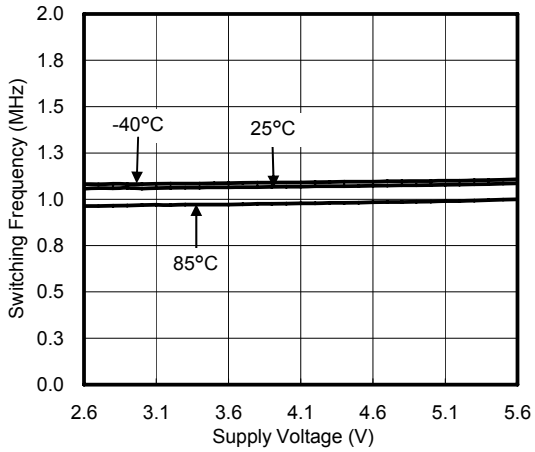
Efficiency vs Load Current
(VCC = VIN = 5V)



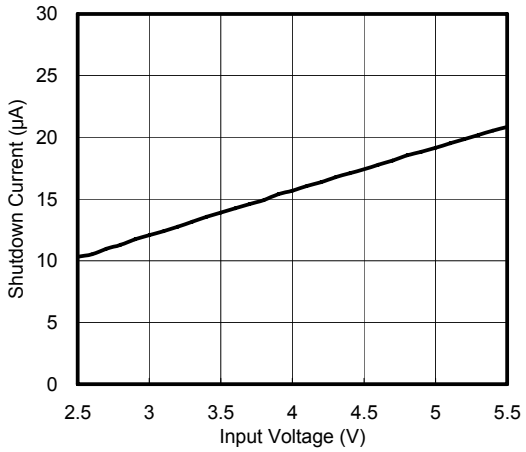
Output Voltage Deviation vs Load Current
(VCC=VIN=5V)



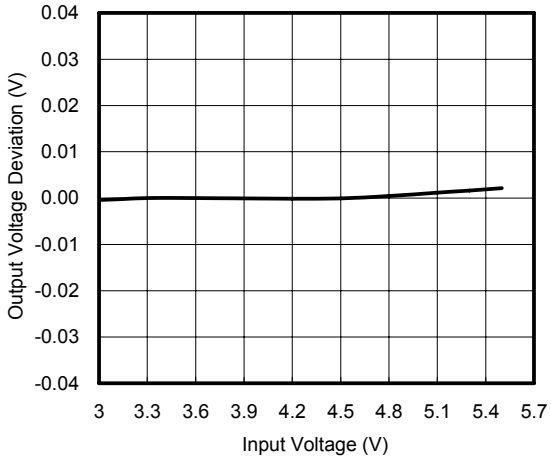
Switching Frequency vs Input Voltage



Shutdown Current vs Input Voltage

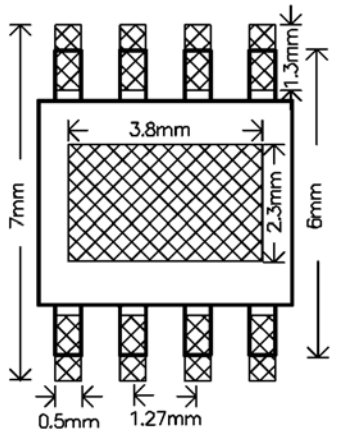


Output Voltage Deviation vs Input Voltage

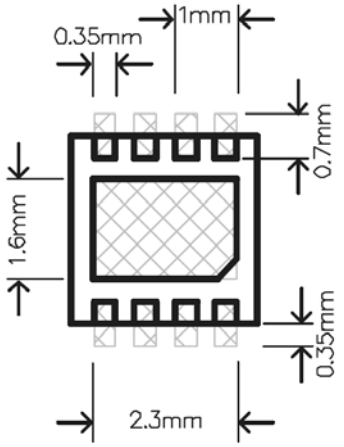


Minimum Footprint PCB Layout Section

SOP-8 (FD)

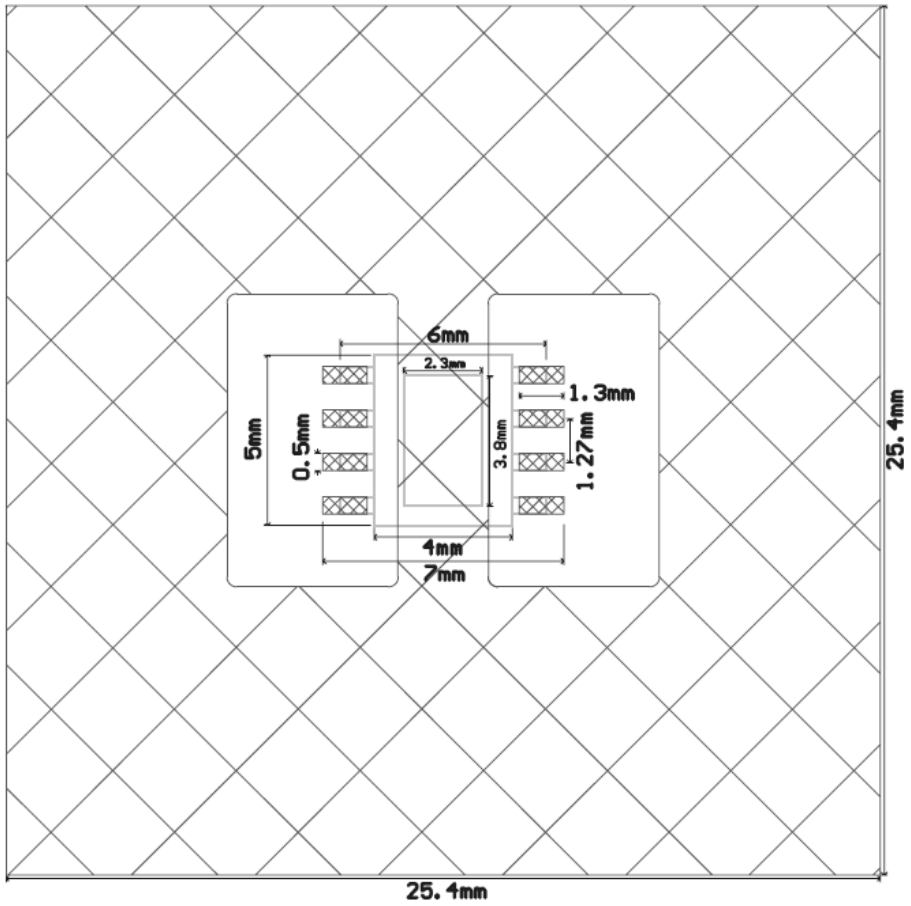


TDFN3X3-8

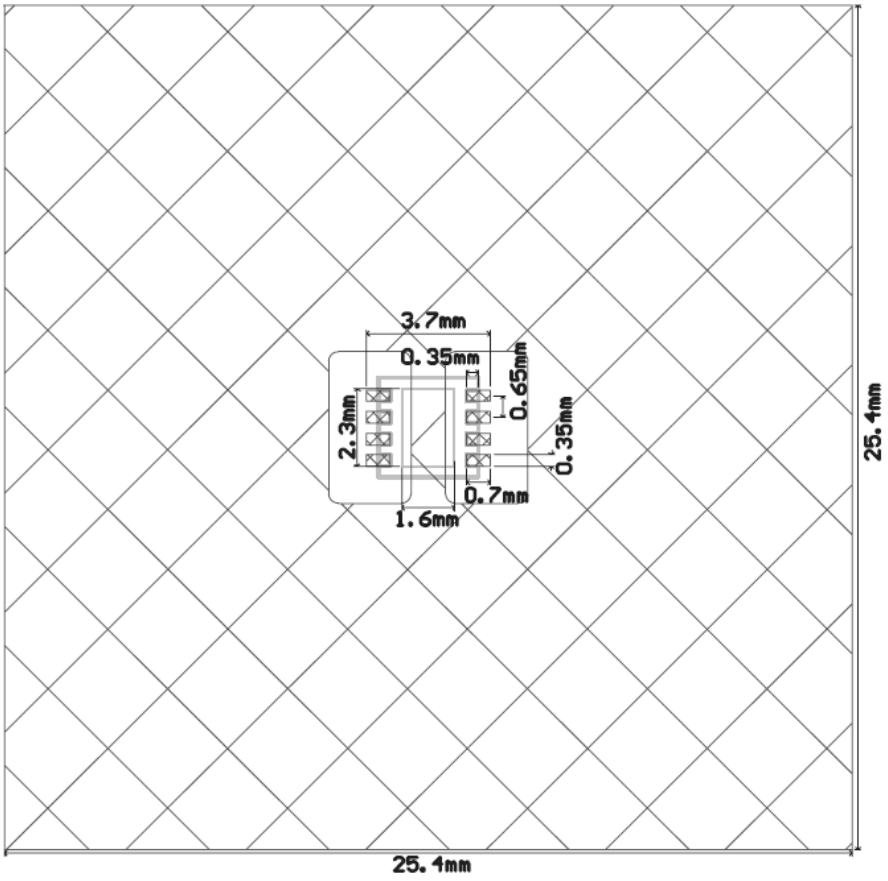


1in^2 of 1oz PCB Layout Section

SOP-8 (FD)



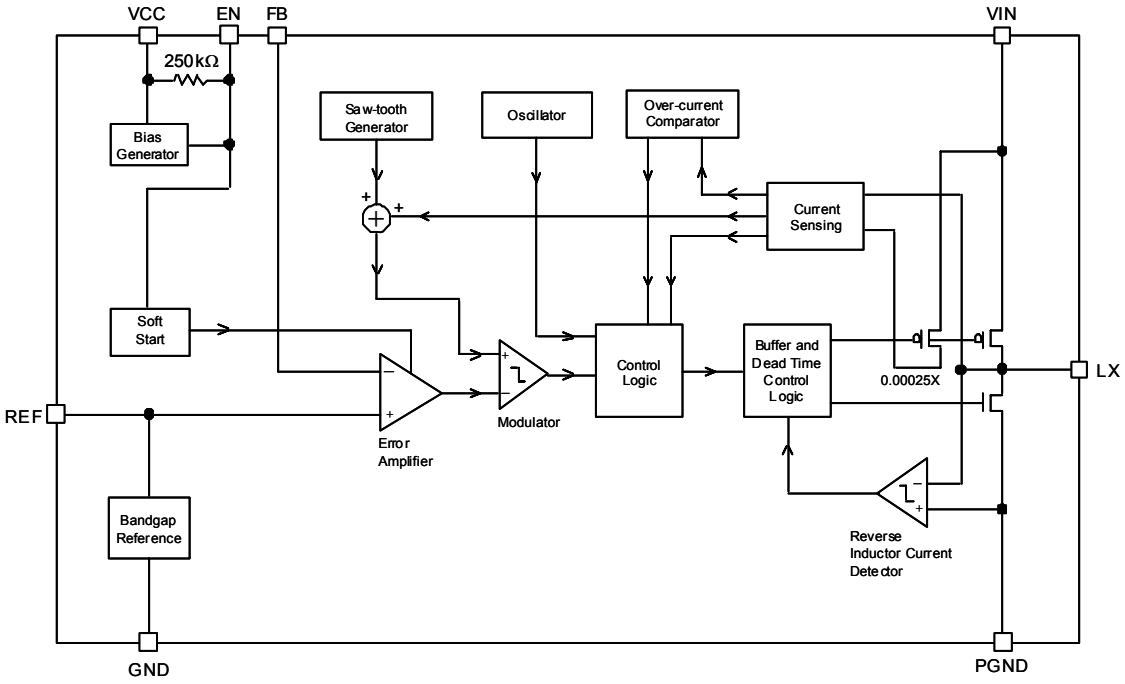
TDFN3X3-8



Pin Descriptions

PIN	NAME	FUNCTION
1	VCC	Supply Voltage. Bypass with 0.1μF capacitor to ground and 10Ω resistor to V_{IN}. The voltage of VCC must be (VIN-0.3V < VCC < VIN+0.3V).
2	REF	Reference Bypass. Bypass with 0.1μF capacitor to ground.
3	GND	Ground
4	FB	Feedback Input. Connect an external resistor-divider from the output to FB and GND to set the output to a voltage between 0.8V and V_{IN}.
5	EN	Enable. Internal pull high with a resistor. Pull EN below 0.4V to shut down the regulator.
6	PGND	Power Ground. Internally connected to GND. Keep power ground and signal ground planes separate.
7	LX	Inductor Connection. Connect an inductor between LX and the regulator output.
8	VIN	Power-Supply Voltage. Input voltage range from 2.5V to 6V. Bypass with a 10μF (min.) ceramic capacitor to ground and a 10Ω resistor to V_{CC}.
Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram



Function Description

The AT1529 high-efficiency switching regulator is a small, simple, DC-to-DC step-down converters capable of delivering up to 3.2A of output current. The devices operate in pulse-width modulation (PWM) at a fixed frequency of 1MHz from a 2.5V to 6V input voltage and provide an output voltage from 0.8V to V_{IN}, making the AT1529 ideal for on-board post-regulation applications. The high switching frequency allows for the use of smaller external components, and internal synchronous rectifiers improve efficiency and eliminate the typical Schottky free-wheeling diode. Using the on-resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Controller Block Function

The AT1529 step-down converters use a PWM current-mode control scheme. An open-loop comparator (Modulator) compares the amplified voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (<30% ripple current), The circuit acts as a switch-mode transconductance amplifier. To preserve inner-loop stability and eliminate inductor stair-casing, a slope-compensation ramp is summed into the main PWM comparator. During the second half of the cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current, and discharges when the inductor current is lower, smoothing the voltage across the load.

Current Limit

The internal high-side MOSFET has a current limit of 4.8A (typ.). If the current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. A synchronous rectifier current limit of 0A (typ.) protects the device from current flowing into LX. If the negative current limit is exceeded, the synchronous rectifier turns off, forcing the inductor current to flow through the high-side MOSFET body diode, back to the input, until the beginning of the next cycle or until the inductor current drops to zero. The AT1529 utilize a pulse-skip mode to prevent overheating during short-circuit output conditions. The device enters pulse-skip mode when the FB voltage drops below 300mV, limiting the current to 4.8A (typ.) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

VCC Decoupling

Due to the high switching frequency and tight output tolerance, decouple VCC with a 0.1µF capacitor connected from VCC to GND, and a 10Ω resistor connected from VCC to VIN. Place the capacitor as close to VCC as possible.

Soft-Start

The AT1529 employ soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO) or shut-down mode, the soft-start circuitry will slowly ramp up the output voltage.

Undervoltage Lockout

If VCC drops below 2.3V (typ.), the UVLO circuit inhibits switching. Once VCC rises above 2.3V (typ.), the UVLO clears, and the soft-start sequence activates.

Input Over Voltage Protection

If VCC rises above 6.3V (typ.), the Input OVP circuit inhibits switching. Once VCC falls below 6V (typ.), the OVP clears, and the soft-start sequence activates.

Shutdown Mode

The EN pin has a internal pull high resistor connect to VCC. To shut down the AT1529, use an NPN bipolar junction transistor or a MOSFET to pull EN to GND. Shutdown mode causes the internal MOSFETs to stop switching, forces LX to a high-impedance state, and shorts REF to GND. Release EN to exit shutdown and initiate the soft-start sequence.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Application Information

Inductor Selection

Use a 2μH inductor with a minimum 3.2A-rated DC current for most applications. For best efficiency, use an inductor with a DC resistance of less than 20mΩ and a saturation current greater than 5A (min). For most designs, derive a reasonable inductor value (L_{INIT}) from the following equation:

$$L_{INIT} = V_{OUT} \times (V_{IN} - V_{OUT}) / (V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{SW})$$

where f_{SW} is the switching frequency (1MHz typ) of the oscillator. Keep the inductor current ripple percentage LIR between 20% and 40% of the maximum load current for the best compromise of cost, size, and performance. Calculate the maximum inductor current as:

$$I_{L(MAX)} = (1 + LIR / 2) \times I_{OUT(MAX)}$$

Check the final values of the inductor with the output ripple voltage requirement. The output ripple voltage is given by:

$$V_{RIPPLE} = V_{OUT} \times (V_{IN} - V_{OUT}) \times ESR / (V_{IN} \times L_{FINAL} \times f_{SW})$$

where ESR is the equivalent series resistance of the output capacitors.

Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS}=(1/V_{IN}) \times (I_{OUT}^2 \times V_{OUT} \times (V_{IN}-V_{OUT}))^{1/2}$$

For duty ratios less than 0.5, the input capacitor RMS current is higher than the calculated current. Therefore, use a +20% margin when calculating the RMS current at lower duty cycles. Use ceramic capacitors for their low ESR, equivalent series inductance (ESL), and lower cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability. After determining the input capacitor, check the input ripple voltage due to capacitor discharge when the high-side MOSFET turns on. Calculate the input ripple voltage as follows:

$$V_{IN\_RIPPLE} = (I_{OUT} \times V_{OUT}) / (f_{SW} \times V_{IN} \times C_{IN})$$

Keep the input ripple voltage less than 3% of the input voltage.

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and the voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-to-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = I_{P-P} / (8 \times C_{OUT} \times f_{SW})$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = (I_{P-P} / t_{ON}) \times ESL \text{ or } (I_{P-P} / t_{OFF}) \times ESL,$$

whichever is greater

and I_{P-P} the peak-to-peak inductor current is:

$$I_{P-P} = [\ (V_{IN} - V_{OUT}\ ) / f_{SW} \times L)\ ] \times V_{OUT} / V_{IN}$$

Use these equations for initial capacitor selection, but determine final values by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for their low ESR and ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible. Load transient response depends on the selected output capacitor. During a load transient, the output instantly changes by ESR × I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, thus preventing the output from deviating further from its regulating value.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

V_{OUT} = 0.8 × (1 + R1/R2) Volt.

Please keep R2 not larger than 25kΩ and select R1 using the formula.

Efficiency Considerations

Although all dissipative elements in the circuit produce losses, one major source usually account for most of the losses in AT1529 circuits: I^2R losses. The I2R loss dominates the efficiency loss at medium to high load currents.

The I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOTTOM})(1-D)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from Electrical Characteristics table. Thus, to obtained I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal considerations

In most application the AT1529 does not dissipate much heat due to its high efficiency. But, in applications where the AT1529 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the LX node will become high impedance.

Thermal performance can be improved with one of the following options:

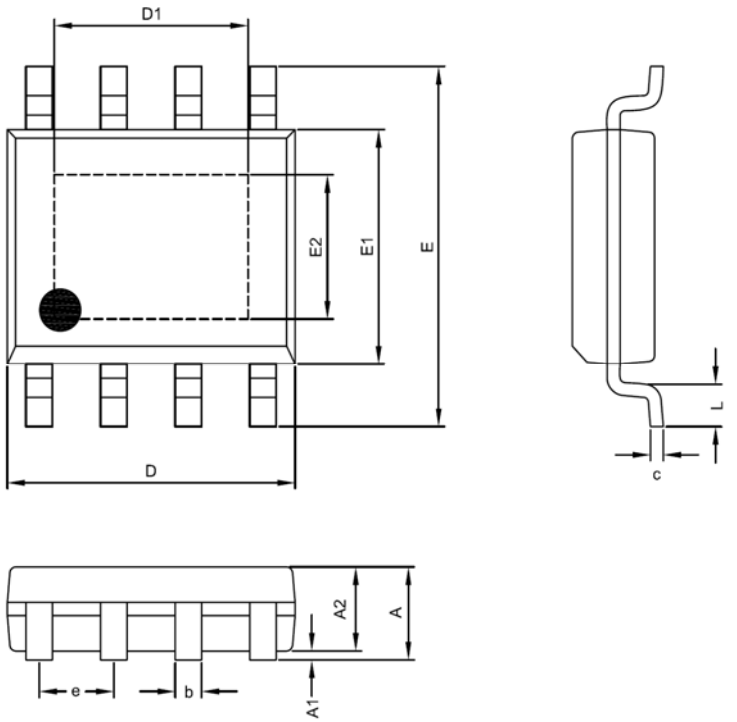
- Increase the copper areas connected to GND, LX, and VIN.
- Provide thermal vias next to GND and VIN, to the ground plane and power plane on the back side of PC board, with openings in the solder mask next to the vias to provide better thermal conduction.
- Provide forced-air cooling to further reduce case temperature.

PC Board Layout Considerations

Careful PC board layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

- Place decoupling capacitors as close to the IC as possible. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
- Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.

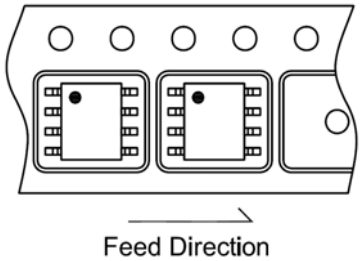
Package Information



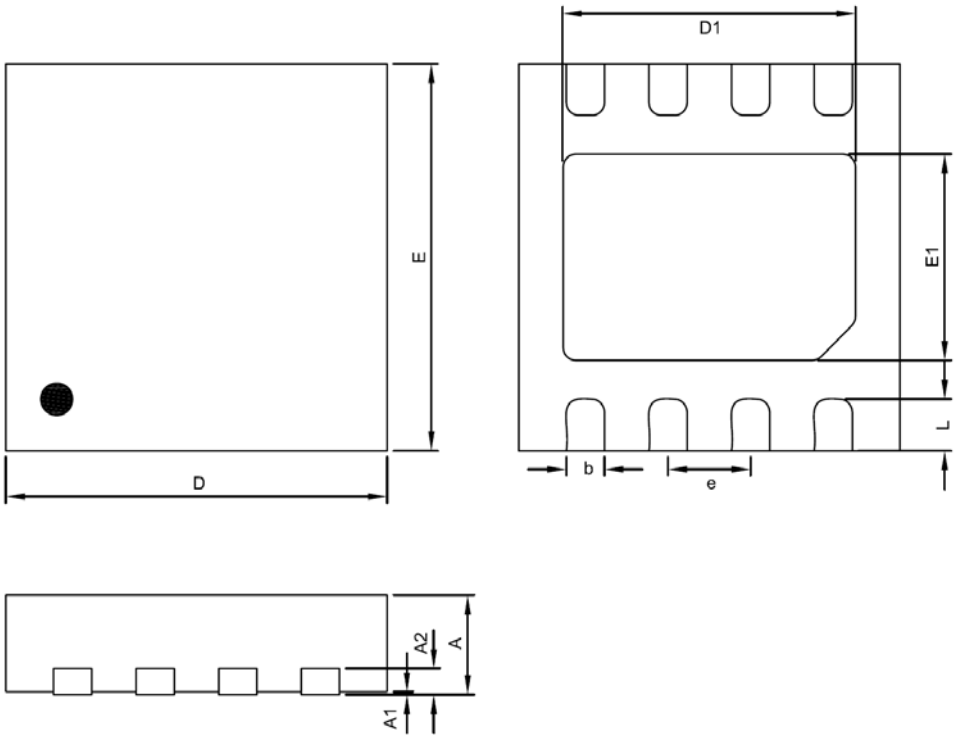
SOP- 8 (FD) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.65	0.053	0.061	0.065
A1	0.00	---	0.15	0.000	---	0.006
A2	1.15	1.35	1.50	0.045	0.053	0.059
D	4.80	4.90	5.00	0.189	0.192	0.197
D1	2.29	---	3.71	0.090	---	0.146
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.153	0.157
E2	2.29	---	2.64	0.090	---	0.104
c	0.19	0.23	0.27	0.007	0.009	0.011
b	0.33	0.43	0.53	0.013	0.017	0.021
e	1.27 BSC			0.050 BSC		
L	0.40	0.70	1.00	0.016	0.028	0.039

Taping Specification



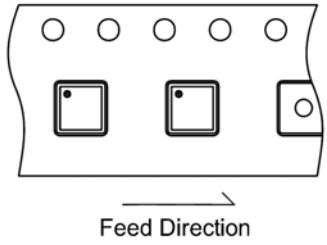
PACKAGE	Q'TY/REEL
SOP-8 (FD)	2,500 ea



TDFN3X3-8 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	2.20	2.30	2.40	0.0866	0.0906	0.0945
E1	1.40	1.50	1.60	0.0551	0.0591	0.0630
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
e	0.65 BSC			0.0256 BSC		
L	0.30	0.35	0.45	0.0118	0.0138	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TDFN3X3-8	3,000 ea