AT1793

Preliminary Product Information

2-Channel Step-Down PWM Controller

Features

- 4.75V to 26V supply voltage operating.
- Efficiency up to 85%.
- Typical frequency operation to 1MHz.
- Voltage-mode PWM step-down regulation.
- 1V±2% internal reference.
- Shutdown current less than 30uA.
- Soft-start built-in.
- Short-circuit protection build-in
- QFN-16 & SOP-14 package.

Applications

•DC-DC power management.

General Description

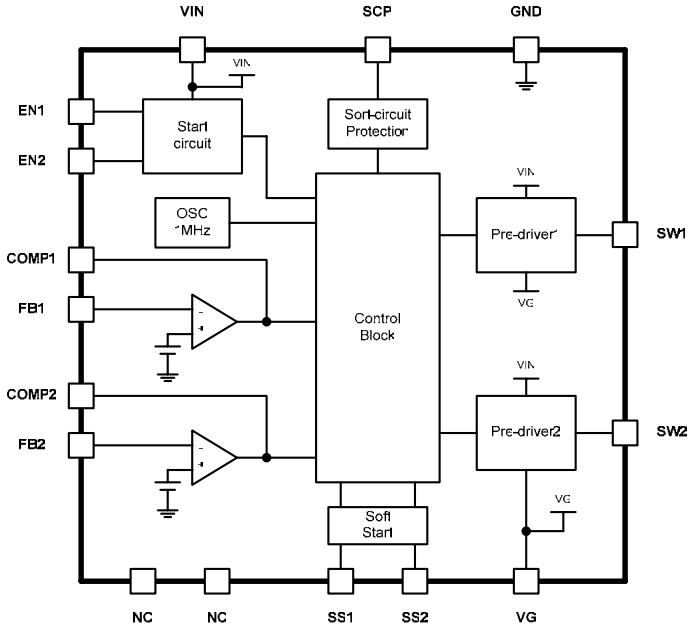
AT1793 is a voltage-mode PWM step-down controller capable of driving loads over a wide input supply range with excellent line and load regulation characteristics. High efficiency is obtained through the use of a low Rds(on) P-channel power switch.

It uses a fixed switching frequency up to 1MHz thus allowing smaller sized components. The output voltage level is user-programmable via an external resistive voltage divider. The built-in soft-start can reduce inrush current on the input source at turn on. The built-in short-circuit protection can prevent from a short-circuit.

The AT1793 also has built-in 2 control pins that can power down the regulator to a shutdown mode. In shutdown mode the regulator draws less than 30uA of supply current

AT1793 is available in QFN-16 or SOP-14 package.

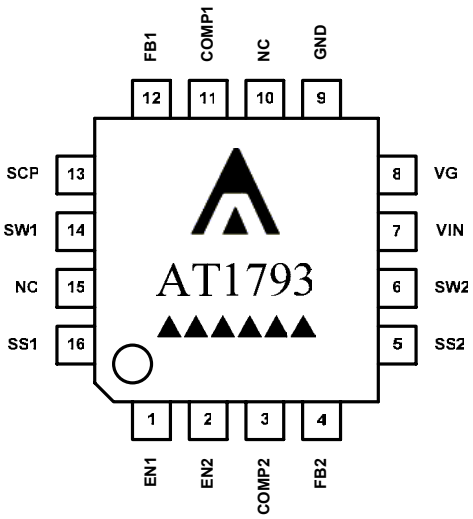
Block Diagram



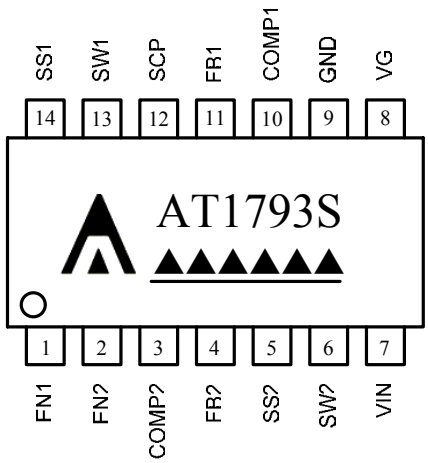
Aimtron reserves the right without notice to change this circuitry and specifications.

Pin Configurations

QFN-16



SOP-14



Ordering Information

Part number	Package	Marking
AT1793N_GRE	QFN16,Green	▲▲▲▲▲▲, Date Code
AT1793S_GRE	SOP14,Green	▲▲▲▲▲▲, Date Code with one bottom line

**For more marking information, contact out sales representative directly*

Pin Description

QFN-16

Symbol	Pin No.	Descript
EN1	1	Enable pin for buck controller 1
EN2	2	Enable pin for buck controller 2
COMP2	3	Error amplifier output 2
FB2	4	DC-DC feedback input 2
SS2	5	Soft start for buck controller2
SW2	6	Switching output 2
VIN	7	Power supply for step down controller
VG	8	Reference Voltage(VIN-5V) for SW Virtual Ground
GND	9	GND
NC	10	NC
COMP1	11	Error amplifier output 1
FB1	12	DC-DC feedback input 1
SCP	13	SCP setting capacitor connection
SW1	14	Switching output 1
NC	15	NC
SS1	16	Soft start for buck controller 1
EP	-	Exposed Paddle. For good thermal dissipation, the exposed pad must be connected to the power ground

SOP-14

Symbol	Pin No.	Descript
EN1	1	Enable pin for buck controller 1
EN2	2	Enable pin for buck controller 2
COMP2	3	Error amplifier output 2
FB2	4	DC-DC feedback input 2
SS2	5	Soft start for buck controller2
SW2	6	Switching output 2
VIN	7	Power supply for step down controller
VG	8	Reference Voltage(VIN-5V) for SW Virtual Ground
GND	9	GND
COMP1	10	Error amplifier output 1
FB1	11	DC-DC feedback input 1
SCP	12	SCP setting capacitor connection
SW1	13	Switching output 1
SS1	14	Soft start for buck controller 1

Absolute Maximum Ratings

Parameter	Condition	Rated Value		Unit
		Min.	Max.	
Power Supply Voltage, VIN	—	—	+28	V
Control Input EN1,EN2	—	—	+5.5	V
Thermal Resistance from Junction to Ambient θ_{JA} *2	QFN-16(3x3)	—	60	^{0}C/W
	SOP-14	—	75	^{0}C/W
Operating temperature T_A	—	-30	+85	^{0}C
Storage temperature	—	-55	+150	^{0}C
ESD Susceptibility *2	HBM	2		KV
	MM	200		V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Measured on approximately 1" square of 1 oz. copper FR4 board.

3. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

(Ta=+25^{0}C)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power supply voltage	VIN	4.75	12	26	V
Operating temperature*	T_A	-20	+25	+85	°C
Operating junction temperature	T_J	-	-	+150	°C

***Using X5R or X7R input capacitors.**

Electrical Characteristics

(VIN=12V, T_a =+25℃ , unless otherwise noted.)

Parameter	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
VIN UVLO threshold	V_{UVLO}		4.1	4.3	4.5	V
UVLO hysteresis			--	0.2	--	V
Quiescent Current	$I_{CC(VIN)}$	EN1=EN2=5V, FB1=FB2=1.5V	--	0.6	1	mA
Current in standby mode 1	$I_{ST(VIN)}$	EN1=EN2=0V, FB1=FB2=1.5V	--	30	50	μA
EN high level voltage	V_{ENH}	The initial state of EN is H level.	2	--	5	V
EN low level voltage	V_{ENL}		0	--	0.5	V
<Step down controller>						
Virtual Ground Voltage	VG		--	VIN-4.5V	--	V
Oscillator Frequency	f_{osc}		0.8	1.0	1.2	MHz
FB Threshold Voltage	V_T		0.98	1	1.02	V
FB Input Bias Current	IT	VFB=1V	--	--	1	μA
SW sink current	I_{SINK}	VFB =0V, VSW =VIN-5V	--	30	--	mA
SW source current	I_{SOURCE}	VFB=1.5V, VSW =VIN-0.5V	--	-30	--	mA
SW rising time	trv	CL =1.5nF, TA=25^{0}C	--	125	--	ns
SW falling time	tfv	CL =1.5nF, TA=25^{0}C	--	125	--	ns
< Soft start >						
Charging current	I_{CSS}		2	4	6	μA
Voltage at soft start completion	V_{tss}		0.4	0.5	0.6	V
< Short circuit detection and protection>						
Charging current	I_{CSCP}	SS1 and SS2>0.5V VFB1 or VFB2<0.8V	2	4	6	μA
Threshold voltage	V_{tscp}	SS1 and SS2>0.5V VFB1 or VFB2<0.8V	0.7	0.8	0.9	V

Truth table of mute mode operation

EN1	EN2	CH I	CH II
H or Floating	L	Active	Disable
L	H or Floating	Disable	Active

Typical Application Circuit

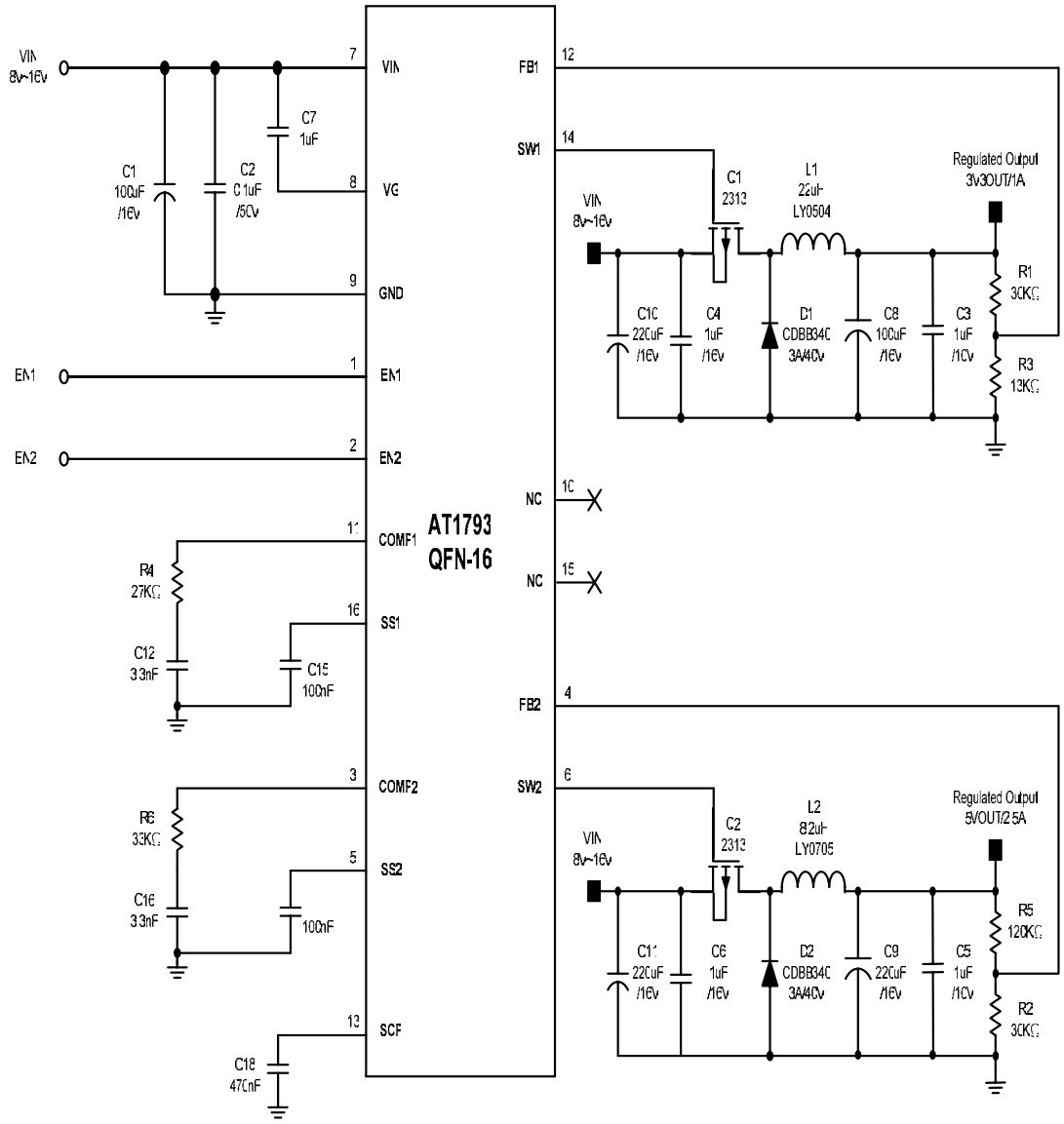


Fig. 1: Typical application circuit for QFN-16 of AT1793

Typical Application Circuit

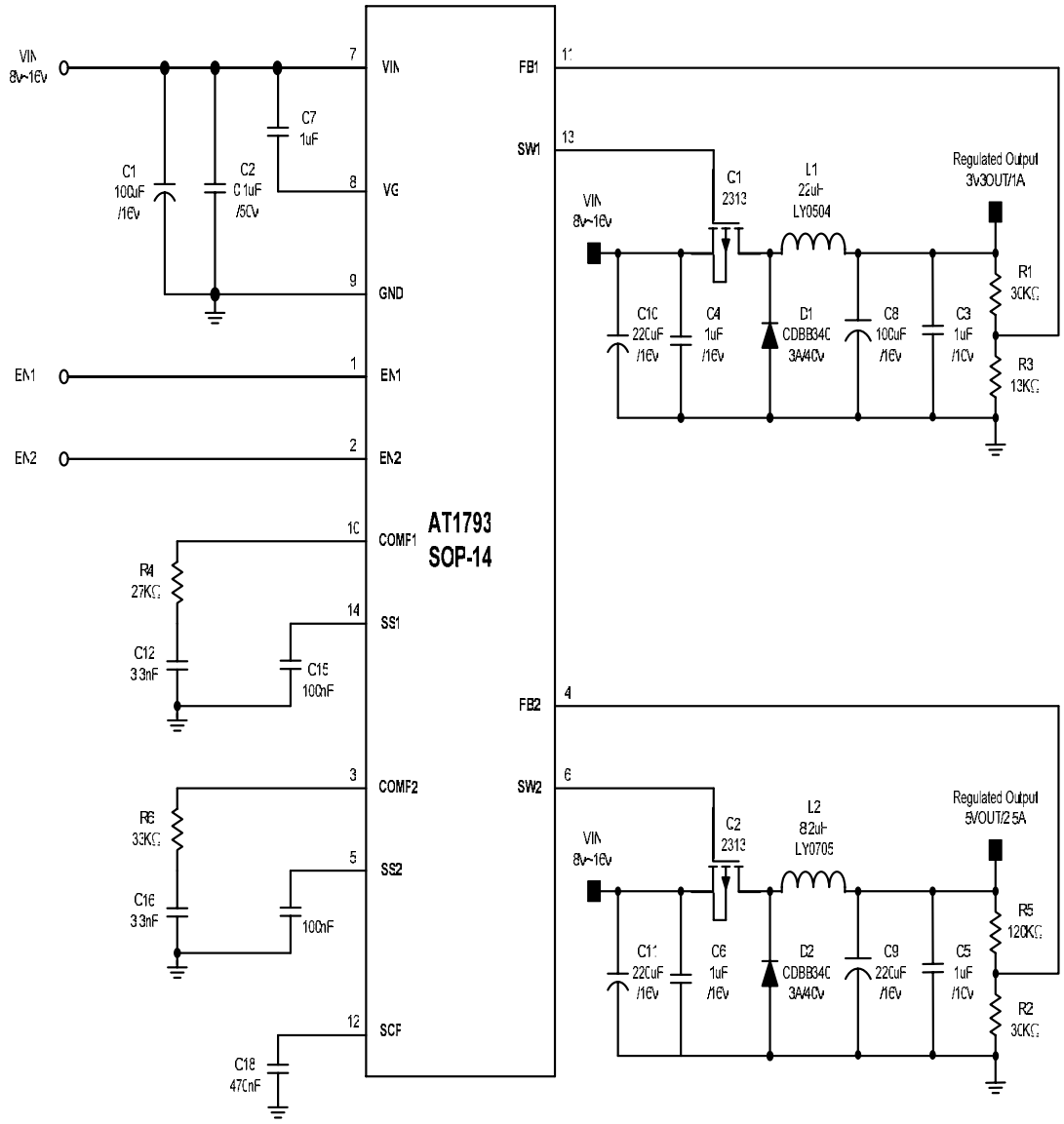


Fig. 2: Typical application circuit for SOP-14 of AT1793

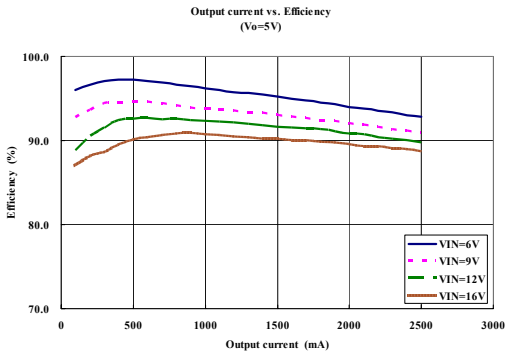
Application Data :

Table 1 : Quick Design Component Selection Table

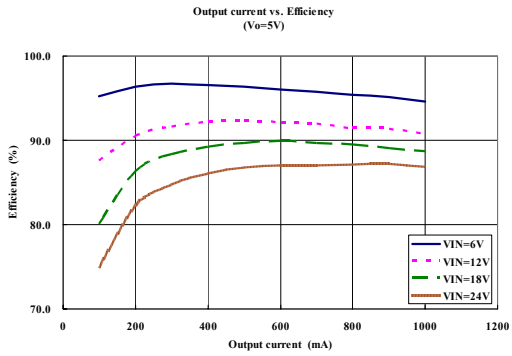
		Ex1	Ex2	Ex3	Ex4	Ex5	Ex6
Input Voltage	VIN	12	24	12	24	12	12
Output Voltage	Vo	5		3.3		2.5	1.8
Load	Io	2.5A	1A	1A	2A	1.5A	2A
Feedback Voltage	R1/R2	120KΩ		30KΩ		15 KΩ	12 KΩ
	R3/R4	30 KΩ		13 KΩ		10 KΩ	15 KΩ
MOSFET	Q1/Q2	2313	2313	2313	2313	2313	2313
Input Capacitor	C10/C11	220uF /16V	100uF /35V	220uF /16V	220uF /35V	220uF /16V	220uF /16V
	C4/C6	1uF /16V	1uF/50V	1uF/16V	1uF/50V	1uF/16V	1uF/16V
Inductance	L1/L2	8.2uH LY0705 0.05Ω/2.5A	22uH LY0504 0.18Ω/1.1A	22uH LY0504 0.18Ω/1.1A	10uH LY0705 0.1Ω/1.4A	8.2uH LY0504 0.09Ω/1.5A	10uH LY0504 0.1Ω/1.4A
Diode	D1/D2	CDBA340	CDBA340	CDBA340	CDBA340	CDBA340	CDBA340
Output Capacitor	C8/C9 ESR	220uF/16V 117mΩ	100uF/16V 250mΩ	100uF/16V 250mΩ	100uF/16V 250mΩ	100uF/16V 250mΩ	100uF/16V 250mΩ
	C3/C5	1uF/16V	1uF/16V	1uF/16V	1uF/16V	1uF/16V	1uF/16V
Compensator	R4/R6	33KΩ	22KΩ	27KΩ	6.2KΩ	8.2KΩ	7.5KΩ
	C12/C16	3.3nF	5.1nF	3.6nF	22nF	10nF	22nF

Typical Characteristics :

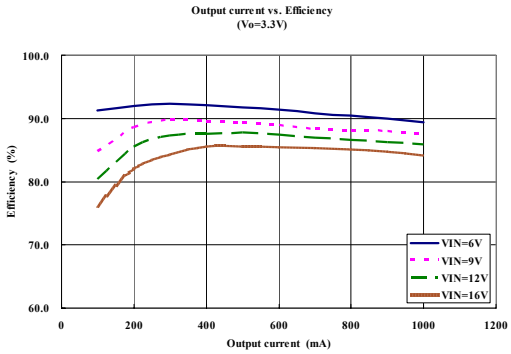
- The Efficiency of Ex1 (OUT=5V)



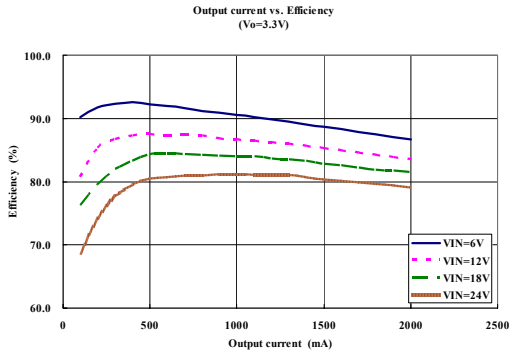
- The Efficiency of Ex2 (OUT=5V)



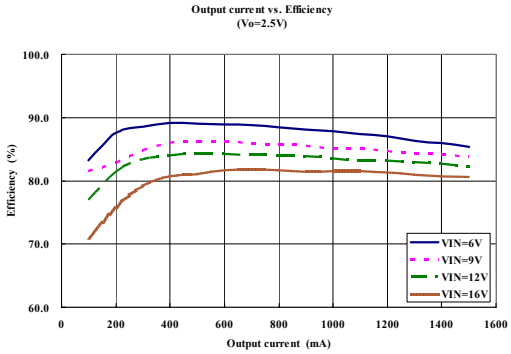
- The Efficiency of Ex3 (OUT=3.3V)



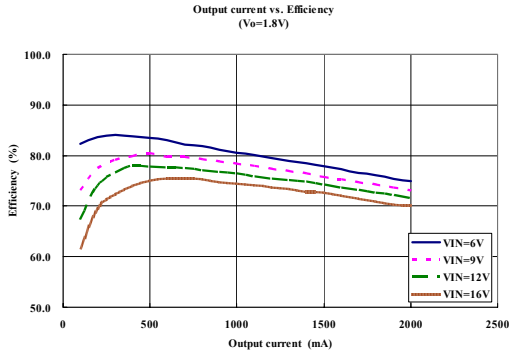
- The Efficiency of Ex4 (OUT=3.3V)



- The Efficiency of Ex5 (OUT=2.5V)



- The Efficiency of Ex6 (OUT=1.8V)



Typical Characteristics :

- **Output ripple (** CH1=drain terminal of MOS, CH3=Output voltage ripple)

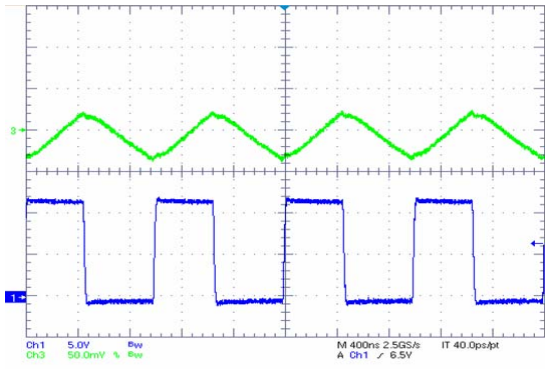


Fig. 3: Ex1,VIN=12V, Vo=5V, Io=2.5A

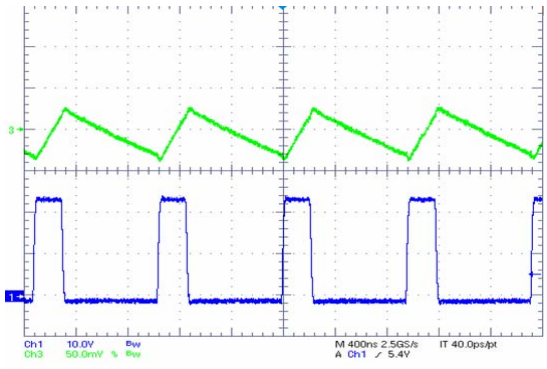


Fig. 4: Ex2, VIN=24V, Vo=5.0V, Io=1A

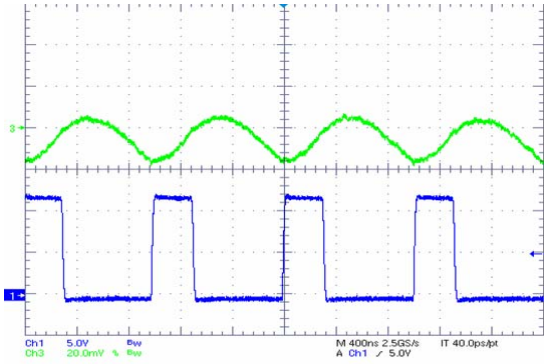


Fig. 5: Ex3, VIN=12V, Vo=3.3V, Io=1A

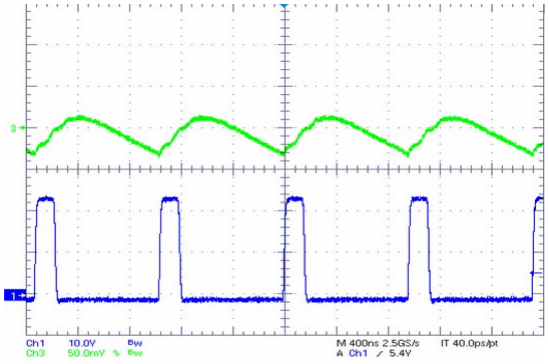


Fig. 6: Ex4, VIN=24V, Vo=3.3V, Io=2A

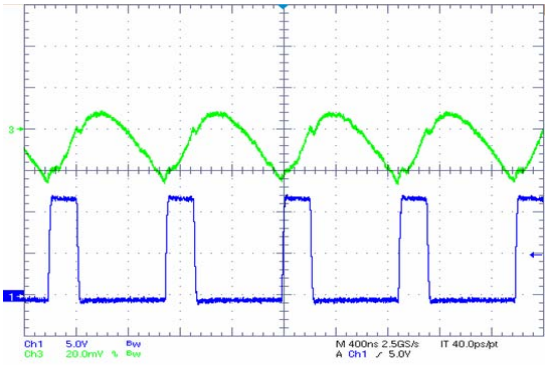


Fig. 7: Ex5, VIN=12V, Vo=2.5V, Io=1.5A

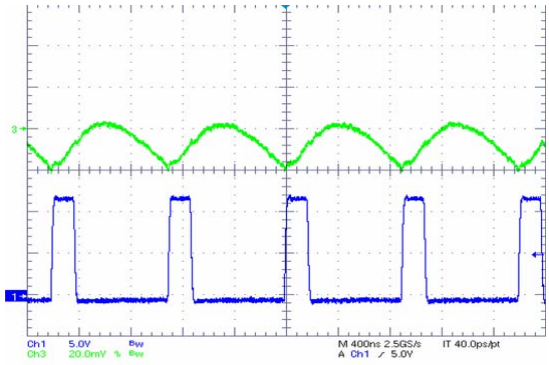


Fig. 8: Ex6, VIN=12V, Vo=1.8V, Io=2A

Typical Characteristics :

- **Load Transient Response (** CH3=Output voltage, CH4=Io.)

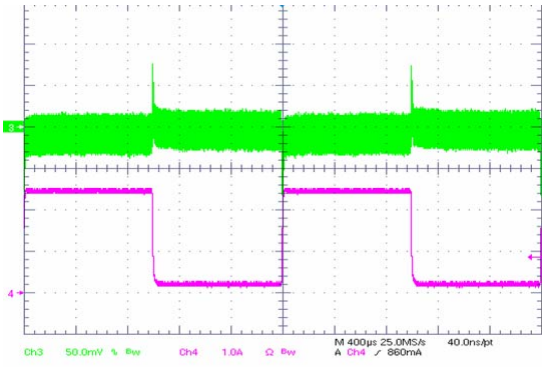


Fig. 9: Ex1,VIN=12V, Io=0.25A to 2.5A

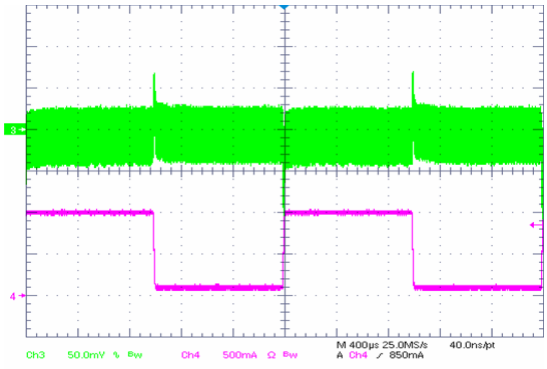


Fig. 10: Ex2, VIN=24V, Vo=5.0V, Io=0.1A to 1A

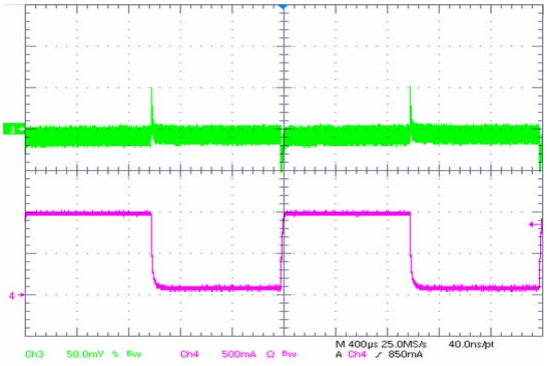


Fig. 11: Ex3, VIN=12V, Vo=3.3V, Io=0.1A to 1A

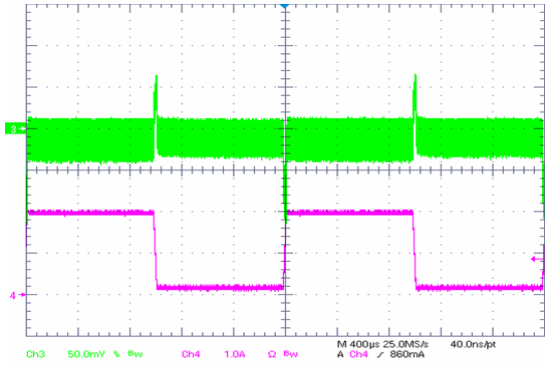


Fig. 12: Ex4, VIN=24V, Vo=3.3V, Io=0.2A to 2A

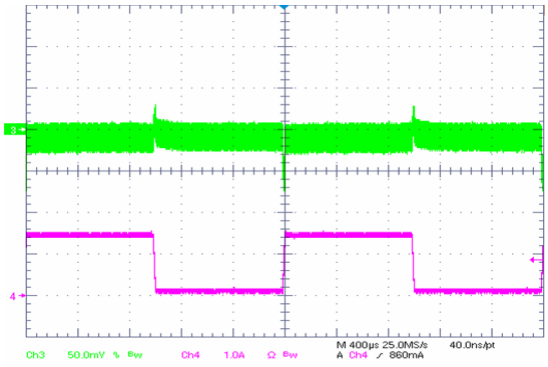


Fig. 13: Ex5, VIN=12V, Vo=2.5V, Io=0.15A to 1.5A

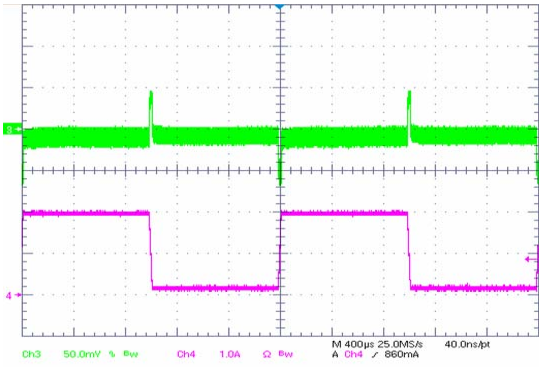


Fig. 14: Ex6, VIN=12V, Vo=1.8V, Io=0.2A to 2A

Application Information

1. Mute mode

There are two control pins for mute mode of AT1793. EN1 and EN2 control 2-CH DC-DC step-down controller, separately. The initial state of EN1 and EN2 is high level voltage (internal pull high). **Noted that, the maximum high level voltage of these control pins are 5V**. The following table indicates the details of operation for control mode.

Table 2 : Truth table of mute mode operation

EN1	EN2	DC-DC I	DC-DC II
H or Floating	L	Active	Disable
L	H or Floating	Disable	Active

2. Soft start

The A1793 offers soft start for 2-CH DC-DC step-down controller. The value of the capacitor, C_{SS}, on the SS pin sets the ramp rate of the inrush current profile at startup. During soft-start, 4μA is sourced into the C_{SS} connected from SS pin to GND causing the reference voltage to ramp up slowly. When voltage of SS pin reaches V_{tSS} the output becomes fully active. Set the soft-start time using the following equation:

$$t_{SS}(s) = \frac{V_{tSS}(V) \times C_{SS}(F)}{4(\mu A)}$$

For example, the C_{SS} is set to be 100nF, and the t_{SS} can be calculated to be 12.5ms.

3. Short circuit protection

The short circuit protection will enable after the DC-DC controller finishing sort-start. When V_{SS} exceeds V_{tSS} and VFB decreases to 0.8V, the SCP start to charge the C_{SCP} till V_{tSCP} by 4uA. The SCP will turn off 2-CH controller when V_{SCP} exceeds V_{tSCP}. Two operations can achieve to re-enable the 2-CH DC-DC controller. One is that user must power on AT1793 after powering down. Another is that user should pull high level voltage at EN1 and EN2 after pulling low level voltage.

$$t_{SCP}(s) = \frac{V_{tSCP}(V) \times C_{SCP}(F)}{4(\mu A)}$$

For example, the C_{SCP} is set to be 470nF, and the t_{SS} can be calculated to be 94ms.

Application Information

4. Regulator Design Procedure

$$L_{min} \geq \frac{V_O \times (1-D) \times T_S}{2 \times I_{OB}} = \frac{V_{i(max)} \times D \times (1-D) \times T_S}{2 \times I_{OB}} = \frac{(V_{i(max)} - Vo) \times D \times T_S}{2 \times I_{OB}}$$

Application Example:

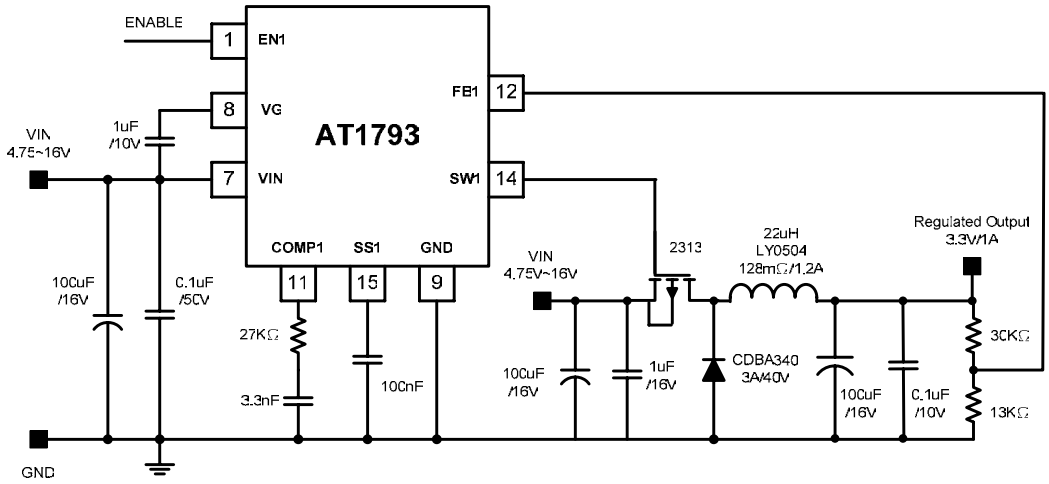


Fig. 15. Using AT1793 to Buck Converter

*** Design Procedure :**

VIN=12V, Vo=3.3V, Io=1A, fosc=1MHz, and the circuit becomes DCM mode, typical value is 10% of the full load (IOB).

VSAT is internal switch saturation voltage of the 2313 (90mΩ*0.6A=0.054V)

$$D = \frac{V_O + V_F}{V_i - V_{SAT} + V_F} = \frac{3.3 + 0.5}{12 - 0.054 + 0.5} = 0.305$$

VF is forward voltage drop of the output rectifier.(0.5V)

Application Information

4-1. Inductor L1:

The condition of L because of a continuous current in the range of the use voltage

$$L \geq \frac{V_O \times (1-D) \times T_S}{2 \times I_{OB}}$$
$$\geq \frac{3.3 \times (1-0.305) \times 1 \times 10^{-6}}{2 \times 0.1} \geq 11.47uH$$

Select L=22μH, Load current value which becomes continuous current condition.

$$I_{OB} \geq \frac{V_O \times (1-D) \times T_S}{2 \times L} = \frac{3.3 \times (1-0.305) \times 1 \times 10^{-6}}{2 \times 22 \times 10^{-6}} \geq 0.052A$$

If IO≥IOB

$$\Delta I_L = \frac{(V_{i(max)} - V_O) \times t_{ON}}{L} = \frac{(V_{i(max)} - V_O) \times D \times T_S}{L}$$

The peak value of the inductor I_L(peak)

$$I_{L(peak)} = I_O + \frac{\Delta I_L}{2} = I_O + \frac{(V_i - V_O) \times t_{ON}}{2 \times L}$$

$$I_L \geq I_{L(peak)} = 1 + \frac{(12-3.3) \times 0.305 \times 1 \times 10^{-6}}{2 \times 22 \times 10^{-6}} = 1.06A$$

→ Select LY0504-220 (22μH,180mΩ/1.11A). As a result, the condition is satisfied.

4-2. Diode D1:

The peak value of diode current IFSM

$$I_{FSM} \geq 1 + \frac{(12-3.3) \times 0.305 \times 1 \times 10^{-6}}{2 \times 22 \times 10^{-6}} = 1.06A$$

The Average Current IF

$$I_F \geq I_O \geq 1A$$

The repetition peak reverse voltage of the diode VRRM. The reverse voltage rating of the output rectifier should be at least 1.5 times the maximum input voltage.

$$V_{RRM} \geq 1.5 \times V_i \geq 18V$$

→ Select CDBA340(40V/3A). As a result, the condition is satisfied.

Application Information

4-3. Output Capacitor:

If the desired output ripple voltage is 50mV, then the ESR needed is:

$$ESR \le \frac{\Delta V_O}{\Delta I_L} - \frac{1}{8 f_s C} \cong \frac{\Delta V_O}{\Delta I_L} = \frac{0.05}{0.122} = 410m\Omega$$

$$V_{WVDC} \ge 1.5 \times V_O \ge 4.95V$$

$$I_{RMS} = \frac{\Delta I_L}{2\sqrt{3}} = 0.289 \times 0.122 = 0.035A_{RMS}$$

4-4. Input Capacitor:

The value of input capacitor RMS current can be calculated from the following expression:

$$I_{RMS} = \sqrt{D \times (I_{OUT}{}^2 + \frac{\Delta I_L{}^2}{12})} = \sqrt{0.305 \times (1^2 + \frac{0.122^2}{12})} \approx 0.553A$$

$$V_{WVDC} \ge 1.5 \times V_I \ge 18V$$

Application Information

5. Compensation Design Procedure

A proper compensation should meet the steady-state and transient response requirements of buck converter. The Fig. 16 shows that the typical compensator can be a lag compensator consists of a resistor, R_C, and a capacitor, C_C. The lag compensator can boost the DC gain and have a higher control bandwidth to improve the performance of transient response.

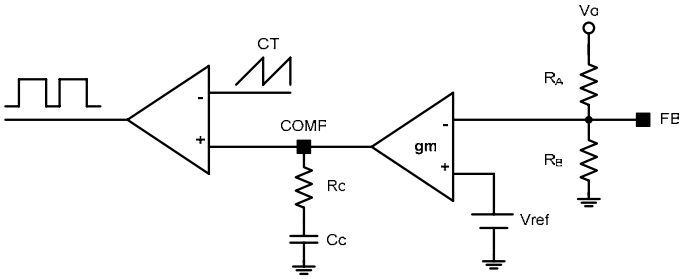


Fig. 16: Loop compensation.

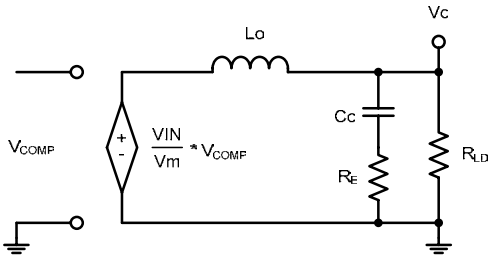


Fig. 17: Small signal model of control loop and power stage.

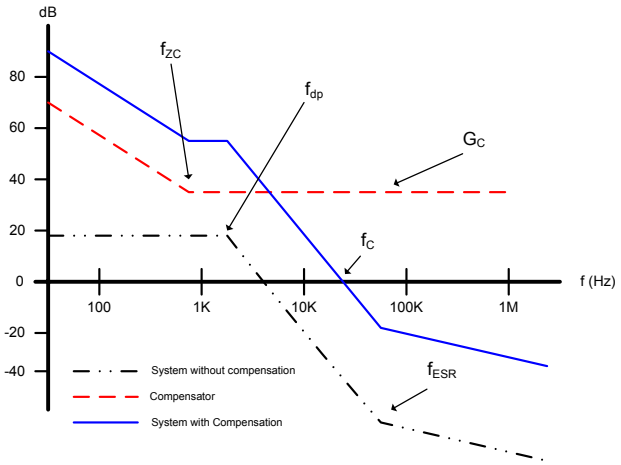


Fig. 18: Bode plots of the transfer function

Application Information

The typical system loop can be divided into two parts. One is the loop compensator showed in Fig. 16. Another is control loop and power stage, and its small signal model is illustrated in Fig.17. In the model, L_O is the output inductor. C_O is the output capacitance and R_E is the ESR. R_{LD} is the load resistance. V_{COMP} is the voltage at COMP pin and V_m is the peak-to-peak voltage of the PWM ramp, CT, which is 0.5V in the case of AT1793.

The DC gain of the control loop transfer function is showed as

$$G_{dc} = \frac{VIN}{V_m} \tag{5.1}$$

The double poles occur at

$$f_{dp} = \frac{1}{2\pi} \times \sqrt{\frac{1}{L_O C_O}} \tag{5.2}$$

The ESR zero can be produced by

$$f_{ESR} = \frac{1}{2\pi} \times \frac{1}{R_E C_O} \tag{5.3}$$

It is typically that decreasing the ESR by paralleling a ceramic capacitor to reduce output voltage ripple. But smaller ESR might deteriorate the phase-margin to be critical stable. The phase margin of 45 degree is typical. The trade-off between smaller output voltage ripple and enough phase-margin will be concerned. Generally, 1uF or less capacitance of a ceramic capacitor can be accepted.

Refer to Fig. 18 for asymptotic bode plot of the control loop. The lag compensator has one pole-zero pair. The pole occurs at zero frequency, and the zero is determined by

$$f_{ZC} = \frac{1}{2\pi} \times \frac{1}{R_C C_C} \tag{5.4}$$

Application Information

The place of the zero also affects the loop stability. This f_{ZC} must be less than f_{dp}.

The cut-off frequency, f_C, is where the loop transfer function has 0 dB gain in bode plot. f_C is also referred to as control bandwidth. In the time domain, the control bandwidth can translate into a faster load transient recovery speed.

Typically, the control bandwidth will be chosen as (5.5).

$$5 \le \frac{f_{SW}}{f_C} \le 10 , \tag{5.5}$$

where f_{SW} means the switching frequency of MOSFET. If f_C is too larger, the gain at switching frequency will be boosted and the loop stability will be disturbed by switching noise.

To calculate the compensation values, using following equations.

$$R_C = \frac{G_C}{gm} \times \frac{R_A + R_B}{R_B} , \tag{5.6}$$

and

$$C_C = \frac{1}{2\pi \times f_{ZC} \times R_C} \tag{5.7}$$

where G_C is the compensator gain beyond compensation zero frequency, f_{ZC}.

Application Information

Application example:

In AT1793 case, as Ex2, f_{SW}=1MHz, gm=270umho, V_m=0.5V, R_A=30KΩ, R_B=13kΩ, L_O=22uH, C_O=100uF, R_E=250mΩ. According (5.1) to (5.3), G_{dc}=27.6dB, f_{dp}=3.39KHz, and f_{ESR}=6.37KHz.

Because f_{SW}=1MHz, the f_C can be chosen to be 100KHz. The G_C can be get by (5.8).

$$G_C = \left| G_{dc} - 40 \times \log\left(\frac{f_{ESR}}{f_{dp}}\right) - 20 \times \log\left(\frac{f_C}{f_{ESR}}\right) \right| \quad (5.8)$$

Then, the G_C=7.25dB. Due to (5.7), R_C=28.22KΩ, C_C=3.76nF.

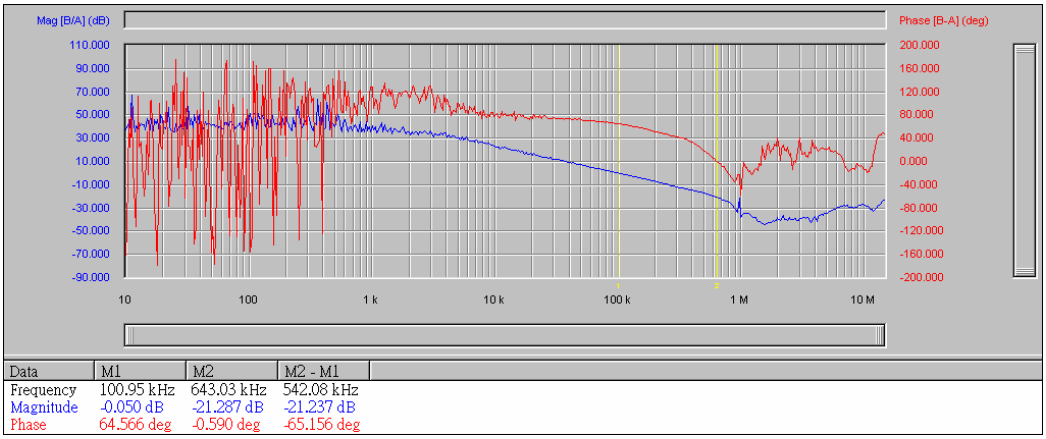
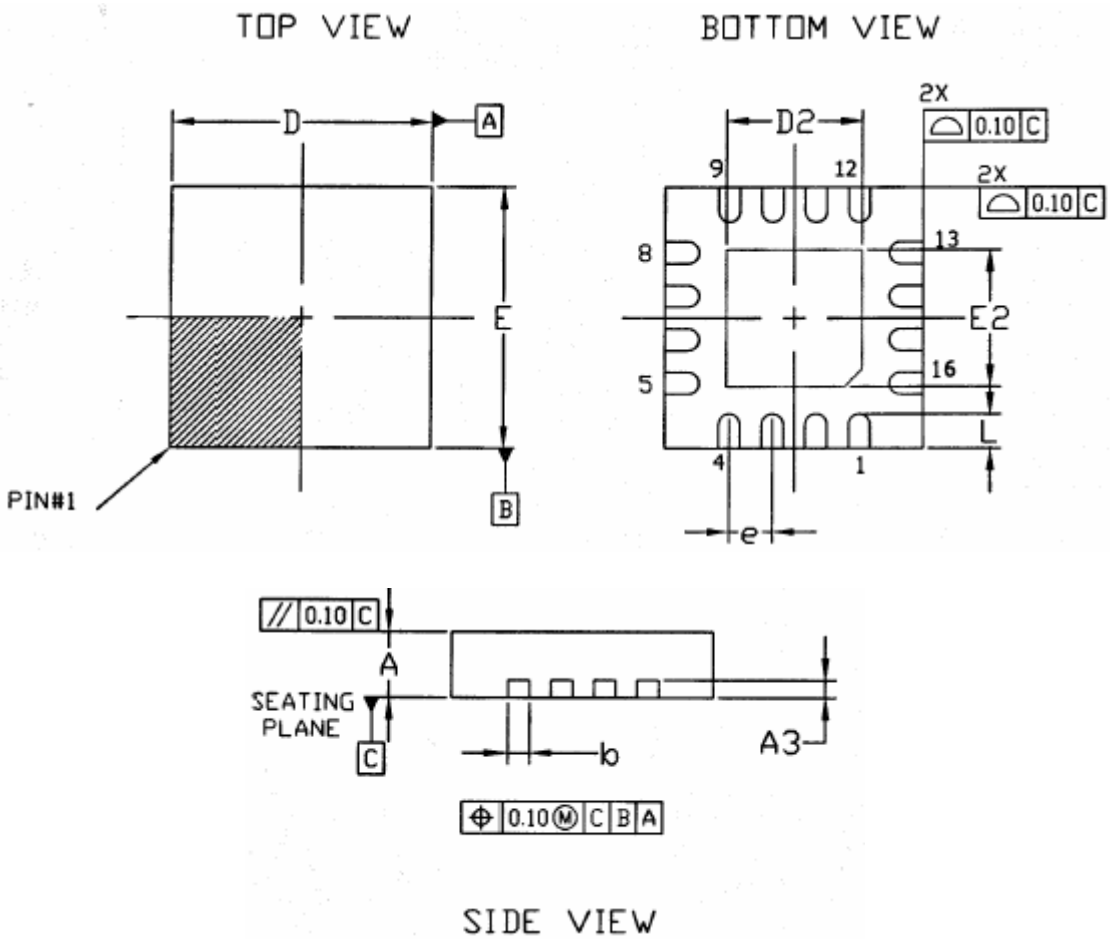


Fig. 19: The bode plot of 3V3OUT loop. GM=21dB, PM=64.6.

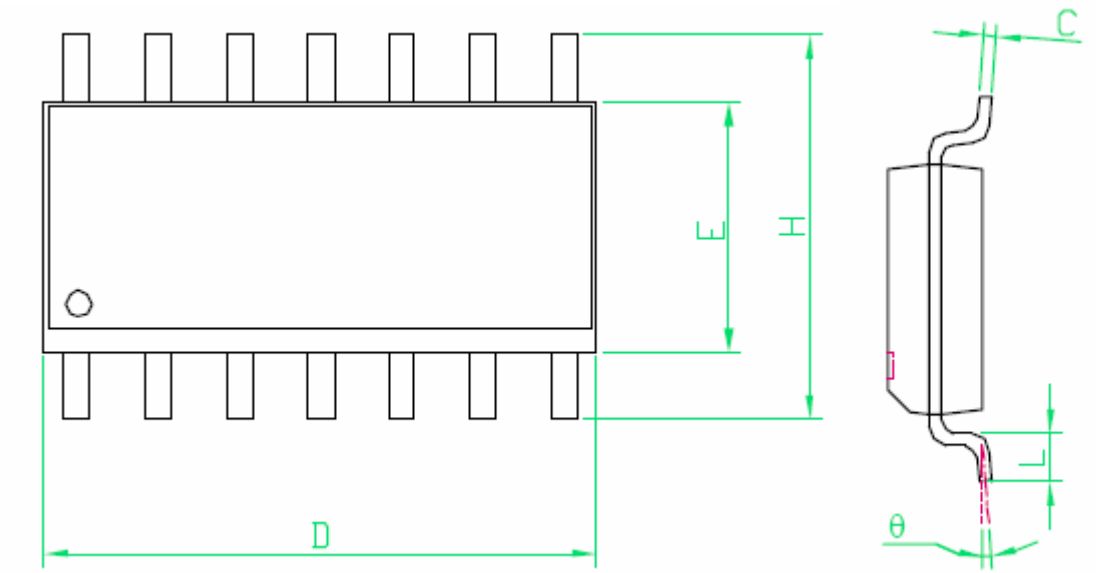
Fig. 19 shows the bode plot of overall loop using above components. The bandwidth is 100.95KHz. The phase margin is 64.6 degree and gain margin is 21dB. This result fits with except design purpose.

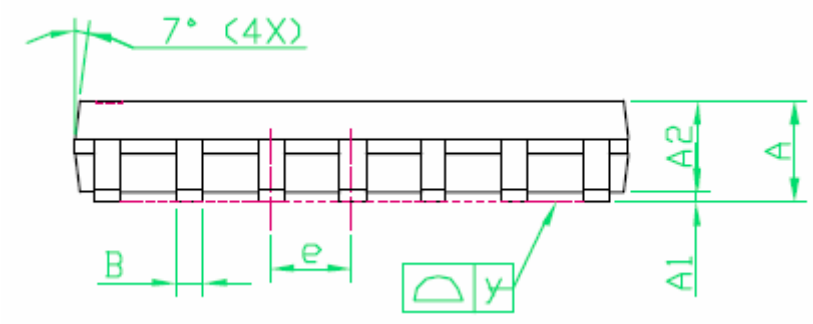
Package Outline : QFN-16



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.027	0.031	0.7	0.8	-
A3	0.008 REF.		0.20 REF.		-
b	0.007	0.012	0.18	0.30	-
D	0.12 BSC.		3.00 REF.		-
D2	0.058	0.065	1.47	1.67	-
E	0.12 REF.		3.00 REF.		-
E2	0.058	0.065	1.47	1.67	-
e	0.020 REF.		0.50 REF.		-
L	0.012	0.020	0.30	0.50	-

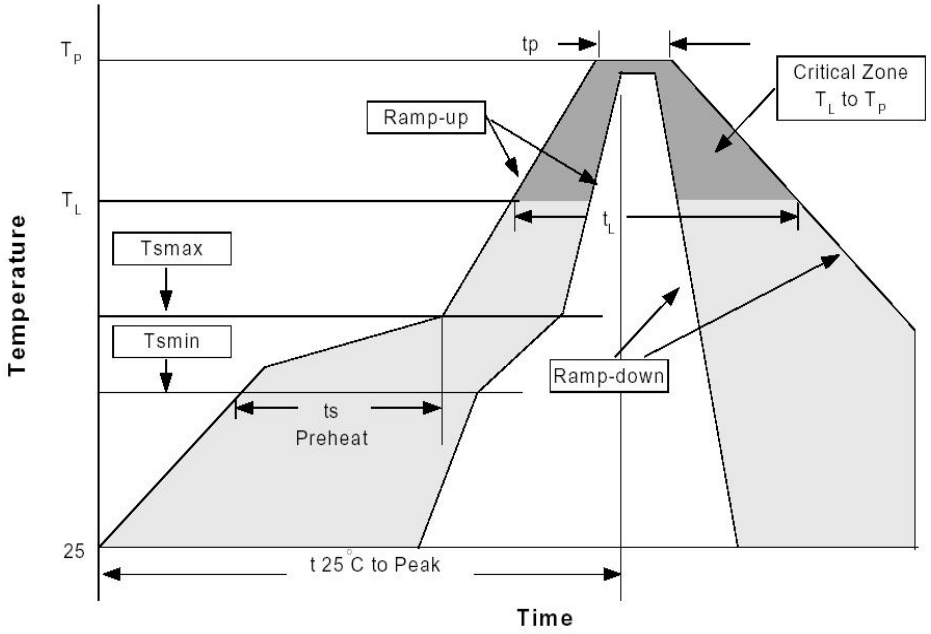
Package Outline : SOP-14





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	---	1.45	---	---	0.057	---
B	0.33	---	0.51	0.013	---	0.020
C	0.19	---	0.25	0.007	---	0.010
D	8.55	---	8.75	0.337	---	0.344
E	3.80	---	4.00	0.150	---	0.157
e	---	1.27	---	---	0.050	---
H	5.80	---	6.20	0.228	---	0.244
L	0.40	---	1.27	0.016	---	0.050
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm³	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm³**	**Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm³**	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm³**
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L -Ramp-up Rate			3°C/second max.	
Time maintained above: -Temperature (T_L) -Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(T_P)	225+0/-5°C	240+0/-5°C	245+0/-5°C	250+0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

***All temperatures refer to topside of the package, measured on the package body surface.**