AT1818

3.0A Ultra Low Dropout Regulator

Immense Advance Tech.

FEATURES

- 250mV dropout @2A
- Input voltage range: 1.8V to 5.5V
- Enable Function
- Over current and over temperature protection
- 5µA quiescent current in shutdown
- P-CH design to reduce the operation current
- Full industrial temperature range
- Adjustable output voltage range 0.8V to 5V
- Output voltage accuracy ± 2%
- Supply current typically 0.4mA
- VOUT Power Good Signa

APPLICATION

- Notebook computers
- Battery powered systems
- Motherboards/Peripheral cards
- Telecom/Networking cards
- Industrial Applications
- Set top boxes
- Wireless infrastructure
- Medical equipment
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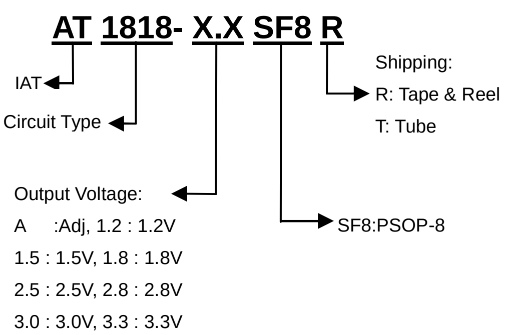
DESCRIPTION

The AT1818 is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A amps. It operates with a VIN as low as 1.8V, with output voltage programmable as low as 0.8V. The AT1818 features ultra low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, the AT1818 has an enable pin to further reduce power dissipation while shut down. The enable pin may be tied to V_{IN} if it is not required for ON/OFF control. The AT1818 provides excellent regulation over variations in line , load and temperature. The AT1818 provides a Power Good signal to indicate if the voltage level of V_{OUT} reaches 92% of its rating value.

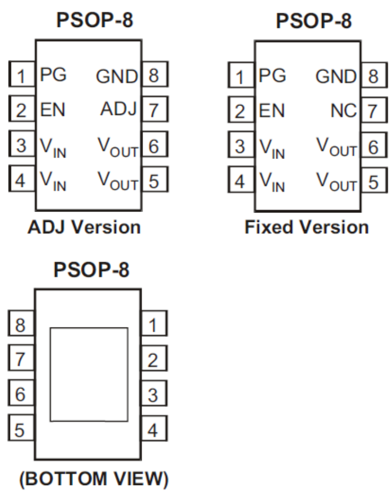
The AT1818 is available in the PSOP-8(Exposed Die Pad) package. The adjustable output version that can be programmed from 0.8V to 5V with two external resistors.

The optimum thermal condition has to consider the layout placement and application to achieve its satisfied high output current requirement.

ORDER INFORMATION



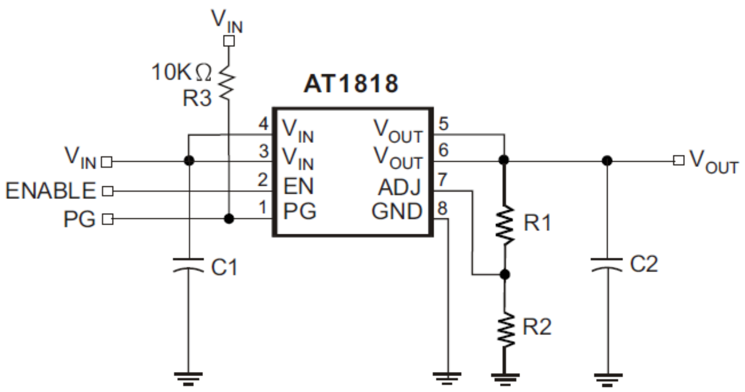
PIN CONFIGURATIONS (TOP VIEW)



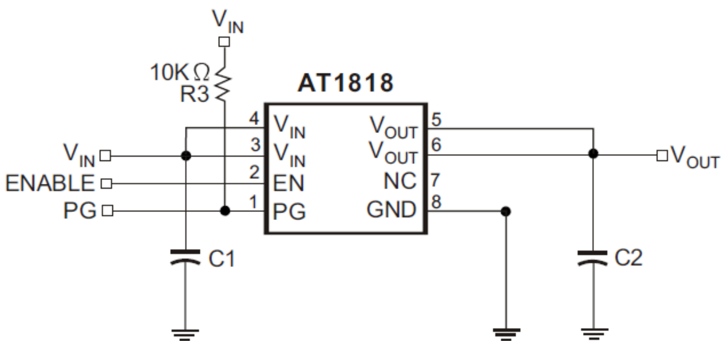
PIN DESCRIPTIONS

Pin Name	Pin Description
PG	Assert high once V_{OUT} reaches 92% of its rating voltage. Open-drain output.
EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to V_{IN} if not being used.
V_{IN}	Input Voltage. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.8V.
V_{OUT}	The pin is the power output of the device.
ADJ	For the adjustable versions of the AT1818. This is the input to the error amplifier. The ADJ reference voltage is 0.8V referenced to ground. The output range is 0.8V to 5V $V_{OUT} = \frac{0.8(R1+R2)}{R2}$ Volts
GND	Reference Ground.
THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not electrically connected internally.

TYPICAL APPLICATION CIRCUITS

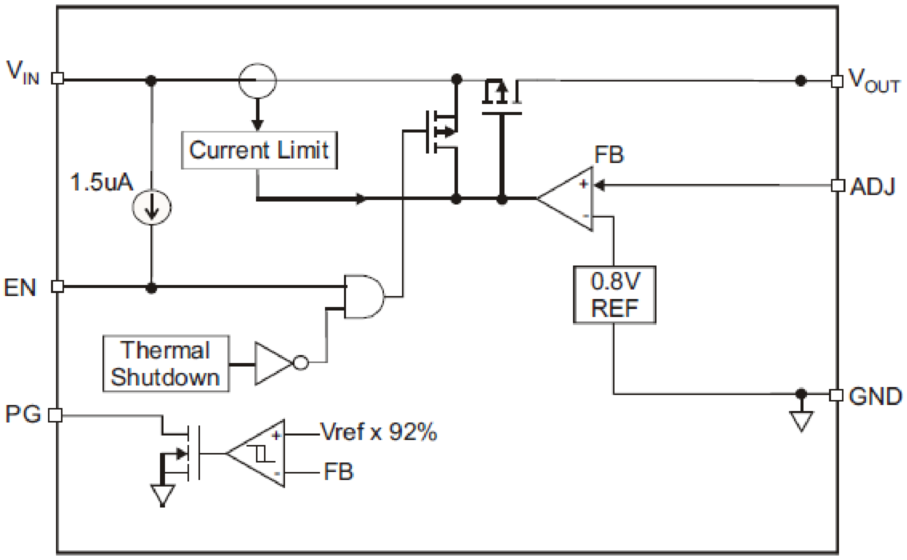


$$V_{OUT} = \frac{0.8V(R1+R2)}{R2} \text{ Volts}$$

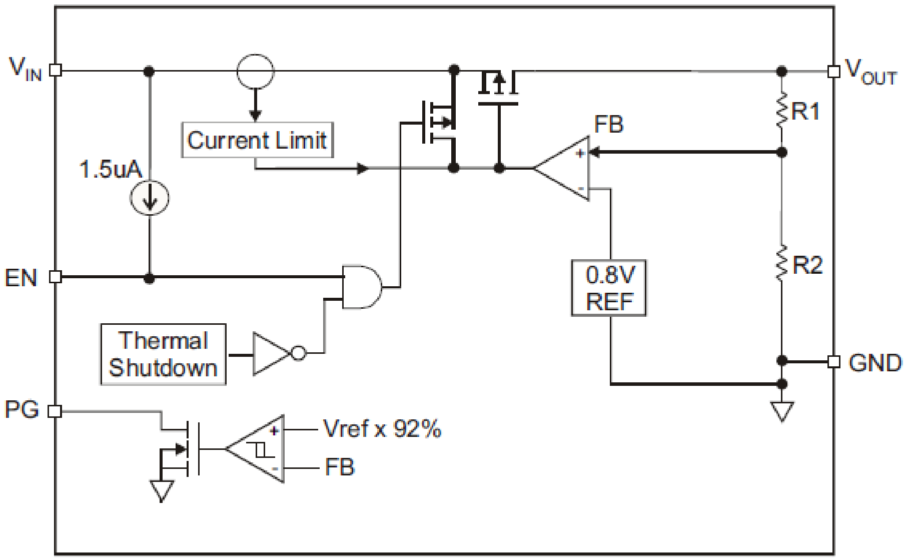


BLOCK DIAGRAM

ADJ Version



Fixed Output Version



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Max Value	Unit
V_{IN}, EN, V_{OUT}, PG, addition Absolute Voltage		6	V
Power Dissipation	P_D	Internally Limited	W
Operating Ambient Temperature Range	T_A	-40 to 85	℃
Operating Junction Temperature Range	T_J	-40 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +125	
Lead Temperature(Soldering) 5 Sec.	T_{LEAD}	260	℃
ESD Rating (Human Body Mode)	V_{ESD}	2	kV
Thermal Resistance Junction to Ambient (Note 2)	θ_{JA}	36	℃/W

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: 2 square inch of FR-4 , double sided, 1 oz. minimum copper weight.

ELECTRICAL CHARACTERISTICS

Unless specified: V_{EN} =V_{IN}.Adjustable version: V_{IN} =3.3V and I_{LOAD} = 10μA to 2A, Fixed version: V_{IN} = V_{OUT} +0.8V and I_{LOAD} = 10μA to 2A.,T_J=25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
V_{IN}						
Supply Voltage Range	V_{IN}		1.8	—	5.5	V
Supply Current	I_{SS}		—	0.4	1.45	uA
Quiescent Current	I_Q	V_{IN} = 5.5V,V_{EN} = 0V	—	5	10	uA
V_{OUT}						
Output Voltage Accuracy(Note 3)	V_{OUT}	V_{IN}=V_{OUT}+0.8V,I_{LOAD}=10mA	-2	V_{OUT}	+2	%
Line Regulation (Note 3)	Reg_line	V_{IN}=(V_{OUT}+0.8V), to 5.5V,I_{LOAD}=10mA	—	0.2	1.0	%/V
Load Regulation (Note 3)	Reg_load	V_{IN} =(V_{OUT}+0.8V), 10mA≤I_{LOAD}≤2A	—	0.1	1.0	%
Dropout Voltage (Note 3,4)	V_D	Fix.1.2V≤V_{OUT}≤1.5, I_{LOAD}=2A Fix. 1.5＜V_{OUT}, I_{LOAD}=2A	—	550 250	650 350	mV
		Adj. V_{OUT}=2.5V, I_{LOAD}=2A	—	250	350	
Current Limit (Note 3,5)	I_{CL}		—	3.6	—	A
ADJ						
Reference Voltage (Note 3)	V_{REF}	V_{IN}=3.3V, V_{ADJ}=V_{OUT}, I_{LOAD} =10mA	0.788	0.8	0.812	V
Adjust Pin Current (Note 6)	I_{ADJ}	V_{ADJ} = V_{REF}	—	80	200	nA

EN						
Enable Pin Current	I_{EN}	V_{EN}=0V	—	1.5	10	μA
Enable Pin Threshold	V_{IH}		1.6	—	—	V
	V_{IL}		—	—	0.4	V
PG						
V_{OUT} Power Good Voltage	V_{THPG}		—	92	—	%
Hysteresis	T_{HYPG}		—	7	—	%
Over Temperature Protection						
High Trip Level	T_{HI}		—	160	—	℃
Hysteresis	T_{HYST}		—	20	—	℃

Note 3: Low duty cycle pulse testing with Kelvin connections required.

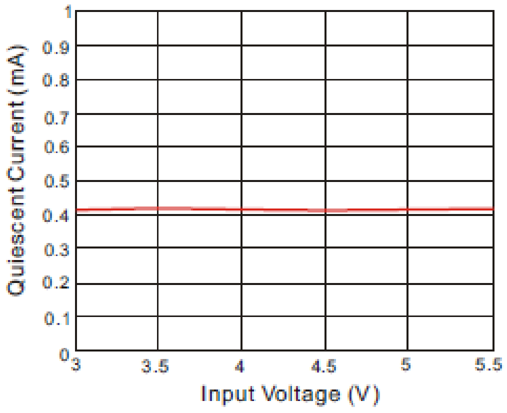
Note 4: Defined as the input to output differential at which the output voltage drops to 2% below the value measured at a differential of 0.8V.

Note 5: Guaranteed by design.

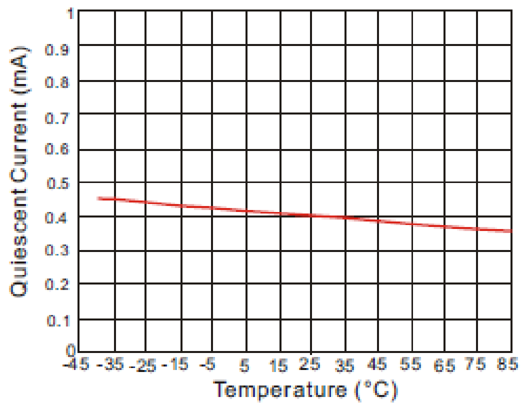
Note 6: Required to maintain regulation. Voltage set resistors R1 and R2 are usually utilized to meet this requirement.

TYPICAL OPERATING CHARACTERISTICS

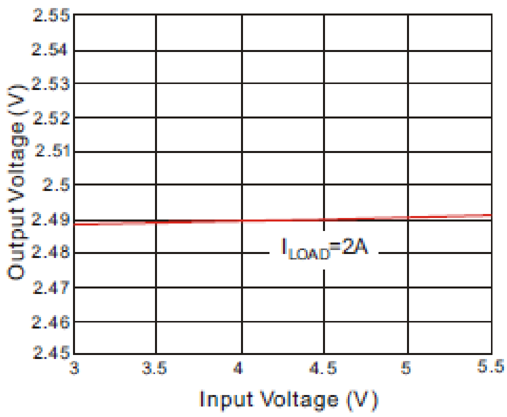
(1) Quiescent Current vs. Input Voltage



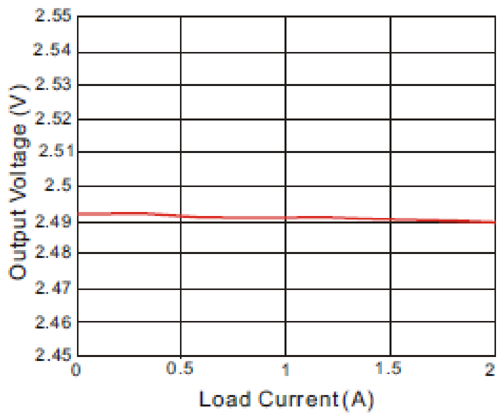
(2) Quiescent Current vs. Temperature



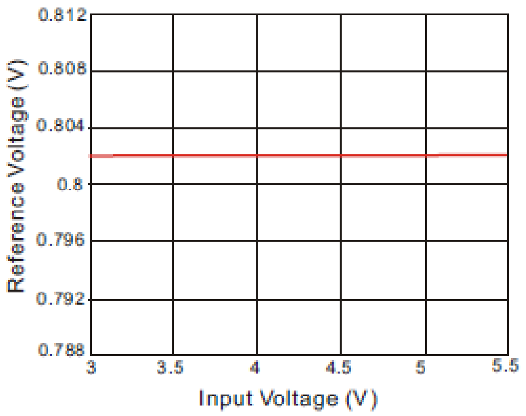
(3) Output Voltage vs. Input Voltage



(4) Output Voltage vs. Load Current



(5) Reference Voltage vs. Input Voltage



APPLICATION INFORMATION

Introduction

The AT1818 is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little PCB real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

Component Selection

Input capacitor : A minimum of 10μF ceramic ca-pacitor is recommended to be placed directly next to the V_{IN} pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally,bulk capacitance of about 100μF may be added closely to the input supply pin of the AT1818 to ensure that V_{IN} does not sag, improves load transient response.

Output Capacitor : A minimum bulk capacitance of 10μF, along with a 0.1μF ceramic decoupling ca-pacitor is recommended. Increasing the bulk ca-pacitance will improve the overall transient re-sponse.

The use of multiple lower value ceramic ca-pacitors in parallel to achieve the desired bulk ca-pacitance will not cause stability issues. Although designed for use with ceramic output capacitors , and thus will also work comfortably with tantalum output capacitors.

External Voltage Selection Resistors : The use of 1% resistors, and consider for system stability and power losing , we recommend to design high dividing resistance (R1>100K) to strengthen the benefits which AT1818 has inherent .

Noise Immunity : In very electrically noisy environments,it is recommended that 0.1μF ceramic capacitors be placed from V_{IN} to GND and V_{OUT} to GND as close to the device pins as possible.

Parallel a small cap (ex:100p) would be recomme-ndedto improve the transient response.

Thermal Considerations

The power dissipation in the AT1818 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (V_{IN} - V_{OUT})*I_{LOAD}$$

The absolute worst-case dissipation is given by:

$$P_{D(MAX)} = (V_{IN(MAX)}-V_{OUT(MIN)})xI_{LOAD(MAX)}+V_{IN(MAX)}xI_{G(MAX)}$$

For a typical scenario, V_{IN}=3.3V±5%, V_{OUT}=2.5V and I_{LOAD}=1.5A, therefore:

$V_{IN(MAX)}$ =3.465V,$V_{OUT(MIN)}$=2.45V and $I_{G(MAX)}$=1.45mA,

Thus $P_{D(MAX)}$ =1.53W.

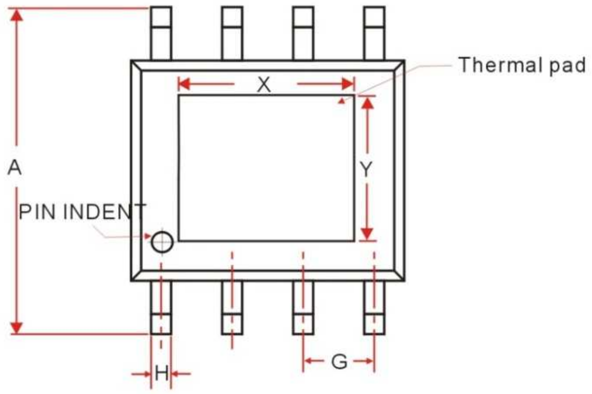
Using this formula, and assuming $T_{A(MAX)}$=85℃ , we can calculate the maximum thermal impedance allowable to maintain $T_J \leq 125℃$:

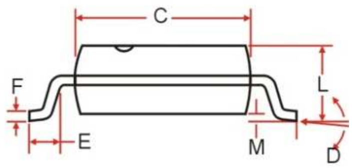
$$R_{\Theta(J-A)(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(125-85)}{1.53} = 26.2°C/W$$

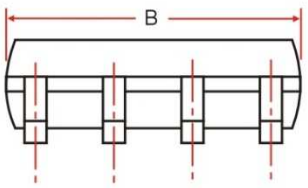
The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad.

PACKAGE OUTLINE DIMENSIONS

PSOP-8 PACKAGE OUTLINE DIMENSIONS

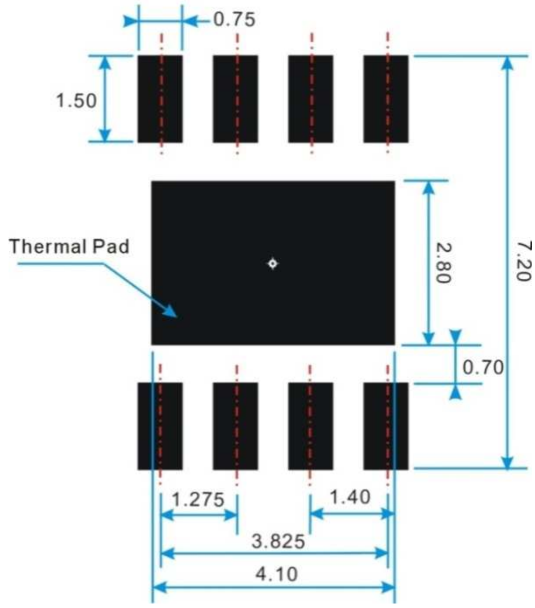






REF.	DIMENSIONS Millimeters	
	Min.	Max.
A	5.79	6.20
B	4.80	5.00
C	3.80	4.00
D	0°	8°
E	0.40	1.27
F	0.15	0.26
M	0	0.25
H	0.31	0.51
L	1.30	1.75
G	1.27 TYP.	
X	3.30 TYP.	
Y	2.50 TYP.	

PSOP-8 PACKAGE FOOTPRINT (mm)



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