Atelic Systems, Inc.

AT2008 Application Note *Preliminary*
8 Channels ADPCM Processor
Version 1.0 January 29, 2001

Description

The AT2008 is an eight full-duplex channels ADPCM processor. It follows the G.726 ITU Standard for ADPCM compression for 40k, 32k, 24k and 16k bit rates with selectable μ-law and A-law input/output. This chip can operate on 16 channels of PCM to ADPCM compression, 16 channels of ADPCM to PCM decompression, 8 channels of full-duplex operation in an 8KHz frame basis, or any combination of M-channels of compression plus N-channels of decompression when M+N <= 16. Using the 3-wire command serial port, each individual half-channel can be dynamically configured to perform the ADPCM algorithm at different bit rates, idle or reset of the algorithm. It can also be programmed to set up different input/output time slots, or to select, (1) bypass without compression, (2) idle, or (3) reset of the algorithm.

Features

- 8 full channels of ITU G.726 ADPCM
- ADPCM coding and decoding with bypass mode
- Per channel selectable μ-Law and A-law input/output
- Up to 8 synchronous signals for direct interface with popular combo/codec.
- On-chip time slot assignment
- Available internal clock generator and frame sync. generator
- Simple 3-wire serial command port for chip configuration
- On-chip power-up/power down/reset
- The two clock pins (CLKA and CLKP) used as PCM/ADPCM data clocks, and the FSY pin used for Frame Sync signals can be programmed to become either as input pins or as output pins. (The defaults are as input pins).

Applications

- DECT
- VoIP / VoDSL
- Wireless PBX systems

Default Settings

3-wire serial command is required to configure the chip running ADPCM in 8 full channels.

PIN Description

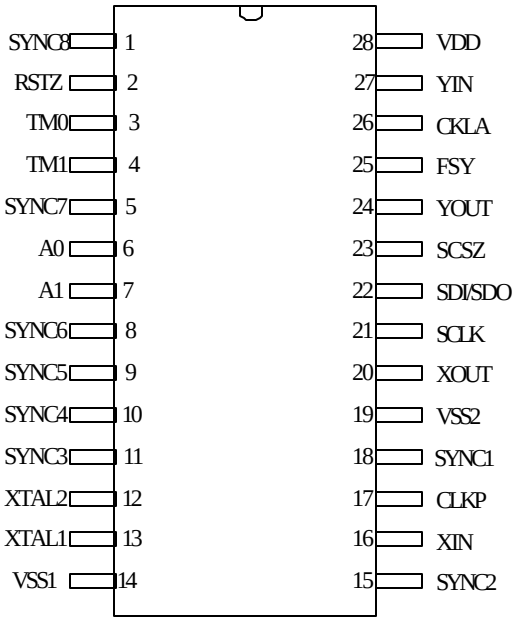
PIN	SYMBOL	TYPE	DESCRIPTION
16	XIN	I	**X Channel Data In**. Sampled on the falling edge of CLKP during selected time slots with MSB first.
20	XOUT	O	**X Channel Data Out**. Updated on the rising edge of CLKP during selected time slots with MSB first.
27	YIN	I	**Y Channel Data In**. Sampled on the falling edge of CLKA during selected time slots with MSB first.
25	FSY	I/O	**Y Channel Frame Sync**. Master Y Channel Frame Sync. Signal followed by the first time slot of transmission. It can be either input or output by initial setup sequence.
24	YOUT	O	**Y Channel Data Out**. Updated on the rising edge of CLKA during selected time slots with MSB first.
2	RSTZ	I	**Reset**. Low active signal to force chip reset.
13 12	XTAL1/MCLK XTAL2	I O	**Crystal In & Out**. 14.318 MHz Crystal connected***.
17	CLKP	I/O	**PCM Clock**. It can be either input created by external control circuit, or output generated by internal control circuit.
26	CLKA	I/O	**ADPCM Clock**. It can be either input created by external control circuit, or output generated by internal control circuit.
18 15 11 10 9 8 5 1	SYNC1 SYNC2 SYNC3 SYNC4 SYNC5 SYNC6 SYNC7 SYNC8	O O O O O O O O	**Sync 1**. Frame sync. for 1st CODEC. **Sync 2**. Frame sync. for 2nd CODEC. **Sync 3**. Frame sync. for 3rd CODEC. **Sync 4**. Frame sync. for 4th CODEC. **Sync 5**. Frame sync. for 5th CODEC. **Sync 6**. Frame sync. for 6th CODEC. **Sync 7**. Frame sync. for 7th CODEC. **Sync 8**. Frame sync. for 8th CODEC.
4 3	TM1 TM0	I I	**TM1 &TM0**. Tie to Ground for normal operation.
7 6	A1 A0	I I	**A1 & A0**. Address ID key for 3-wire serial port. If match, 3-wire serial port can be enabled for configuration.
22	SDI/SDO	I/O	**Serial Data In**. Data for configuration on the fly by 3-wire serial port. Sampled on the rising edge of SCLK with LSB first. **Serial Data Out**. Output data after sending Read Memory command by 3-wire serial port. Sampled on the rising edge of SCLK with LSB first.
21	SCLK	I	**Serial Clock**. Used to write to the 3-wire serial port registers or output data from 3-wire serial port registers.
23	SCSZ	I	**Serial Port Chip Select**. Low active to enable 3-wire serial port.
28	VDD	-	**Power**. 3.3 Volts.
14 19	Vss1 Vss2	- -	**Ground**. 0 Volt.

***For clock source other than 14.318MHz, please contact Atelic Systems.

AT2008 PIN Assignment

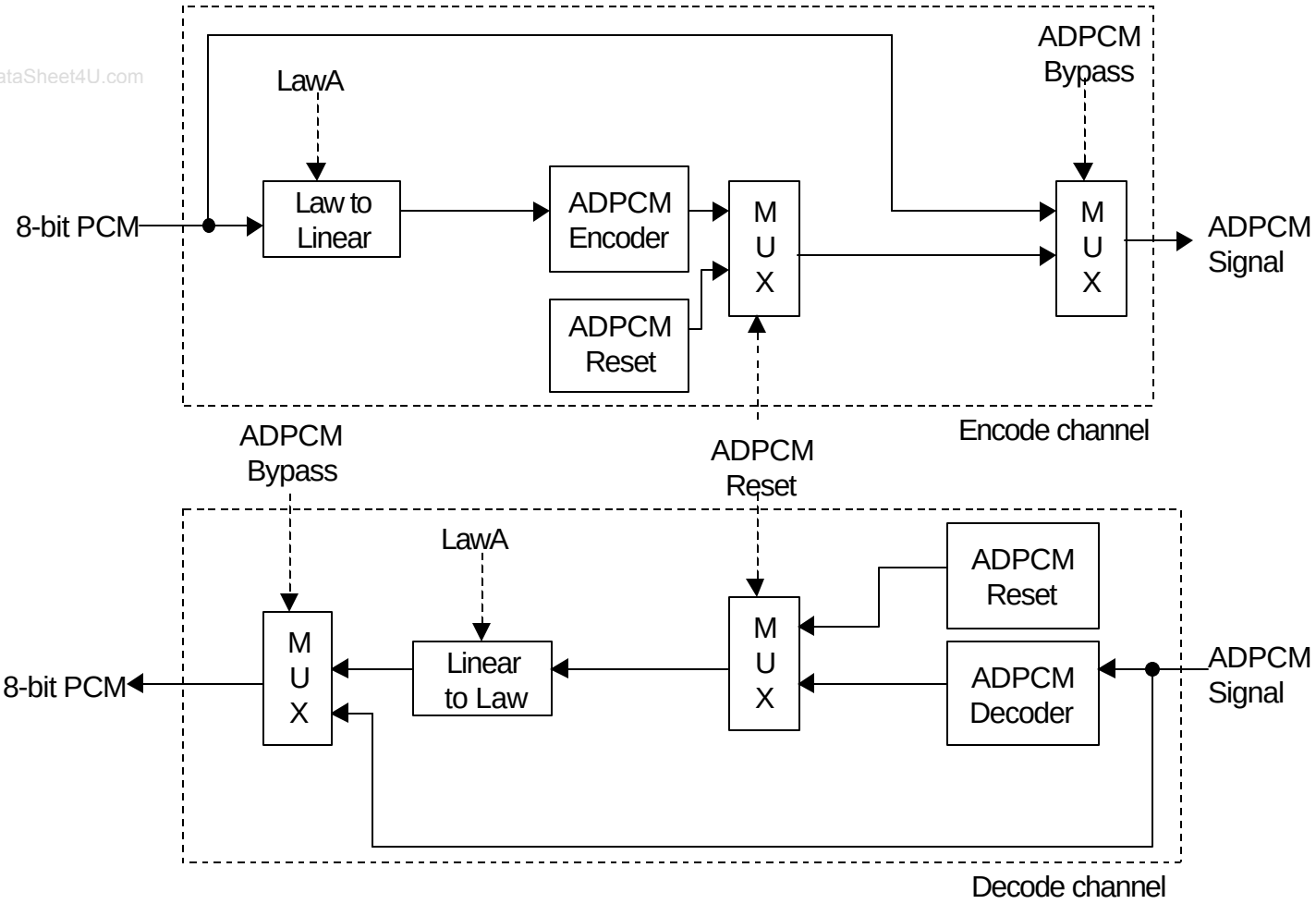
AT2008 SOP Pin Assignment

28-PIN SOP



1. When there are multiple AT2008 used on the same system, A1, A0 are used to identify the chip.
2. A1, A0 are for chip ID. Values are from 00 to 03. They should be connected to microcontroller I/O line or hard wired to either VCC or ground.

AT2008 Block Diagram



Note:

- A dotted line with arrow mark indicate the control bit in the per channel control command, such as LawA, ADPCM bypass and ADPCM reset. Please refer to page 9 for detail information.
- Only two half channel is shown above. AT2008 has additional capability to process up to 16 half channels simultaneously.

Power

The AT2008 is powered by a 3.3 V source and draws 100 mA at full operation and < 1 mA in powerdown mode.

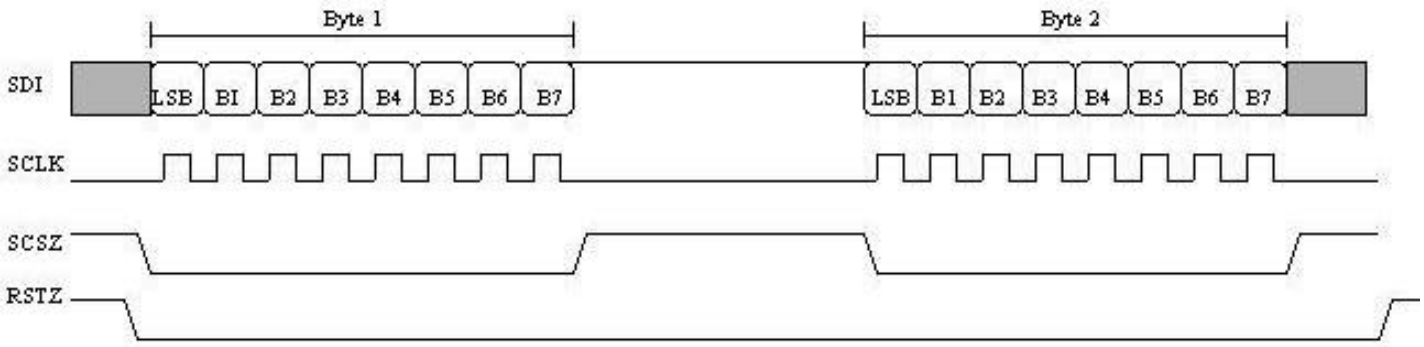
Initialization

There are two different classes of resets available on the AT2008 chip. For the default reset, hold the RSTZ pin low for 50 ms. This reset will bring the chip to a functioning default state. In the default state, the following parameters are set:

1. Pins FSY, CLKP, CLKA default to input (chip will receive these signals from external source)
2. 4 half channels of 32k μ-law ADPCM decoder running on half channels 0-3
3. 4 half channels of 32k μ -law ADPCM encoder running on half channels 4-7

A second type of reset involving the use of the 3-wire serial interface can also be used direct the pin I/O configurations of FSY, CLKP, and CLKA during reset.

AT2008 PIN I/O Configurations



Pattern:

MSB	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB
1	0	1	0	0	1	0	1

First Byte Write

MSB	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB
0	0	p5	p4	p3	p2	0	0

Second Byte Write

p2 – CLKP's setting: "0" as input; "1" as output
p3 – CLKA's setting: "0" as input; "1" as output
p4 – FSX's setting: "0" as input; "1" as output
p5 – FSY's setting: "0" as input; "1" as output

Configuration Access: Write 2 bytes during RESET active. First byte MUST be 0xA5 as the key to enter PIN I/O configuration mode, otherwise the setting doesn't change.

Chip ID Setup

The two Chip ID pins A0 and A1 (Pins 6,7) should also be set during chip initialization. The "Chip ID" is used to differentiate between AT2008 chips in a system that uses more than one AT2008 chip. When using only one chip, it is recommended to tie A0 and A1 to digital zero. Thus, when programming the AT2008 chip, you can use the Chip ID = '00' to substitute wherever you see A1, A0.

The maximum number of AT2008 can be used in a system is 4, and a chip ID must be assigned to each AT2008 in a system. The format of A0 and A1 should be specified according to the following table:

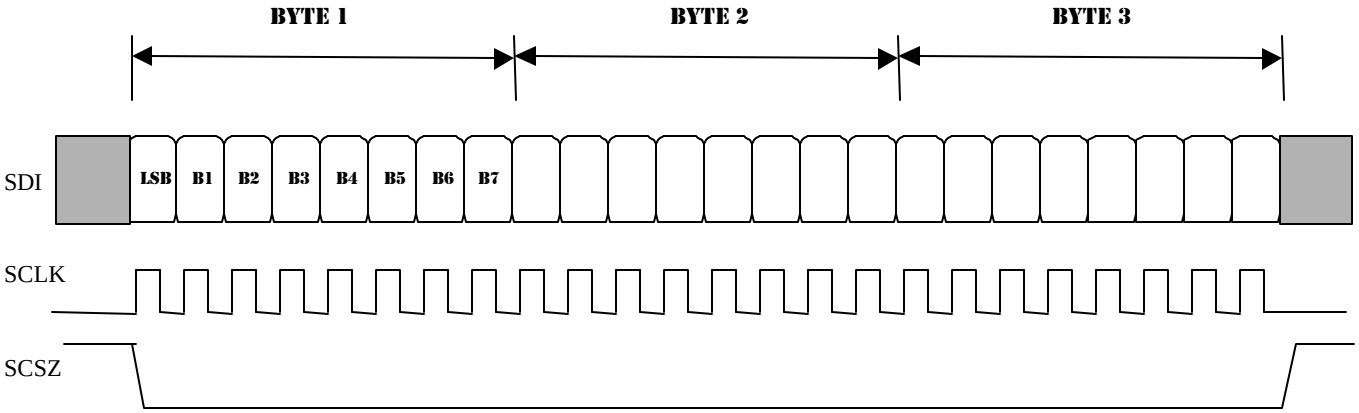
A1	A0	Description
0	0	AT2008 chip ID=0
0	1	AT2008 chip ID=1
1	0	AT2008 chip ID=2
1	1	AT2008 chip ID=3

Programming the AT2008

Using the Serial Port to Input Commands

Commands for the AT2008 are entered using the 3-wire Serial Interface. The "three wires" refer to the three pins which control the interface: SDI/SDO (Serial Data In/Serial Data Out), SCLK (Serial Clock), and SCSZ (Serial Chip Select). When SCSZ is enabled (low), the SDI is sampled every SCLK signal. Sampled bits are collected into an 8-bit register and read by the DSP. The SCSZ signal can be held more than 8-bits at a time in 8-bit multiples forming a COMMAND SEQUENCE. Different command sequences form the bulk of AT2008 programming.

Generic 3-byte Command Sequence



Command Sequence Overview

The AT2008 understands four different types of command sequences.

1. The PLL command sequences sets the operating speed of the chip.
2. The MCU7byte command sequence set the ADPCM algorithms, bit-slots, bit-rate and encode or decode channel.
3. The Per Channel Control command sequence sets the ADPCM bypass, reset and Law format.
4. Chip Power-up and Power-down commands.

PLL Command Sequence

The PLL Command Sequence is a 3-byte command sequence that sets the operating speed of the AT2008 to be a multiple of the input crystal Mhz.

Format of PLL Command Sequence								
Byte 1	0	1	F3	F2	F1	F0	A1	A0
Byte 2	N6	N5	N4	N3	N2	N1	N0	M5
Byte 3	M4	M3	M2	M1	M0	P2	P1	P0

A[1:0] refers to the chip ID (please refer to section talking about chip ID)
N[6:0] = n, binary number used for frequency multiplier
M[5:0] = m, binary number used for frequency divider
P[2:0] = table specialized frequency divider (please refer to table).
F[3:0] = Divider for CLKP & CLKA Generator. f(CLKA/CLKP) = f(XTAL) / F[3:0]

Table for P, frequency multiplier	
P = 0	Bypass, PLLclk = XTALclk regardless of N, M.
P = 1	16
P = 2	8
P = 3	4
P = 4	2
P = 5	1
P = 6	No PLLclk, PLLclk = 0 Hz (chip disabled!)
P = 7	No PLLclk, PLLclk = 0 Hz (chip disabled!)

The system clock uses **N**, **M**, and **P** to determine the speed of the system clock using the following formula:
System Clock = (Crystal_clk * N * 4) / (M * P)

By default, the chip is set to run at 86 Mhz using a 14.3 Mhz crystal input.

MCU7byte Command Sequence

This command sequence allows the user to specify the ADPCM algorithm, I/O bit-slots. The command sequence length is variable, and is dependent on the number of channels that are specified. The command sequence consists of a header byte, a data portion consisting of 7 bytes for every channel specified, and a footer byte. The total number of bytes in the command sequence will be 2+7N where N = number of half channels specified.

The channels should be sorted by the user in increasing order of 'Input Begin Bit'. All the YIN channels should be placed in sorted order before all the XIN channels.

Below is a sample of MCU7byte command sequence for two 'half channels'.

	Command Byte [7:0]								Description
	0	0	0	0	0	0	A1	A0	Chip Setup Command Header with A1, A0 chip ID
Chan 0 Data	In/Out		0	ADPCM_ind	0	0	0	0	Specify channel In/Out source and ADPCM indicator.
	0	Dec	0	1	1	1	Rate		ADPCM, configuration command for Channel #0
	0	0	0	0	0	0	0	0	System reserved
	Input Begin Bit								These commands specify the begin and ending bits of input data and output data for channel #0
	Input End Bit								
	Output Begin Bit								
	Output End Bit								
Chan 1 Data	In/Out		0	ADPCM_ind	0	0	0	0	Specify channel In/Out source and ADPCM indicator
	0	Dec	0	1	1	1	Rate		ADPCM, configuration command for Channel #1
	0	0	0	0	0	0	0	0	System reserved
	Input Begin Bit								These commands specify the begin and ending bits of input data and output data for channel #1
	Input End Bit								
	Output Begin Bit								
	Output End Bit								
	1	1	1	1	1	1	1	1	Footer of Chip Setup.

Note: The format of data fields In/Out, ADPCM_ind, Dec and Rate are specified below.

In/Out		Description
0	0	Input on Xin, Output on Xout
0	1	Input on Xin, Output on Yout
1	0	Input on Yin, Output on Xout
1	1	Input on Yin, Output on Yout

Default: Input is on Xin, Output is on Xout for ADPCM encoding functions.
Input is on Yin, Output is on Yout for ADPCM decoding functions.

ADPCM_ind	Description
0	No resource is allocated for ADPCM operation
1	Allocate resource for ADPCM operation

Default: 1, allocate resource for ADPCM operation

Dec	Description
0	ADPCM (Input is PCM, Output is ADPCM) encode channel
1	ADPCM (Input is ADPCM, Output is PCM) decode channel

Default: 1 for channel 0, 1, 2, 3;
0 for channel 4, 5, 6, 7.

Rate		Description
0	0	16k ADPCM bitrate
0	1	24k ADPCM bitrate
1	0	32k ADPCM bitrate
1	1	40k ADPCM bitrate

Default: 10 for 32k ADPCM bit-rate

Per Channel Control Command Sequence

The Per Channel Control command sequence allows the user to specify some parameters for each half channel. The command sequence length is variable, and is dependent on the number of channels that are specified. The format of the command consists of a header, a begin channel number byte, and a data portion containing information of each channel. The total number of bytes in the command sequence will be 2+2N where N = number of half channels specified.

Below is a sample of Per Channel Control command sequence for two half channels.

		Command Byte [7:0]								Description
		0	0	1	1	0	0	A1	A0	Per Channel Control command Header with A1, A0 chip ID
		Channel Configuration Begin								To begin on first channel, set to 0
Ch0	High Byte	0	0	0	0	0	0	0	0	Configuration for channel 0
	Low Byte	0	0	0	ADPCM Reset	ADPCM Bypass	LawA	0	Idle	
Ch1	High Byte	0	0	0	0	0	0	0	0	Configuration for channel 1
	Low Byte	0	0	0	ADPCM Reset	ADPCM Bypass	LawA	0	Idle	

Note: The format of each data fields like ADPCM reset, ADPCM bypass, lawA, lawP and idle are specified below.

ADPCM reset	Description
0	Normal operation without reset of ADPCM
1	Reset ADPCM internal states

Default: 1

When ADPCM reset bit is '1', ADPCM encoder will output "ff", ADPCM decoder will output "ff" for u-law and "d5 " for A-law.

ADPCM bypass	Description
0	Normal operation with ADPCM
1	Bypass ADPCM

Default: 0

LawA	Description
0	u-law
1	A-law

Default: 0

Idle	Description
0	Normal operation
1	The output is tri-state during its time slot. Once this bit is cleared, it will come back to normal operation

Default: 0

Chip Power-up Power-down command

The chip power-up / power-down command is a single command byte which enables and disables the AT2008 chip.

Power-up chip mode will:

1. Stop the sample processing
2. Power-up the PLL to the specified multiplier frequency
3. Reset algorithms on the chip.

Power-down chip mode will:

1. Stop the sample processing.
2. Switch the system clock to the power down clock running approximately at 125 Hz.

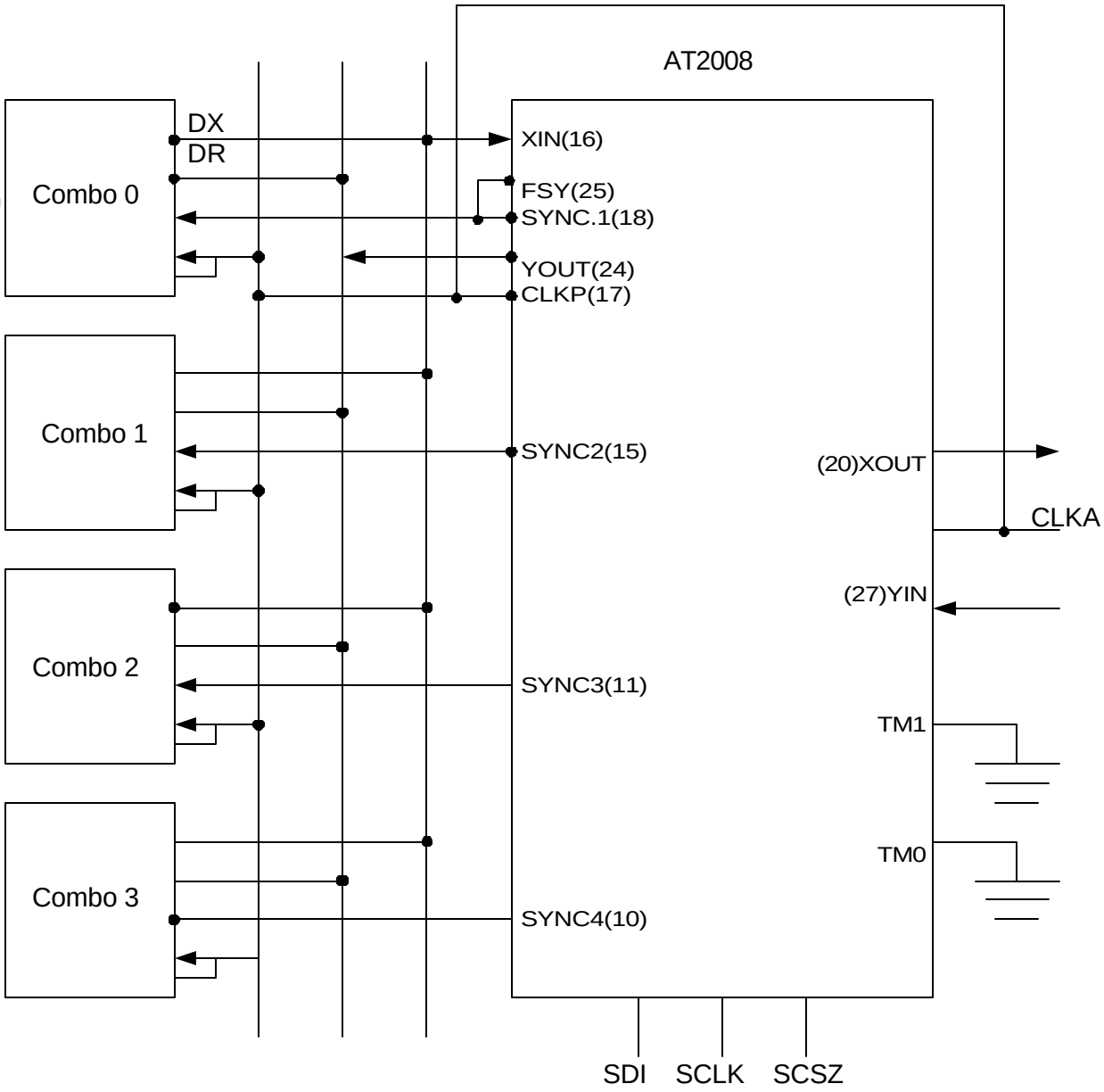
0	0	0	1	0	0	A1	A0	Power-up Chip Command

0	0	0	0	1	0	A1	A0	Power-down Chip Command

Note: A1, A0 refers to the chip ID.

Reference Designs and Additional Notes

Using the AT2008 with other combo chips



Note:
SDI, SCLK, SCSZ are for 3-wire commands and should be connected to microcontroller I/O pins.
CLKA and FSY.
Typical application of default setting uses National single channel Combo (Quad Combo can be used to replace the 4 single Combo)

When there are multiple AT2008 used on the same systems, A1, A0 are used to identify the chip.
A1, A0 are for chip ID. Values are from 00-03. They should be connected to microcontroller I/O lines or wired to either VCC or ground.

Sample Command Sequences:

ADPCM 32k, m-Law, 8-half channels:

For convenience, each half duplex channel is assigned a number corresponding to the internal processing order of the channels. Channels 0 through Channel 3 correspond with ADPCM decode channels and Channels 4 through Channel 7 corresponds with ADPCM encode channels.

The following is brief description of what each half duplex channel is running:

Channel 0: (decode ADPCM channel)
MCU7byte Command:

- Decode (i.e. input is ADPCM sample sequence)
- u-Law output, 32k ADPCM algorithm.
- Input time slot: @yin[0:3] (beginning bit=0, ending bit=3)
- Output time slot: @yout[0:7] (beginning bit=0, ending bit=7)

Channel 1: (decode ADPCM channel)
MCU7byte Command:

- Decode
- u-Law output, 32k ADPCM algorithm.
- Input time slot: @yin[16:19]
- Output time slot: @yout[16:23]

Channel 2: (decode ADPCM channel)
MCU7byte Command:

- Decode
- u-Law output, 32k ADPCM algorithm.
- Input time slot: @yin[32:35]
- Output time slot: @yout[32:39]

Channel 3: (decode ADPCM channel)
MCU7byte Command:

- Decode
- u-Law output, 32k ADPCM algorithm.
- Input time slot: @yin[48:51]
- Output time slot: @yout[48:55]

Channel 4: (encode ADPCM channel)
MCU7byte Command:

- Encode (i.e. output is ADPCM sample sequence)
- u-Law input, 32k ADPCM algorithm.
- Input time slot: @xin[0:7]
- Output time slot: @xout[0:3]

Channel 5: (encode ADPCM channel)
MCU7byte Command:

- Encode (i.e. output is ADPCM sample sequence)
- u-Law input, 32k ADPCM algorithm.
- Input time slot: @xin[16:23]
- Output time slot: @xout[16:19]

Channel 6: (encode ADPCM channel)
MCU7byte Command:

- Encode (i.e. output is ADPCM sample sequence)

- u-Law input, 32k ADPCM algorithm.
- Input time slot: @xin[32:39]
- Output time slot: @xout[32:35]

Channel 7: (encode ADPCM channel)
MCU7byte Command:

- Encode (i.e. output is ADPCM sample sequence)
- u-Law input, 32k ADPCM algorithm.
- Input time slot: @xin[48:55]
- Output time slot: @xout[48:51]

The following is command sequences of per channel control and mcu7byte:

Command bytes specifying per channel control

```
30   // Begin per channel control.  This byte is fixed.
00   // begin at 0 channel.  This byte is usually fixed (usually begin specifying at 0).
00   // 0 channel high byte.
00   // 0 channel low byte.
00   // 1 channel high byte.
00   // 1 channel low byte.
00   // 2 channel high byte.
00   // 2 channel low byte.
00   // 3 channel high byte.
00   // 3 channel low byte.
00   // 4 channel high byte.
00   // 4 channel low byte.
00   // 5 channel high byte.
00   // 5 channel low byte.
00   // 6 channel high byte.
00   // 6 channel low byte.
00   // 7 channel high byte.
00   // 7 channel low byte.
```

Command bytes specifying mcu7byte definition.

```
00   // begin mcu7byte definition.
D0   // [7]: input; [6]:output; 0==X; 1==Y, channel 0, yin-yout
5E   // Algorithm Setup, default value = 5EH for expand
00   //
00   // Begin input slot bit, ADPCM
03   // End input slot bit, ADPCM
00   // Begin output slot bit, PCM
07   // End output slot bit, PCM
D0   // [7]: input; [6]:output; 0==X; 1==Y, channel 1, yin-yout
5E   // Algorithm Setup, default value = 5EH for expand
00   //
10   // Begin input slot bit, ADPCM
13   // End input slot bit, ADPCM
10   // Begin output slot bit, PCM
17   // End output slot bit, PCM
D0   // [7]: input; [6]:output; 0==X; 1==Y, channel 2, yin-yout
```



```
5E    // Algorithm Setup, default value = 5EH for expand
00    //
20    // Begin input slot bit, ADPCM
23    // End input slot bit, ADPCM
20    // Begin output slot bit, PCM
27    // End output slot bit, PCM
D0    // [7]: input; [6]:output; 0==X; 1==Y, channel 3, yin-yout
5E    // Algorithm Setup, default value = 5EH for expand
00    //
30    // Begin input slot bit, ADPCM
33    // End input slot bit, ADPCM
30    // Begin output slot bit, PCM
37    // End output slot bit, PCM
10    // [7]: input; [6]:output; 0==X; 1==Y, channel 4, xin-xout
1E    // Algorithm Setup, default value = 1EH for compress
00    //
00    // Begin input slot bit, PCM
07    // End input slot bit, PCM
00    // Begin output slot bit, ADPCM
03    // End output slot bit, ADPCM
10    // [7]: input; [6]:output; 0==X; 1==Y, channel 5, xin-xout
1E    // Algorithm Setup, default value = 1EH for compress
00    //
10    // Begin input slot bit, PCM
17    // End input slot bit, PCM
10    // Begin output slot bit, ADPCM
13    // End output slot bit, ADPCM
32    // [7]: input; [6]:output; 0==X; 1==Y, channel 6, xin-xout
1E    // Algorithm Setup, default value = 1EH for compress
00    //
20    // Begin input slot bit, PCM
27    // End input slot bit, PCM
20    // Begin output slot bit, ADPCM
23    // End output slot bit, ADPCM
10    // [7]: input; [6]:output; 0==X; 1==Y, channel 7, xin-xout
1E    // Algorithm Setup, default value = 1EH for compress
00    //
30    // Begin input slot bit, PCM
37    // End input slot bit, PCM
30    // Begin output slot bit, ADPCM
33    // End output slot bit, ADPCM
FF    // End of mcu7byte commands
```


Electrical Characteristics:

(0°C to 70°C)

DC Electrical Characteristics (V_{DD}=3.3V+20%-10%)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Active Supply Current	Ivcc		40		mA	1,2
Power down	I_{VCCPD}		< 1		mA	3
Input Leakage	I_I	-1.0		+1.0	µA	
Output Leakage	I_O	-1.0		+1.0	µA	4
Output Current (2.4V)	I_{OH}		1.2		mA	
Output Current (0.4 v)	I_{OL}		4		mA	

Notes:
1. CLKP = CLKA = 2.048MHz; MCLK = 10MHz.
2. Outputs open; inputs swinging full supply levels; 8 channel full duplex operation.
3. Power down; Xtal = high; fsx, fsy, CLKA, CLKP all 0.
4. Xout and Yout are 3-stated.

PCM Interface (0°C to 70°C)

AC Electrical Characteristics (V_{DD}=3.3V+20%-10%)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
CLKP, CLKA Period	t_{PXY}	244		3906	ns	1
CLKP, CLKA Pulse Width	t_{WXYL} t_{WXYH}	100			ns	
CLKP, CLKA Rise Fall Times	t_{RXY} t_{FXY}		10	20	ns	
Hold Time from CLKP, CLKA to FSY	t_{HOLD}	0			ns	2
Setup Time from FSY high to CLKP, CLKA low	t_{SF}	50			ns	2
Setup Time for Xin, Yin to CLKP, CLKA low	t_{SD}	50			ns	2
Hold Time from Xin, Yin to CLKP, CLKA low	t_{HD}	50			ns	2
Delay Time from CLKP, CLKA to Valid Xout, Yout	t_{DXYO}	10		150	ns	3

Notes:
1. Maximum width of FSY is CLKP/CLKA period (except for signaling frame).
2. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.
3. Load = 150 pF + 2LSTTL loads.
4. For LSB of PCM or ADPCM byte.

Master Clock/Reset (0°C to 70°C)
AC Electrical Characteristics (V_{DD}=3.3V+20%-10%)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
MCLK Period	t_{PM}	69.84	100	125	ns	1
MCLK Rise/Fall Times	t_{RM}, t_{FM}			10	ns	
RSTZ Pulse Width	t_{RST}	1			ms	

Note:
1. MCLK = 14MHz or 10MHz.

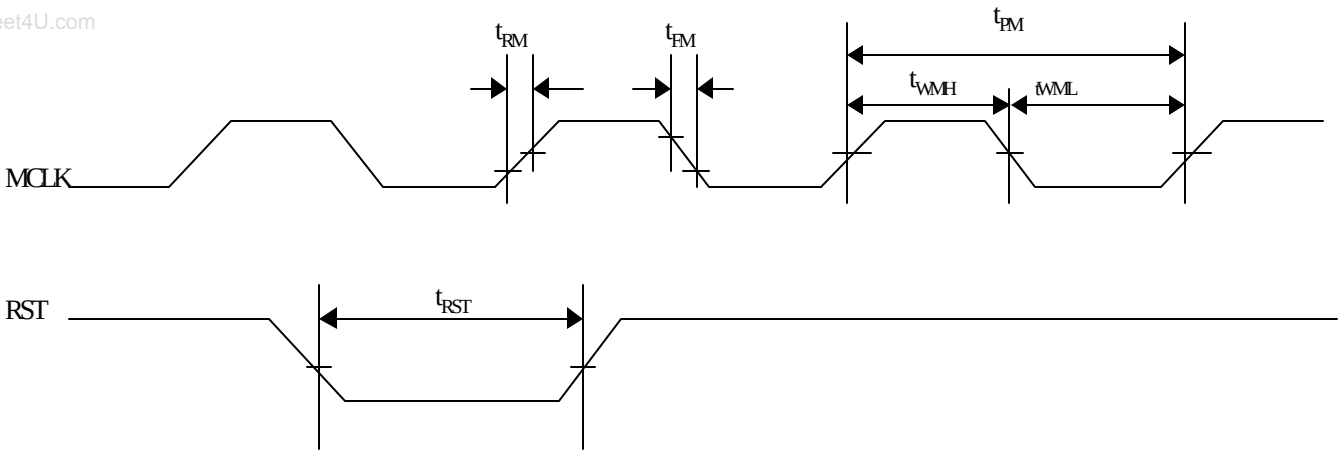
Serial Port (0°C to 70°C)
AC Electrical Characteristics (V_{DD}=3.3V+20%-10%)

Parameter	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK Period	t_P	1			µs	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250	500		ns	1
SCLK High Time	t_{CH}	250	500		ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
SCSZ to SCLK Setup	t_{CC}	50			ns	1
SCLK to SCSZ Hold	t_{CCH}	250			ns	1
SCSZ Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to SCSZ Falling	t_{SCC}	50			ns	1

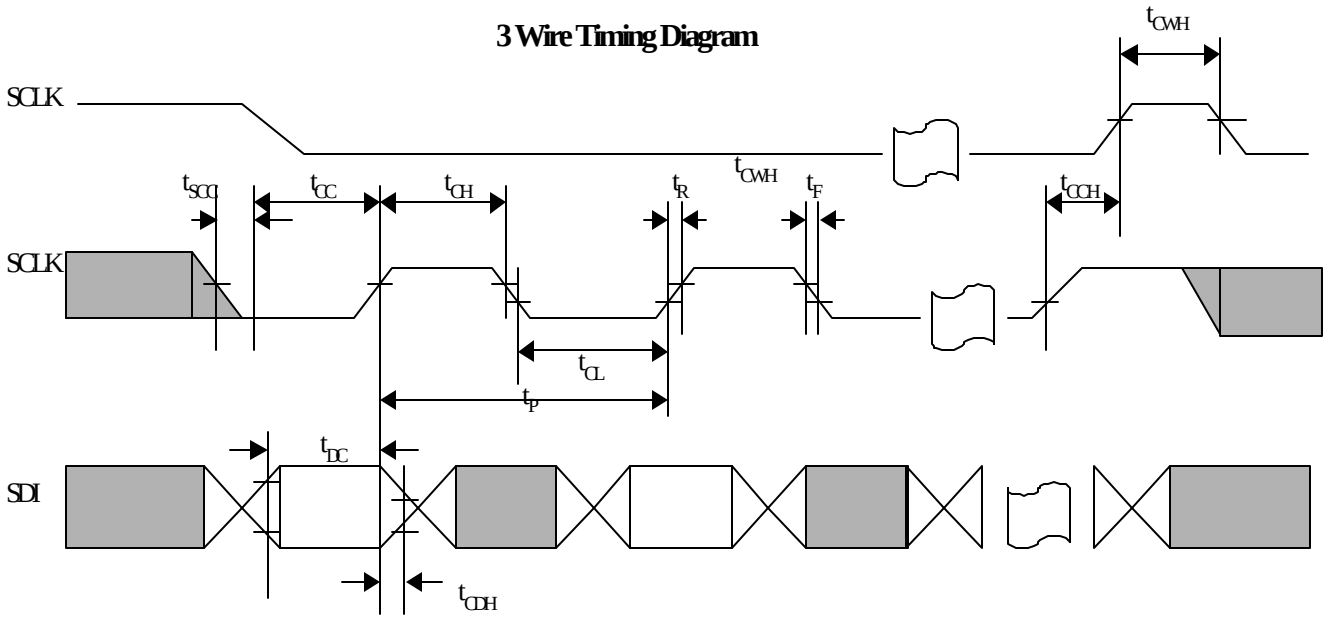
Note:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall time.

Timing Diagrams

Master Clock/Reset AC Timing Diagram

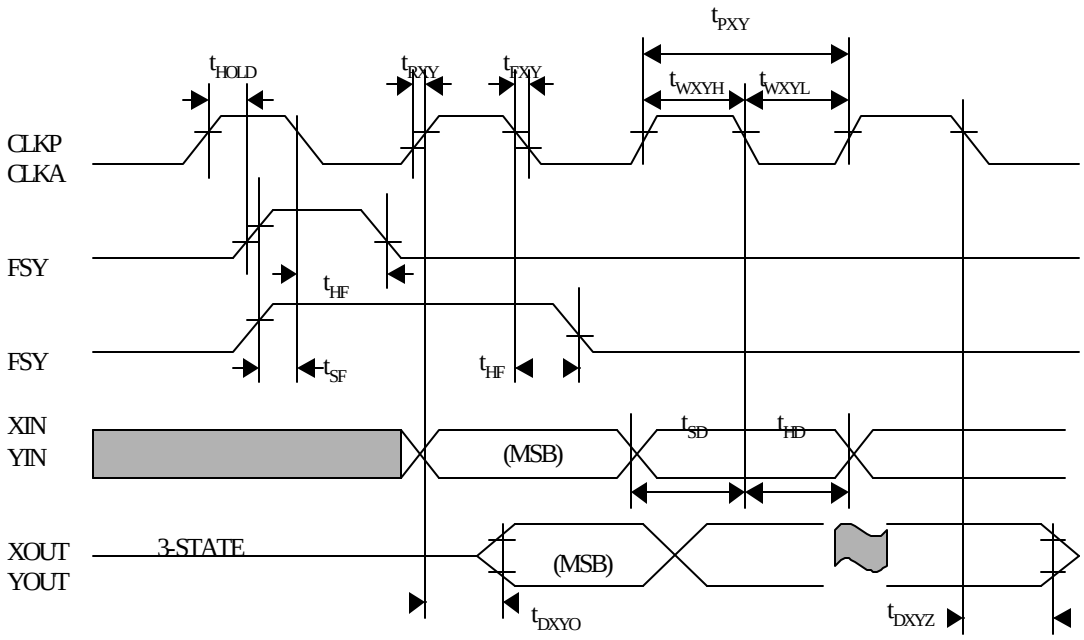


3 Wire Timing Diagram



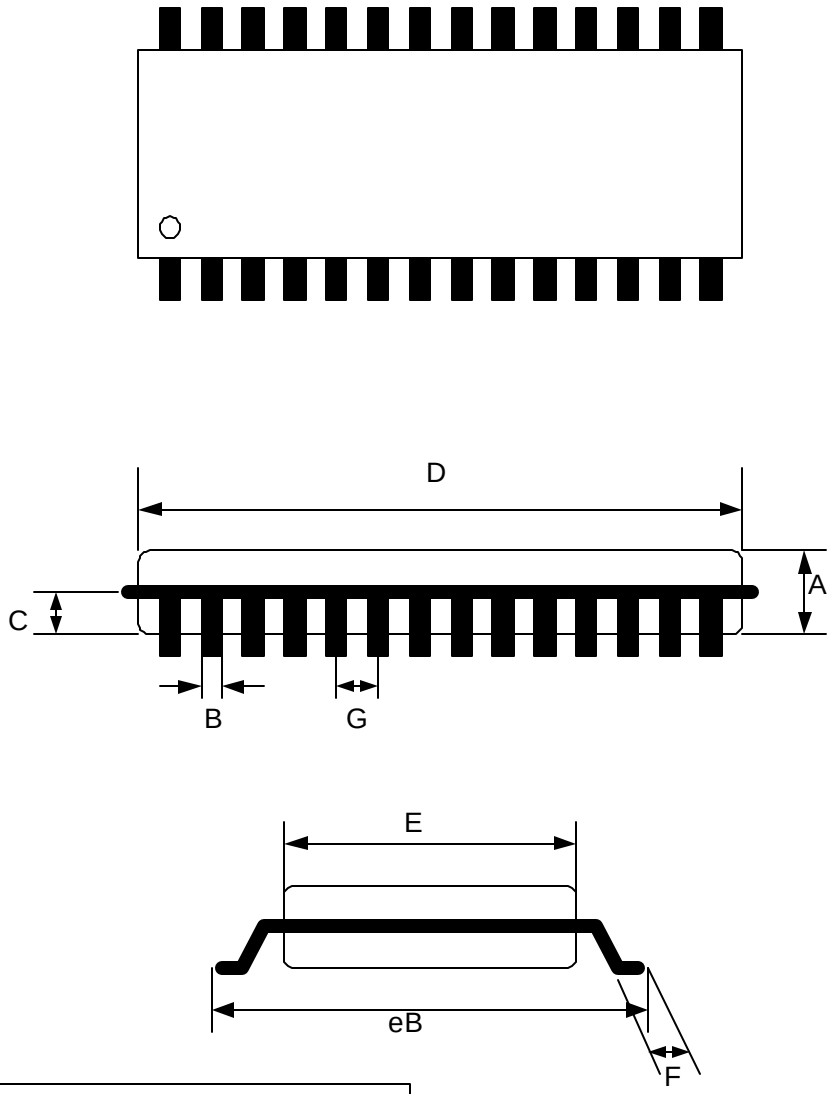
Note: SCLK may be either high or low when SCSZ is taken low.

PCM Interface AC Timing Diagram



Package Information

28 Pin SOP AT2008
Package Information



	Min	Normal	Max
A	2.286	2.337	2.388
B	0.305	0.406	0.508
C	0.991	1.041	1.092
D	17.856	17.907	17.958
E	7.442	7.493	7.544
eB	10.312	10.414	10.516
F	0.635	--	--
G	1.194	1.27	1.346

Dimension in mm.

