AT2721

8-40V,3A Synchronous Buck Converter

Immense Advance Tech.

FEATURES

- Wide 8V to 40V Operating Input Range
- Integrated 140mΩ Power MOSFET Switches
- Output Adjustable from 1V to 25V
- Up to 93% Efficiency
- Internal Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Cycle-by-Cycle Over Current Protection
- Input Under/Over Voltage Lockout
- 3A Output Current

DESCRIPTION

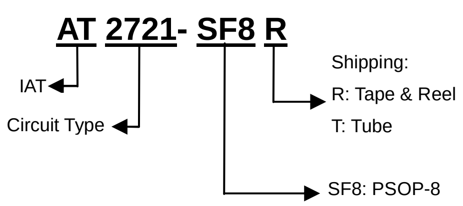
The AT2721 is a monolithic synchronous buck regulator. The device integrates two internal power MOSFETs, and provides 3A of continuous load current over a wide input voltage of 8V to 40V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An internal soft-start prevents inrush current a turn-on, This device, available in PSOP-8 package, provides a very compact solution with minimal external components.

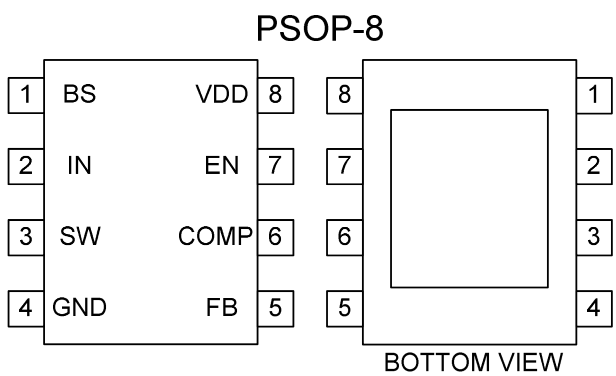
APPLICATION

- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- Battery-Powered Equipment
- PCMCIA V_{CC} and V_{PP} Regulation / Switching
- Consumer / Personal Electronics
- SMPS Post-Regulator / DC-to-DC Modules
- High-Efficiency Linear Power Supplies

ORDER INFORMATION



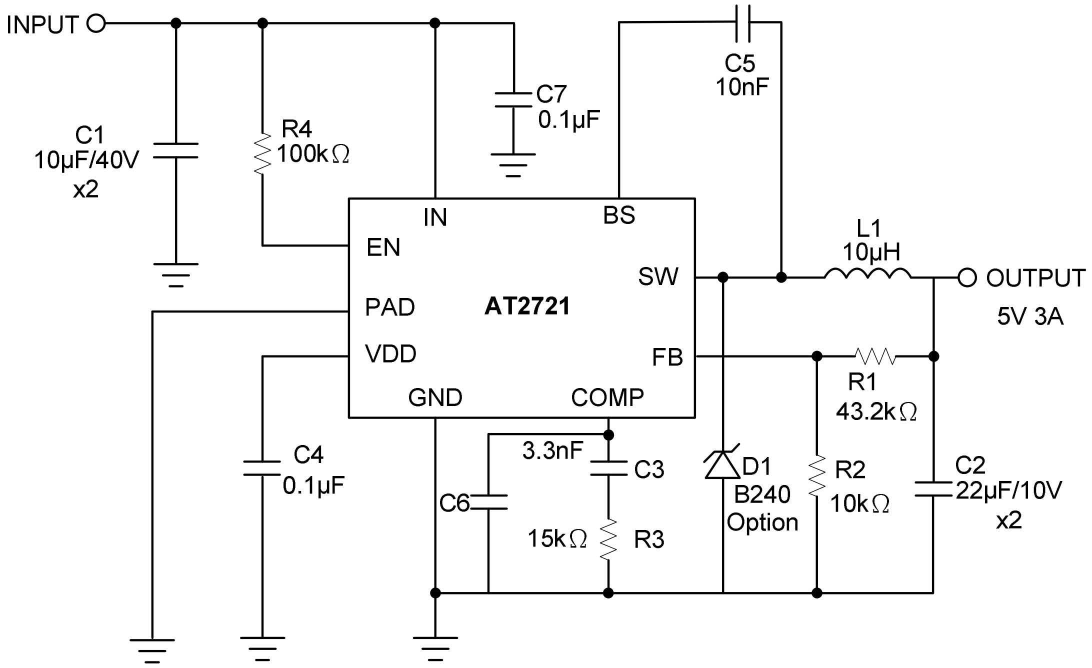
PIN CONFIGURATIONS (TOP VIEW)



PIN DESCRIPTIONS

Pin Name	Pin Description
BS	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to SW pin with 10nF ceramic cap.
IN	Power Input pin. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
GND	Ground.
PAD	Ground (Connect to GND).
FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage.
COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop.
EN	Enable control. Pull high to turn on. Do not let it float.
VDD	Internal regulator pin

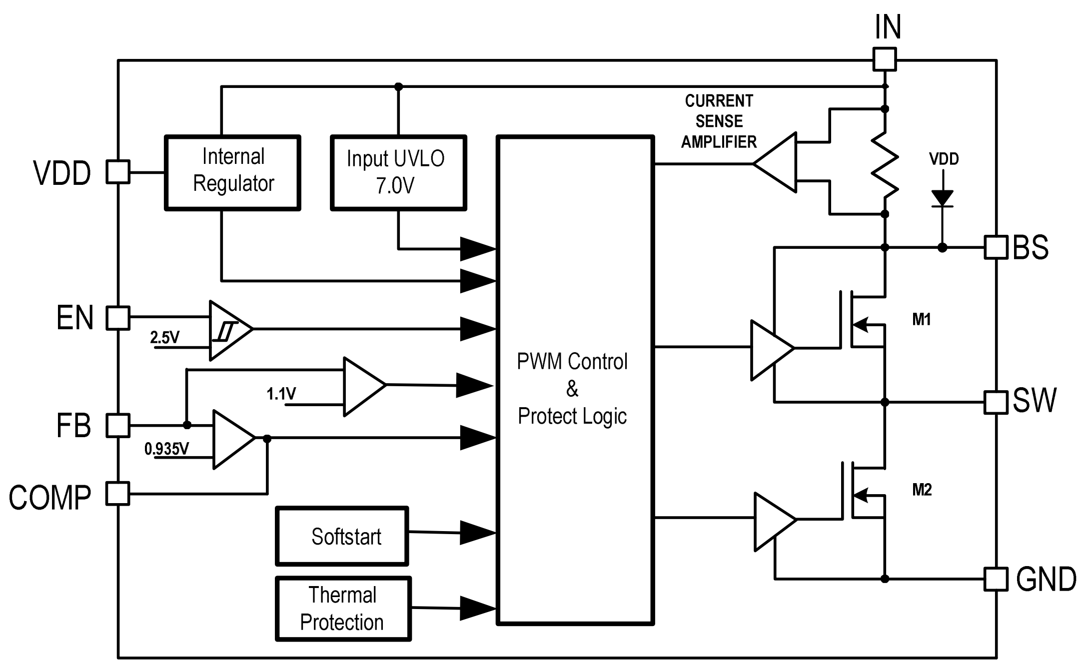
TYPICAL APPLICATION CIRCUITS



$V_{OUT}=V_{FB}\times(1+R1/R2)$, $V_{FB}=0.935V$

V_{OUT}	R1	R2
12V	46.4kΩ	3.9kΩ
5V	43.2K	10K
3.3V	40.2K	15.8K
2.5V	12.7K	7.5K
1.8V	11.3K	12.1K

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Max Value	Unit
Supply Input Voltage	V_{IN}	-0.3 to +41	V
Switch Node Voltage	V_{SW}	-0.3 to V_{IN} +0.3	V
Boost Voltage	V_{BS}	V_{SW} – 0.3 to V_{SW} +5	V
EN Voltage	V_{EN}	-0.3 to +41	V
All Other Pins		–0.3 to +6	V
Maximum Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{STG}	-60 to +150	℃
Lead Temperature(Soldering) 5 Sec.	T_{LEAD}	260	℃
Power DissipationP_D @ T_A=25℃	P_D	2770	mW
Thermal Resistance Junction to Ambient (Note 2)	θ_{JA}	36	℃/W
Thermal Resistance Junction to Case	θ_{JC}	5.5	℃/W
ESD rating (Human body mode) (Note 3)	V_{ESD}	2	kV

RECOMMENDED OPERATING CONDITIONS (Note 4)

Parameter	Symbol	Operation Conditions	Unit
Supply Input Voltage	V_{IN}	8 to 40	V
Output Voltage	Vout	1 to 25	V
Operating Junction Temperature Range	T_J	-40 to +125	℃
Operating Ambient Temperature Range	T_{OPA}	-40 to +85	℃

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: Thermal Resistance is specified with the component mounted on a low effective thermal conductivity test board in free air at T_A=25℃.

Note 3: Devices are ESD sensitive. Handing precaution recommended.

Note 4: The device is not guaranteed to function outside its operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range			8	—	40	V
Shutdown Supply Current	I_{SD}	V_{EN} = 0V	—	0.3	3	uA
Quiescent Current	I_{CCQ}	V_{EN} = 5.0V; V_{FB} = 1.05V	—	1.5	—	mA
Feedback Voltage	V_{FB}	4.8V≦V_{IN}≦40V	917	935	953	mV
		-40℃≦T_A≦85℃	907	—	963	mV
Feedback Overvoltage Threshold	$OVP_{(FB)}$		1.05	1.1	1.15	V_{FB}
High-Side Switch On Resistance (Note5)	$R_{DS(ON)1}$		—	130	—	mΩ
Low-Side Switch On Resistance (Note5)	$R_{DS(ON)2}$		—	100	—	mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V	—	—	10	μA
Upper Switch Current Limit		Minimum Duty Cycle	3.3	4.5	—	A
Lower Switch Current Limit		From Drain to Source	—	1.5	—	A
Oscillation Frequency	F_{OSC1}		280	350	420	KHz
Short Circuit Oscillation Frequency	F_{OSC2}	V_{FB} =< 0.5V	—	120	—	KHz
Maximum Duty Cycle	D_{MAX}		80	90	—	%
Minimum On Time (Note5)	$T_{ON(min)}$		—	180	—	ns
EN Lockout Threshold Voltage	$ENH_{(LOCK)}$		—	1.5	2	V
Input Under Voltage Lockout Threshold	UVLO	V_{IN} Rising	6.5	7.0	7.5	V
Input Under Voltage Lockout Threshold Hysteresis	UVLO-Hys		—	200	—	mV
Soft-Start Period		Cvdd=0.1μF	—	15	—	ms
Thermal Shutdown	T_{SD}		—	160	—	℃
Thermal Shutdown Hysterisis	T_{SH}		—	30	—	℃

Note 5: Guarantee by design

APPLICATION INFORMATION

The AT2721 is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 8V to 40V down to an output voltage as low as VFB, and supplies up to 3A of load current.

The AT2721 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal Tran conductance error amplifier. The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the AT2721 FB pin exceeds 10% of the nominal regulation voltage of VFB, the over voltage comparator is tripped and the COMP pin is discharged to GND, forcing the high-side switch off.

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio.

Thus the output voltage is:

$$V_{OUT} = VFB \times \frac{R1 + R2}{R2}$$

For example, VFB =0.935V for a 5.0V output voltage, R2 is 10kΩ, and R1 is 43.5kΩ.

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IIN(RMS)} = I_{OUT} \times \sqrt{D \times (1-D)}$$

Where D is the duty cycle and the value is V_{OUT} / V_{IN}. A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1uF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF low ESR electrolytic capacitor when operated in high input voltage range (V_{IN} > 20V). It can improve the device's stability. The output ripple voltage

ΔV_{OUT} is described as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{fs \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} + \left(\frac{1}{8 \times fs \times C2}\right)$$

Where f_S is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, R_{ESR} is the equivalent series resistance value of the output capacitor, and the C2 is the output capacitor. When using the ceramic capacitors, the R_{ESR} can be ignored and the output ripple voltage Δ VOUT is shown as:

$$\Delta V_{OUT} = \frac{VOUT}{8 \times fs^2 \times L \times C2} \times \left(1 - \frac{VOUT}{VIN}\right)$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage Δ VOUT can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{fs \times L} \times \left(1 - \frac{VOUT}{VIN}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The AT2721 can be optimized for a wide range of capacitance and ESR values.

Inductor

The output inductor is used for store energy and filter output ripple current. A large value inductor will result in less ripple current and lower output ripple voltage. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and results in lower output ripple voltage. A good rule for determining the inductance is set the peak-to-peak inductor ripple current ΔI almost equal to 30% of the maximum load current. Then the minimum inductance can be calculated with the following equation:

$$L \geq \frac{V_{OUT}}{fs \times \Delta I} \times \left(1 - \frac{VOUT}{VIN}\right)$$

$$\Delta I = 0.3 \times I_{LOAD(MAX)}$$

Where V_{IN} is the input voltage, fS is the switching frequency, ΔI is the peak-to-peak inductor ripple current and $I_{LOAD(MAX)}$ is the maximum load current. Choose an inductor that will cause the peak inductor current satisfying the equation:

$$I_{LP} = I_{LOAD(MAX)} + \frac{V_{OUT}}{2 \times fs \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \leq I_{LIMIT}$$

Where I_{LIMIT} is the high-side MOSFET current limit value.

Optional Schottky Diode

During the transition between switching MOSFETs, the body diode of the low-side MOSFET conducts the inductor current. The forward voltage of this body diode is large. An optional Schottky diode may be connected between SW pin and GND pin to improve overall efficiency.

Compensation Components

The system stability and transient response are controlled through the COMP pin. Selecting the appropriate compensation value by the following procedure:

1. Calculate the R_3 value with the following equation:

$$R3 < \frac{2\pi \times C2 \times fs \times V_{OUT}}{10 \times G_{EA} \times G_{CS} \times V_{FB}}$$

where G_{EA} is the error amplifier transconductance, and G_{CS} is the current sense transconductance.

2. Calculate the C_3 value with the following equation:

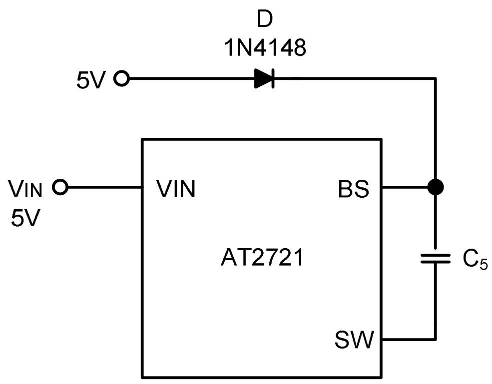
$$C3 > \frac{4 \times 10}{2\pi \times R3 \times fs}$$

3. If the C_2 ESR zero is less than half of the switching frequency, use C6 to cancel the ESR zero:

$$C6 > \frac{C2 \times R_{ESR}}{R3}$$

External Boost Diode Selection

For input voltage lower than 5.5V or duty cycle larger than 65% applications, it is recommended that an external boost diode be added. This helps improve the efficiency. The boost diode can be a low cost one such as 1N4148.



PCB Layout Recommendation

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1. Place the input capacitors, output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.

2. CIN must be closes to Pins VIN and GND. The loop area formed by CIN and VIN/GND pins must be minimized.

3. Place feedback resistors close to the FB pin.

4. Place compensation components close to the COMP pin.

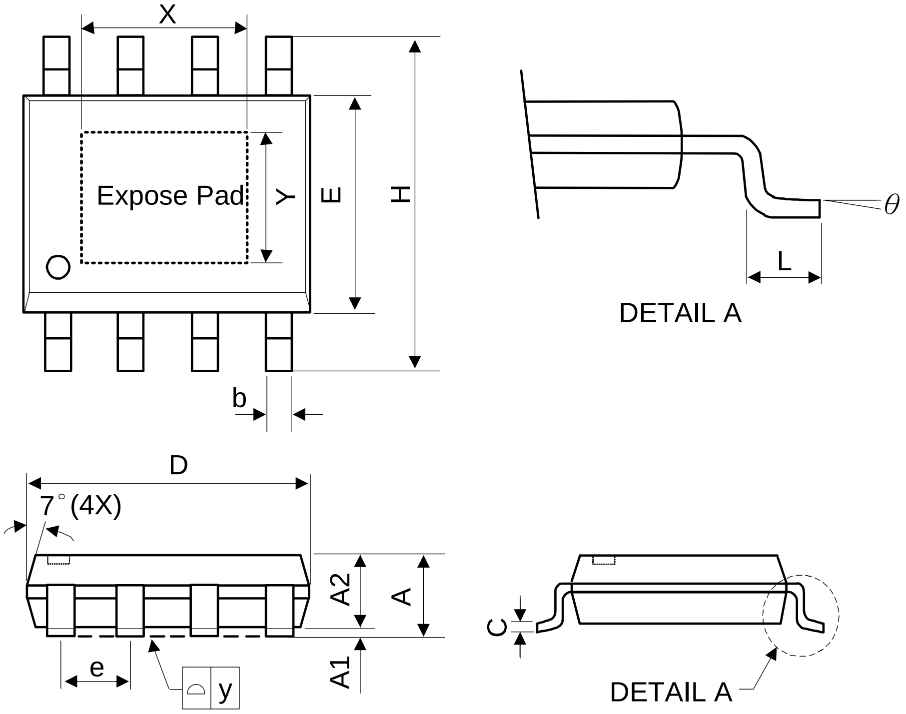
5. Keep the sensitive signal (FB, COMP) away from the switching signal (SW).

6. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.

7. Multi-layer PCB design is recommended.

PACKAGE OUTLINE DIMENSIONS

PSOP-8 PACKAGE OUTLINE DIMENSION



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	-	1.75
A1	0	0.15
A2	1.25	-
C	0.1	0.25
D	4.7	5.1
E	3.7	4.1
H	5.8	6.2
L	0.4	1.27
b	0.31	0.51
e	1.27 BSC	
y	-	0.1
X	-	3.33
Y	-	2.54
θ	0°	8°