## Features

- **Fast Read Access Time - 120 ns**
- **Dual Voltage Range Operation**
  - **Unregulated Battery Power Supply Range, 2.7V to 3.6V**
  - **or Standard 5V ± 10% Supply Range**
- **Compatible with JEDEC Standard AT27C040**
- **Low Power CMOS Operation**
  - **20 µA max. (less than 1 µA typical) Standby for $V_{CC}$ = 3.6V**
  - **29 mW max. Active at 5 MHz for $V_{CC}$ = 3.6V**
- **JEDEC Standard Packages**
  - **32-Lead PLCC**
  - **32-Lead TSOP**
- **High Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **JEDEC Standard for LVTTL and LVBO**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

## Description

The AT27BV040 chip is a high performance, low power, low voltage, 4,194,304 bit one-time programmable read only memory (EPROM) organized as 512K by 8 bits. It requires only one supply in the range of 2.7 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

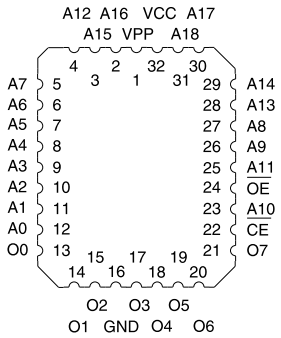
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At $V_{CC}$ = 2.7V, any byte can be accessed in less than 100 ns. With a typical power dissipation of only 18 mW at 5 MHz and $V_{CC}$ = 3V, the AT27BV040 consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3V. The AT27BV040 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

*(continued)*

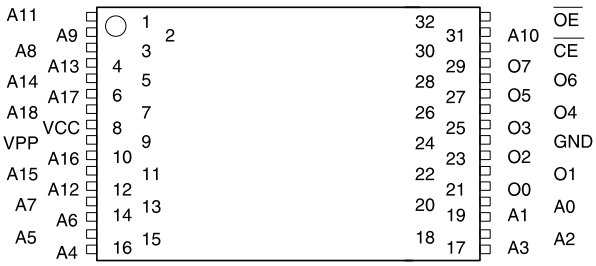
## Pin Configurations

| Pin Name | Function |
|---|---|
| A0 - A18 | Addresses |
| O0 - O7 | Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |

PLCC Top View




TSOP Top View
**Type 1**




# 4 Megabit (512K x 8) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

0346C

## Description (Continued)

The AT27BV040 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

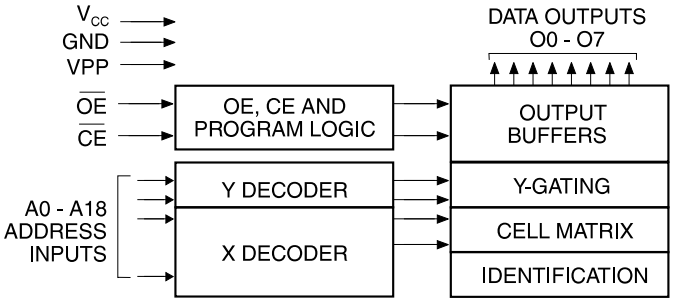
The AT27BV040 operating with $V_{CC}$ at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at $V_{CC}$ = 5.0V. At $V_{CC}$ = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV040 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV040 programs exactly the same way as a standard 5V AT27C040 and uses the same programming equipment.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the $V_{CC}$ and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the $V_{CC}$ and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram




## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -40°C to +85°C |
| Storage Temperature | -65°C to +125°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V (1) |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V (1) |
| $V_{PP}$ Supply Voltage with Respect to Ground | -2.0V to +14.0V (1) |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}$ + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

## Operating Modes

| **Mode \ Pin** | $\overline{CE}$ | $\overline{OE}$ | Ai | $V_{PP}$ | $V_{CC}$ | **Outputs** |
|---|---|---|---|---|---|---|
| Read (2) | $V_{IL}$ | $V_{IL}$ | Ai | X (1) | $V_{CC}$ (2) | $D_{OUT}$ |
| Output Disable (2) | X | $V_{IH}$ | X | X | $V_{CC}$ (2) | High Z |
| Standby (2) | $V_{IH}$ | X | X | X | $V_{CC}$ (2) | High Z |
| Rapid Program (3) | $V_{IL}$ | $V_{IH}$ | Ai | $V_{PP}$ | $V_{CC}$ (3) | $D_{IN}$ |
| PGM Verify (3) | X | $V_{IL}$ | Ai | $V_{PP}$ | $V_{CC}$ (3) | $D_{OUT}$ |
| PGM Inhibit (3) | $V_{IH}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ (3) | High Z |
| Product Identification (3, 5) | $V_{IL}$ | $V_{IL}$ | A9 = $V_H$ (4)<br>A0 = $V_{IH}$ or $V_{IL}$<br>A1 - A18 = $V_{IL}$ | X | $V_{CC}$ (3) | Identification Code |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.
2. Read, output disable, and standby modes require, $2.7V \le V_{CC} \le 3.6V$, or $4.5V \le V_{CC} \le 5.5V$.
3. Refer to Programming Characteristics. Programming modes require $V_{CC}$ = 6.5V.
4. $V_H = 12.0 \pm 0.5V$.
5. Two identifier bytes may be selected. All Ai inputs are held low ($V_{IL}$), except A9 which is set to $V_H$ and A0 which is toggled low ($V_{IL}$) to select the Manufacturer's Identification byte and high ($V_{IH}$) to select the Device Code byte.

## DC and AC Operating Conditions for Read Operation

| | | AT27BV040 | |
|---|---|---|---|
| | | -12 | -15 |
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C |
| $V_{CC}$ Power Supply | | 2.7V to 3.6V | 2.7V to 3.6V |
| | | 5V ± 10% | 5V ± 10% |

= Preliminary Information

## DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| **$V_{CC}$ = 2.7V to 3.6V** | | | | | |
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | | ±5 | µA |
| $I_{PP1}$ (2) | $V_{PP}$ (1) Read/Standby Current | $V_{PP}$ = $V_{CC}$ | | 10 | µA |
| $I_{SB}$ | $V_{CC}$ (1) Standby Current | $I_{SB1}$ (CMOS), $\overline{CE}$ = $V_{CC}$ ± 0.3V | | 20 | µA |
| | | $I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | 100 | µA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz, $I_{OUT}$ = 0 mA, $\overline{CE}$ = $V_{IL}$, $V_{CC}$ = 3.6V | | 8 | mA |
| $V_{IL}$ | Input Low Voltage | $V_{CC}$ = 3.0 to 3.6V | -0.6 | 0.8 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | -0.6 | 0.2 x $V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ = 3.0 to 3.6V | 2.0 | $V_{CC}$ + 0.5 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | 0.7 x $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | 0.4 | V |
| | | $I_{OL}$ = 100 µA | | 0.2 | V |
| | | $I_{OL}$ = 20 µA | | 0.1 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -2.0 mA | 2.4 | | V |
| | | $I_{OH}$ = -100 µA | $V_{CC}$ - 0.2 | | V |
| | | $I_{OH}$ = -20 µA | $V_{CC}$ - 0.1 | | V |
| **$V_{CC}$ = 4.5V to 5.5V** | | | | | |
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | | ±5 | µA |
| $I_{PP1}$ (2) | $V_{PP}$ (1) Read/Standby Current | $V_{PP}$ = $V_{CC}$ | | 10 | µA |
| $I_{SB}$ | $V_{CC}$ (1) Standby Current | $I_{SB1}$ (CMOS), $\overline{CE}$ = $V_{CC}$ ± 0.3V | | 100 | µA |
| | | $I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | 1 | mA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz, $I_{OUT}$ = 0 mA, $\overline{CE}$ = $V_{IL}$ | | 30 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |

Notes: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$, and removed simultaneously with or after $V_{PP}$.

2. $V_{PP}$ may be connected directly to $V_{CC}$, except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP}$.

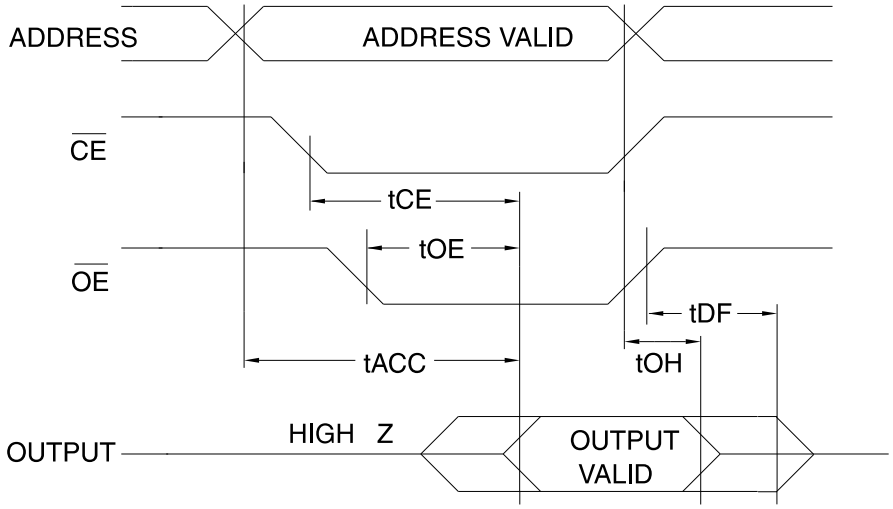
## AC Characteristics for Read Operation ($V_{CC}$ = 2.7V to 3.6V and 4.5V to 5.5V)

| Symbol | Parameter | Condition | AT27BV040 -12 Min | AT27BV040 -12 Max | AT27BV040 -15 Min | AT27BV040 -15 Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{ACC}$ (3) | Address to Output Delay | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 120 | | 150 | ns |
| $t_{CE}$ (2) | $\overline{CE}$ to Output Delay | $\overline{OE}$ = $V_{IL}$ | | 120 | | 150 | ns |
| $t_{OE}$ (2, 3) | $\overline{OE}$ to Output Delay | $\overline{CE}$ = $V_{IL}$ | | 50 | | 60 | ns |
| $t_{DF}$ (4, 5) | $\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first | | | 40 | | 50 | ns |
| $t_{OH}$ | Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first | | 0 | | 0 | | ns |

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

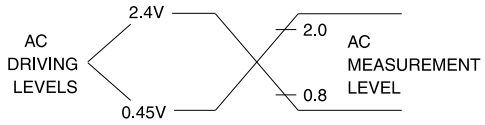
= Preliminary Information

## AC Waveforms for Read Operation (1)



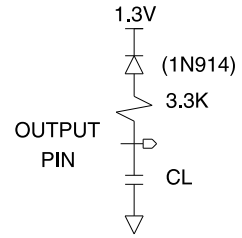

Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to $t_{CE}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the address is valid without impact on $t_{ACC}$.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

## Input Test Waveform and Measurement Level




$t_R$, $t_F$ < 20 ns (10% to 90%)

## Output Test Load



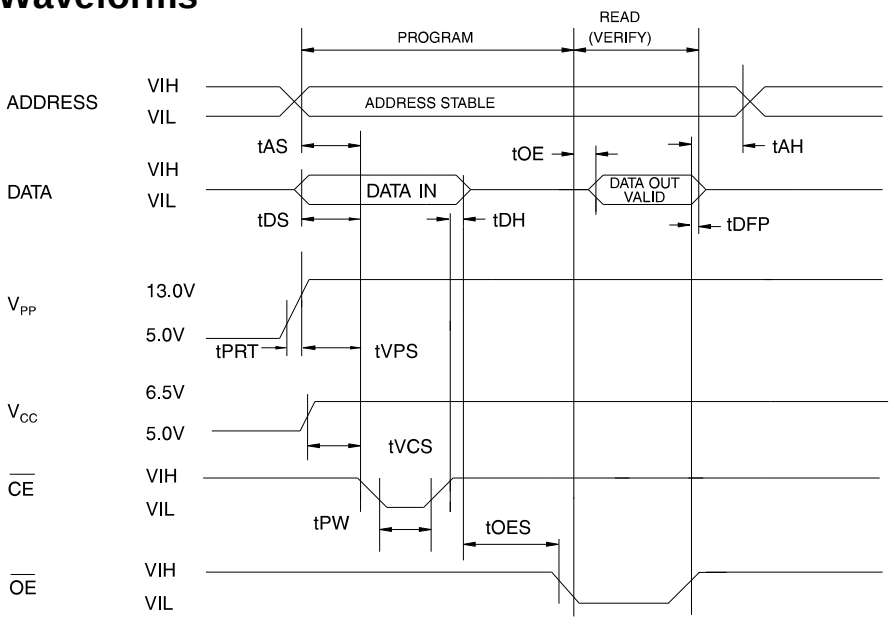

Note: CL = 100 pF
including jig capacitance.

## Pin Capacitance (f = 1 MHz, T = 25°C) [1]

| | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Programming Waveforms [1]




Notes: 1. The Input Timing Reference is 0.8V for $V_{IL}$ and 2.0V for $V_{IH}$.
2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV040 a 0.1 µF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients.

## DC Programming Characteristics

**$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ± 0.25V**

| Symbol | Parameter | Test Conditions | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ±10 | µA |
| $V_{IL}$ | Input Low Level | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ + 0.7 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | 40 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL}$ | | 20 | mA |
| $V_{ID}$ | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

## AC Programming Characteristics

**$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ± 0.25V**

| Symbol | Parameter | Test Conditions* (1) | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address Setup Time | | 2 | | µs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | µs |
| $t_{DFP}$ | $\overline{OE}$ High to Output Float Delay (2) | | 0 | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | µs |
| $t_{PW}$ | $\overline{CE}$ Program Pulse Width (3) | | 95 | 105 | µs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ (2) | | | 150 | ns |
| $t_{PRT}$ | $V_{PP}$ Pulse Rise Time During Programming | | 50 | | ns |

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

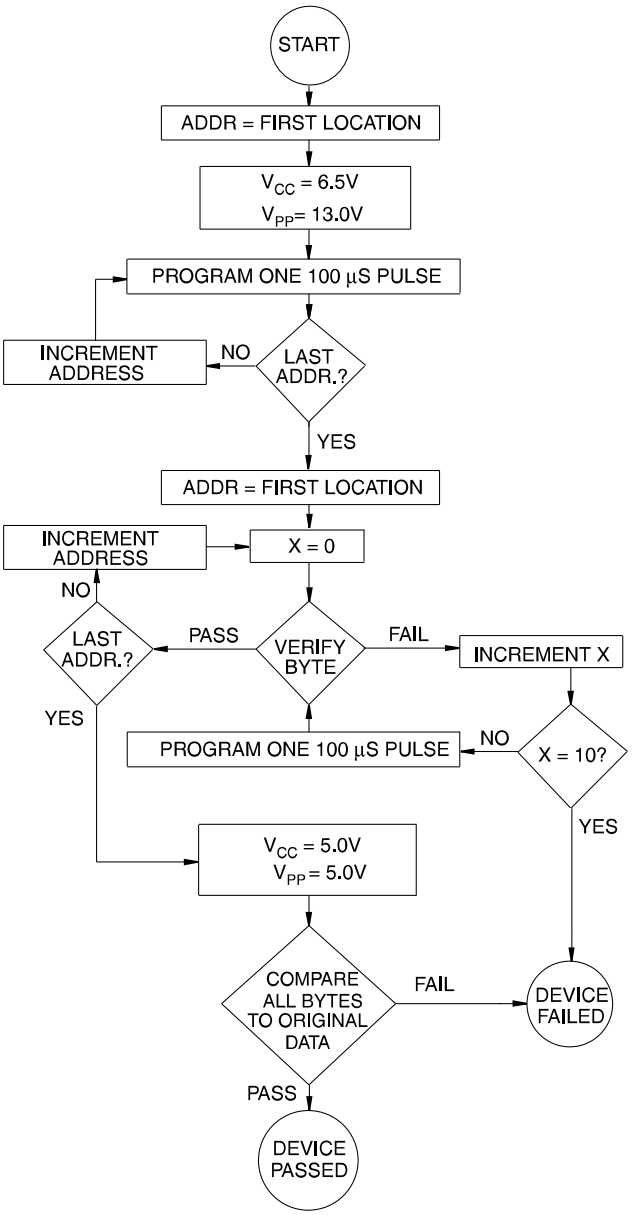
## Atmel's 27BV040 Integrated Product Identification Code (1)

| Codes | Pins A0 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| Device Type | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |

Note: 1. The AT27BV040 has the same Product Identification Code as the AT27C040. Both are programming compatible.

## Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. $V_{CC}$ is raised to 6.5V and $V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $V_{PP}$ is then lowered to 5.0V and $V_{CC}$ to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



## Ordering Information

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) $V_{CC}$ = 3.6V | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 120 | 8 | 0.02 | AT27BV040-12JC<br>AT27BV040-12TC | 32J<br>32T | Commercial<br>(0°C to 70°C) |
| | 8 | 0.02 | AT27BV040-12JI<br>AT27BV040-12TI | 32J<br>32T | Industrial<br>(-40°C to 85°C) |
| 150 | 8 | 0.02 | AT27BV040-15JC<br>AT27BV040-15TC | 32J<br>32T | Commercial<br>(0°C to 70°C) |
| | 8 | 0.02 | AT27BV040-15JI<br>AT27BV040-15TI | 32J<br>32T | Industrial<br>(-40°C to 85°C) |

= Preliminary Information

| Package Type | |
|---|---|
| **32J** | 32 Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| **32T** | 32 Lead, Plastic Thin Small Outline Package (TSOP) |