# ARM®-based 32-bit Cortex®-M4 MCU+FPU, 64 to 256 KB Flash, sLib, 15 timers, 1 ADC, 18 communication interfaces (2 CAN and 1 OTGFS)

## Features

- **AEC Q-100 certification**
- **Core: ARM® 32-bit Cortex®-M4 CPU with FPU**
  - 150 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 64 to 256 Kbytes of Flash memory
  - 20 Kbytes of boot memory used as a Bootloader or as a general instruction/data memory (one-time-configurable)
  - sLib: configurable part of main Flash as a library area with code executable but secured, non-readable
  - Up to 48 Kbytes of SRAM
  - External memory controller (XMC) with 16-bit data bus supporting multiplexed PSRAM and NOR memories
- **XMC as LCD parallel interface, 8080/6800 modes**
- **Power control (PWC)**
  - 2.4 to 3.6 V supply
  - Power-on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep, and Standby modes
  - 20x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal oscillator (HEXT)
  - 48 MHz internal factory-trimmed high speed clock (HICK), ±1 % accuracy at $T_A$ = 25 °C and ±2.5 % accuracy at $T_A$ = -40 to +105 °C, with automatic clock calibration (ACC)
  - 32 kHz crystal oscillator (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1x 12-bit 5.33 MSPS A/D converter, up to 24 external input channels; 12/10/8/6-bit resolution, hardware over-sampling up to equivalent 16-bit resolution
  - Temperature sensor ($V_{TS}$), internal reference voltage ($V_{INTRV}$)
  - 2x 12-bit D/A converters
- **DMA**
  - 2 x 7-channel DMA controllers with flexible mapping capability
- **Up to 87 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 15 timers (TMR)**
  - 1x 16-bit 7-channel advanced timer, including three pairs of complementary channels for PWM output, with dead-time generator and emergency brake
  - Up to 8x 16-bit + 1x 32-bit general-purpose timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature encoder input
  - 2x 16-bit basic timers
  - 2x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarm, subsecond accuracy, and hardware calendar, with calibration feature**
- **Up to 18 communication interfaces**
  - Up to 3x $I^2C$ interfaces (SMBus/PMBus)
  - Up to 3x SPI interfaces (36 Mbit/s), all with multiplexed half-duplex $I^2S$; 2x half-duplex $I^2S$ combined for full-duplex mode
  - Up to 8x USART interfaces support master synchronization SPI and modem control, ISO7816 interface, LIN, IrDA, and RS485 driver enable, TX/RX swap
  - Up to 2x CAN interfaces (2.0B Active), each with dedicated 256-byte buffer
  - OTGFS controller with on-chip PHY, dedicated 1280-byte buffer, supporting crystal-less in device mode
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug mode**
  - SWD and JTAG interfaces
- **Operating temperatures: -40 to +105 °C**

- **Packages**
  - LQFP100 14 x 14 mm
  - LQFP64 10 x 10 mm
  - LQFP64 7 x 7 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm
  - QFN36 6 x 6 mm
  - QFN32 4 x 4 mm

**Table 1. Device summary**

| Flash | Part number |
|---|---|
| 256 Kbytes | AT32A423VCT7, AT32A423RCT7, AT32A423RCT7-7, AT32A423CCT7, AT32A423CCU7, AT32A423TCU7, AT32A423KCU7-4 |
| 128 Kbytes | AT32A423VBT7, AT32A423RBT7, AT32A423RBT7-7, AT32A423CBT7, AT32A423CBU7, AT32A423TBU7, AT32A423KBU7-4 |
| 64 Kbytes | AT32A423V8T7, AT32A423R8T7, AT32A423R8T7-7, AT32A423C8T7, AT32A423C8U7, AT32A423T8U7, AT32A423K8U7-4 |

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# 1 Descriptions

The AT32A423 series microcontroller has passed AEC-Q-100 certification.

The AT32A423 series microcontroller is based on the high-performance ARM®Cortex®-M4 32-bit RISC core operating at a frequency of up to 150 MHz. The Cortex®-M4 core features a Floating Point Unit (FPU) single precision supporting all ARM® single-precision data processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

The AT32A423 series incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, 48 Kbytes of SRAM), and a wide range of enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib” (security library), functioning as a security area with code-executable only. In addition, the AT32A423 device includes a high-level memory extension: an external memory controller (XMC).

The AT32A423 series offers one 12-bit ADC, two 12-bit DACs, eight general-purpose 16-bit timers plus one general-purpose 32-bit timer, two basic timers, one advanced timer and one low-power ERTC. It supports standard and advanced communication interfaces: up to three $I^2C$s, three SPIs (multiplexed as $I^2S$s), eight USARTs, two CANs, one OTGFS, and infrared transmitter.

The AT32A423 series operates in the -40 to +105 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32A423 offers devices in different package types. They are fully pin-to-pin, software and functionally compatible for the entire AT32A423 series, except that the configurations of peripherals are not completely identical depending on the package types.

**Table 2. AT32A423 features and peripheral counts**

| Part Number | | AT32A423xxU7-4 | | | AT32A423xxU7 | | | AT32A423xxU7 | | | AT32A423xxT7 | | | AT32A423xxT7-7 | | | AT32A423xxT7 | | | AT32A423xxT7 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | KC | KB | K8 | TC | TB | T8 | CC | CB | C8 | CC | CB | C8 | RC | RB | R8 | RC | RB | R8 | VC | VB | V8 |
| CPU frequency (MHz) | | 150 | | | | | | | | | | | | | | | | | | | | |
| Flash memory (KB) | | 256 | 128 | 64 | 256 | 128 | 64 | 256 | 128 | 64 | 256 | 128 | 64 | 256 | 128 | 64 | 256 | 128 | 64 | 256 | 128 | 64 |
| SRAM (KB) | | 48 | 48 | 32 | 48 | 48 | 32 | 48 | 48 | 32 | 48 | 48 | 32 | 48 | 48 | 32 | 48 | 48 | 32 | 48 | 48 | 32 |
| XMC | | - | | | - | | | - | | | - | | | 1[1] | | | 1[1] | | | 1 | | |
| Timers | Advanced | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | 32-bit general-purpose | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | 16-bit general-purpose | 8 | | | 8 | | | 8 | | | 8 | | | 8 | | | 8 | | | 8 | | |
| | Basic | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | |
| | SysTick | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | WDT | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | WWDT | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | ERTC | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| Communication | $I^2C$ | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | |
| | SPI[2] | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | |
| | $I^2S$ (half-duplex)[2][3] | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | | 3 | | |
| | USART + UART | 4 + 3[4] | | | 4 + 3[4] | | | 4 + 3[4] | | | 4 + 3[4] | | | 5 + 3[5] | | | 5 + 3[5] | | | 8 + 0 | | |
| | CAN | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | |
| | OTGFS | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | IRTMR | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |

| Part Number | | AT32A423xxU7-4 | | | AT32A423xxU7 | | | AT32A423xxU7 | | | AT32A423xxT7 | | | AT32A423xxT7-7 | | | AT32A423xxT7 | | | AT32A423xxT7 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | KC | KB | K8 | TC | TB | T8 | CC | CB | C8 | CC | CB | C8 | RC | RB | R8 | RC | RB | R8 | VC | VB | V8 |
| Analog | 12-bit ADC numbers/external channels | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | | 1 | | |
| | | 11 | | | 11 | | | 17 | | | 17 | | | 23 | | | 23 | | | 24 | | |
| | 12-bit DAC | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | | 2 | | |
| GPIO | | 27 | | | 29 | | | 39 | | | 39 | | | 53 | | | 53 | | | 87 | | |
| Operating temperatures | | -40 °C to +105 °C | | | | | | | | | | | | | | | | | | | | |
| Packages | | QFN32<br>4 x 4 mm | | | QFN36<br>6 x 6 mm | | | QFN48<br>6 x 6 mm | | | LQFP48<br>7 x 7 mm | | | LQFP64<br>7 x 7 mm | | | LQFP64<br>10 x 10 mm | | | LQFP100<br>14 x 14 mm | | |

(1) For LQFP64 package, XMC only supports the 8-bit mode LCD panel.
(2) Half-duplex $I^2S$ shares the same pin with SPI
(3) Two half-duplex $I^2S$ can be configured by hardware to achieve full-duplex $I^2S$ function.
(4) For 48-pin packages and smaller, USART8 is not available, and USART5/6/7 can only be used as UART for no CK pinout.
(5) For 64-pin packages, USART5/7/8 can only be used as UART for no CK pinout.

# 2 Functionality overview

## 2.1 ARM®Cortex®-M4 with FPU

The ARM®Cortex®-M4 processor is the latest generation of ARM® processor for embedded systems. It is a 32-bit RISC high-performance processor that features exceptional code efficiency, outstanding computing performance and advanced response to interrupts. The processor supports a set of DSP instructions which enable efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up floating point calculation while avoiding saturation.

## 2.2 Memory

### 2.2.1 Flash memory

Up to 256 Kbytes of embedded Flash memory is available for storing programs and data. Any part of the embedded Flash memory can be protected by “sLib” (security library), a security area that is code-executable only but non-readable. “sLib” is a mechanism designed to protect the intelligence of solution venders and facilitate the second-level development by customers.

There is another 20-Kbyte boot memory in which the bootloader is stored. If it is not needed, this boot memory can be used as a general instruction/data memory (one-time-configurable), instead.

A User System Data block is included, which is used to configure hardware operations such as access/erase/write protection and watchdog self-enable. User System Data allows the independent configuration of Flash memory erase/write and access protection. The access protection is divided into low-level and high-level protections.

### 2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can further be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

### 2.2.3 Embedded SRAM

Up to 48 Kbytes of embedded SRAM (read/write) is accessible at CPU clock speed with 0 wait state.

### 2.2.4 External memory controller (XMC)

The XMC peripheral is embedded in the AT32A423 series. It has three Chip Select outputs supporting the following modes: multiplexed PSRAM and NOR memory.

Main features:

- Write buffer area
- Code execution from external memory of the multiplexed PSRAM/NOR

The XMC can be configured to interface with many graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes.

## 2.3 Interrupts

### 2.3.1 Nested vectored interrupt controller (NVIC)

The AT32A423 series embeds a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 25 edge-detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connect up to 16 GPIOs.

## 2.4 Power control (PWC)

### 2.4.1 Power supply schemes

- $V_{DD}$ = 2.4~3.6 V: power supply for GPIOs and the internal blocks such as ERTC, external 32 kHz crystal (LEXT), battery-powered register (BPR) and voltage regulator (LDO), provided externally via $V_{DD}$ pins
- $V_{DDA}$ = 2.4~3.6 V: power supply for ADC and DAC. $V_{DDA}$ and $V_{SSA}$ must be the same voltage potential as $V_{DD}$ and $V_{SS}$, respectively

### 2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR) and low-voltage reset (LVR) circuitry. It is always active and allows proper operation starting from 2.4 V. The device remains in reset mode when $V_{DD}$ goes below a specified threshold ($V_{LVR}$) without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the $V_{DD}$ power supply and compares it to the $V_{PVM}$ threshold. An interrupt is generated when $V_{DD}$ drops below the $V_{PVM}$ threshold or when $V_{DD}$ rises above the $V_{PVM}$ threshold. The PVM is enabled by software.

### 2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power-down.

- Normal mode: used in Run/Sleep mode or in Deepsleep mode;
- Low-power mode: used in Deepsleep mode;
- Power-down mode: used in Standby mode. The regulator LDO output is in high impedance and the kernel circuitry is powered down, and the contents of the registers and SRAM are lost.

This LDO operates always in normal mode after chip reset.

LDO output voltage is software configurable, including 1.3 V and 1.0 V in addition to default 1.2 V, so as to ensure the best trade-off between good performance and power consumption. *Table 12* shows the maximum AHB and APB clock frequencies corresponding to different LDO voltages. Therefore, it is highly advised for users to follow AT32A423 series reference manual to adjust LDO voltage and configure system clock.

### 2.4.4 Low-power modes

The AT32A423 series supports three low-power modes:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Deepsleep mode

  Deepsleep mode achieves low-power consumption while keeping the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The voltage regulator (LDO) can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm, wakeup, tamper, time stamp event, or OTG wakeup signal.
- Standby mode

  The Standby mode is used to acquire the lowest power consumption. The internal LDO is switched off so that the entire LDO power domain is powered down. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for ERTC and BPR registers and standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm/wakeup/tamper/timestamp occurs.

*Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. WDT depends on the User System Data settings.*

## 2.5 Boot modes

At startup, BOOT0 pin and nBOOT1 bit in the User System Data are used to select one of three boot options:

- Boot from Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in the boot memory. It is used to reprogram the Flash memory through USART1, USART2, USART3 or OTGFS1 (crystal-less support). *Table 3* provides the pin configurations for bootloader.

Table 3. Part numbers and pin configurations for bootloader

| Peripherals | Part numbers | Pins |
|---|---|---|
| USART1 | All | PA9: USART1_TX<br>PA10: USART1_RX |
| USART2 | AT32A423VxT7 | PD5: USART2_TX<br>PD6: USART2_RX |
| | Others | PA2: USART2_TX<br>PA3: USART2_RX |
| USART3 | AT32A423VxT7, AT32A423RxT7, AT32A423RxT7-7 | PC10: USART3_TX<br>PC11: USART3_RX<br>or<br>PB10: USART3_TX<br>PB11: USART3_RX |
| | AT32A423CxT7, AT32A423CxU7 | PB10: USART3_TX<br>PB11: USART3_RX |
| | Others | Not support |
| OTGFS1 | All | PA11: OTGFS1_D-<br>PA12: OTGFS1_D+ |

## 2.6 Clocks

On reset, the internal 48 MHz clock (HICK) divided by 6 (that is 8 MHz) is selected as the default CPU clock. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are available to allow the configuration of the AHB and the APB (APB1 and APB2) frequencies. The maximum frequency of the AHB and APB2 domains is 150 MHz, and APB1 120 MHz.

The AT32A423 series embeds an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK, assuring the most precise accuracy of the HICK in the full range of the operating temperatures.

## 2.7 General-purpose inputs / outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as multiplexed functions. Most of the GPIO pins are shared with digital or analog peripherals. All GPIOs are high current-capable.

The GPIO’s configuration can be locked, if needed, in order to avoid false writing to the GPIO’s registers by following a specific sequence.

## 2.8 Direct Memory Access Controller (DMA)

The AT32A423 series features two general-purpose DMA controllers (7-channel DMA1 and 7-channel DMA2) able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. These DMA channels can be connected to peripherals with flexible mapping ability.

The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software, and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI/$I^2S$, $I^2C$, USART, all TMRs, ADC and DAC.

## 2.9 Timers (TMR)

The AT32A423 series device includes an advanced timer, nine general-purpose timers, two basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

**Table 4. Timer feature comparison**

| Type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary output |
|---|---|---|---|---|---|---|---|
| Advanced | TMR1 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | 3 |
| General-purpose | TMR2 | 16-bit or 32-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| | TMR3 TMR4 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| | TMR9 TMR12 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 2 | 2 |
| | TMR10 TMR11 TMR13 TMR14 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TMR6 TMR7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | No | No |

### 2.9.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time insertion. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-period mode output

If configured as a standard 16-bit timer, it has the same features as those of the TMRx timer. If configured as a 16-bit PWM generator, it boasts full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen, and the PWM outputs are disabled to turn off any power switch driven by these outputs.

Many features are identical with those of the general-purpose TMRs that have the same architecture. Thus, the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

### 2.9.2 General-purpose timers (TMR2~4 and TMR9~14)

Up to nine synchronizable general-purpose timers are embedded in the AT32A423 series.

- **TMR2, TMR3 and TMR4**

  The TMR2 timer is based on a 32-bit auto-reload upcounter/downcounter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload upcounter/downcounter and a 16-bit prescaler. They can offer up to four independent channels on the large-size packages. Each channel can be used for input capture/output compare, PWM or one-period mode outputs.

  These general-purpose timers can work with the advanced timer via the link feature for synchronization or event chaining. Any of these general-purpose timers can be used to generate PWM outputs. Each timer has its individual DMA request mechanism.

  They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors. In debug mode, counters can be frozen.

- **TMR9 and TMR12**

  TMR9 and TMR12 are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They both feature two independent channels and two complementary channels for input capture/output compare, PWM, or one-period mode output. They can be synchronized with the TMR2, TMR3, and TMR4 full-featured general-purpose timers. They can also be used as simple timers. In debug mode, counters can be frozen. These timers have their separate DMA request generation.

- **TMR10, TMR11, TMR13 and TMR14**

  These timers are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They all feature one independent channel and one complementary channel for input capture/output compare, PWM, or one-period mode output. They can be synchronized with the TMR2, TMR3, and TMR4 full-featured general-purpose timers. They can also be used as simple timers. In debug mode, counters can be frozen. These timers have their separate DMA request.

### 2.9.3 Basic timers (TMR6 and TMR7)

These two timers are mainly used for DAC trigger generation. Each of them can be used as a generic 16-bit time base.

### 2.9.4 SysTick timer

This timer is dedicated to real-time operating systems, but it could also be used as a standard downcounter. Its features include:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock sources (HCLK or HCLK/8)

## 2.10 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabled or not through the User System Data. The counter can be frozen in debug mode.

## 2.11 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock and works as an early warning interrupt feature. The counter can be frozen in debug mode.

## 2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- 20x 32-bit battery powered registers (BPRs)

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Support sub-seconds value in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic interrupts wakeup from Deepsleep or Standby mode.
- ERTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation

These two alarm registers are used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

A prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 80 bytes of user application data. Battery powered registers are not reset by a system or power reset, nor when the device is woken up from the Standby mode.

*Note: With regard to ERTC, LEXT and BPR-related functions, when $V_{DD}$ power-on rate is lower than 1.3 ms/V, it is necessary for code to wait 60 ms until the $V_{DD}$ is higher than 2.57 V before accessing battery powered domain registers. Doing so can guarantee normal access operation even if $V_{DD}$ voltage drops below 2.57 V later. Refer to AT32A423 errata sheet for details.*

## 2.13 Communication interfaces

### 2.13.1 Serial peripheral interface (SPI)

There are up to three SPIs able to communicate at up to 32 Mbits/s in slave and master modes in full-duplex and half-duplex modes. The frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD/MMC/SDHC card modes. All SPIs can be served by the DMA controllers.

The SPI interface can be configured to operate in TI mode for communications in master and slave modes.

### 2.13.2 Inter-integrated sound interface ($I^2S$)

Three standard $I^2S$ interfaces (multiplexed with SPI) can be operated in master or slave mode, in half-duplex mode. These interfaces can be configured to operate with 16/24/32-bit resolution, as input or output channels. Audio sampling frequencies ranges from 8 kHz up to 192 kHz. When $I^2S$ is configured in master mode, the master clock can be output at 256 times the sampling frequency.

All $I^2S$s can be served by the DMA controller.

In addition, any two of $I^2S$ interfaces in half-duplex mode can be combined (through hardware) to achieve full-duplex communication function, while the remaining one can still operate independently or used as a SPI.

### 2.13.3 Universal synchronous / asynchronous receiver transmitter (USART)

The AT32A423 series embeds eight universal synchronous/asynchronous receiver transmitters (USART1~8).

These eight interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, LIN Master/Slave capability, hardware management of the CTS and RTS signals, RS485 drive enable signal, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All interfaces can be served by the DMA controller, with TX/RX swap support.

USART1 and USART6 are able to communicate at a speed of up to 9.375 Mbit/s, while other USART interfaces can be up to 7.5 Mbit/s.

**Table 5. USART feature comparison**

| USART feature | USART1/2/3/4 | USART6 | USART5/7/8 |
|---|---|---|---|
| Hardware flow control for modem | Yes | - | For RTS only |
| Continuous communication with DMA | Yes | Yes | Yes |
| Multiprocessor communication | Yes | Yes | Yes |
| Synchronous mode | Yes | Yes | Yes |
| Smartcard mode | Yes | Yes | Yes |
| Single-wire half-duplex communication | Yes | Yes | Yes |
| IrDA SIR ENDEC | Yes | Yes | Yes |
| LIN mode | Yes | Yes | Yes |
| TX/RX swap | Yes | Yes | Yes |
| RS-485 driver enable | Yes | Yes | Yes |

### 2.13.4 Inter-integrated-circuit interface ($I^2C$)

Up to three $I^2C$ bus interfaces can operate in multi-master and slave modes. They support standard mode (max. 100 kHz), fast mode (max. 400 kHz). Specifically, $I^2C1$ and $I^2C2$ support fast mode plus (max. 1 MHz). Some GPIOs provide ultra-high sink current of 20 mA.

They support 7-bit/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

### 2.13.5 Controller area network (CAN)

The AT32A423 series offers up to two CAN interfaces that are compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive buffers with 3 stages, and 14 scalable filter banks. Each CAN has dedicated 256 bytes of buffer, which is not shared with any other CAN or peripherals.

To guarantee CAN transmission quality, the CAN 2.0 protocol states that its clock source must come from the HEXT-based PLL clock.

### 2.13.6 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32A423 series embeds one USB OTG full-speed (12 Mb/s) device/host peripheral with integrated transceivers (PHY). It has software-configurable endpoint settings and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock. In host mode, this clock shoule be PLL clocked by HEXT crystal, and only in device mode, the 48 MHz HICK can be selected as the source of this clock directly.

OTGFS has the major features such as:

- Dedicated 1280 bytes of buffer (not shared with any other peripherals)
- 8 IN + 8 OUT endpoints (endpoint 0 included, device mode)
- 16 channels (host mode)
- SOF and OE output
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - Host mode: full-speed and low-speed
  - Device mode: full-speed

### 2.13.7 Infrared transmitter (IRTMR)

The AT32A423 series device provides an infrared transmitter solution. The solution is based on the internal connection between TMR10, USART1, or between USART2 and TMR11. The TMR11 is used to provide carrier frequency, while TMR10, USART1, or USART2 provides the main signal to be sent.

To generate infrared remote control signals, TMR10 channel 1 and TMR11 channel 1 must be correctly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

## 2.14 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

## 2.15 Analog-to-digital converter (ADC)

A 12-bit analog-to-digital converter (ADC) is embedded in AT32A423 device and features below:

- Configurable 12-bit, 10-bit, 8-bit, 6-bit resolution with self-calibration
- 5.33 MSPS maximum conversion rate in 12-bit resolution; conversion time can be shorten through the reduction of resolution
- Share up to 24 external channels, including six fast channels
- Two internal channels dedicated to internal temperature sensor ($V_{TS}$), internal reference voltage ($V_{INTRV}$)
- Channel-by-channel programmable sampling time
- 2 to 256 times hardware over-sampling, equivalent to maximum 16-bit resolution
- Trigger option for both regular and preempted conversion:
  - Software
  - Polarity-configurable hardware (internal timer event or GPIO input event)
- Converting modes:
  - Single mode or sequential mode
  - In sequential mode, each trigger performs conversions on a selected group of channels
  - Repeated mode converts the selected channels continuously
  - Partition mode
- A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.
- The ADC can be served by the DMA controllers

### 2.15.1 Temperature sensor ($V_{TS}$)

The temperature sensor generates a voltage $V_{TS}$ that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to the applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

### 2.15.2 Internal reference voltage ($V_{INTRV}$)

The internal reference voltage ($V_{INTRV}$) provides a stable voltage source for ADC. The $V_{INTRV}$ is internally connected to the ADC1_IN17 input channel.

## 2.16 Digital-to-analog converter (DAC)

The two 12-bit buffered DACs can be used to convert two digital signals into two analog voltage signal outputs.

This DAC has the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left- or right-aligned data in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each DAC
- External triggers for conversion
- Input voltage reference $V_{REF+}$

Several DAC trigger inputs are used in the AT32A423 series. DAC outputs can be triggered through the timer update outputs that are also connected to different DMA channels.

## 2.17 Serial wire debug (SWD)/JTAG debug port

The ARM®SWJ-DP interface is embedded in the AT32A423 series, and it is a combined serial wire debug port and JTAG that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively. In addition, the SWO feature is available for asynchronous tracing in debug mode.

# 3 Pin functional definitions

**Figure 1. AT32A423 LQFP100 pinout**

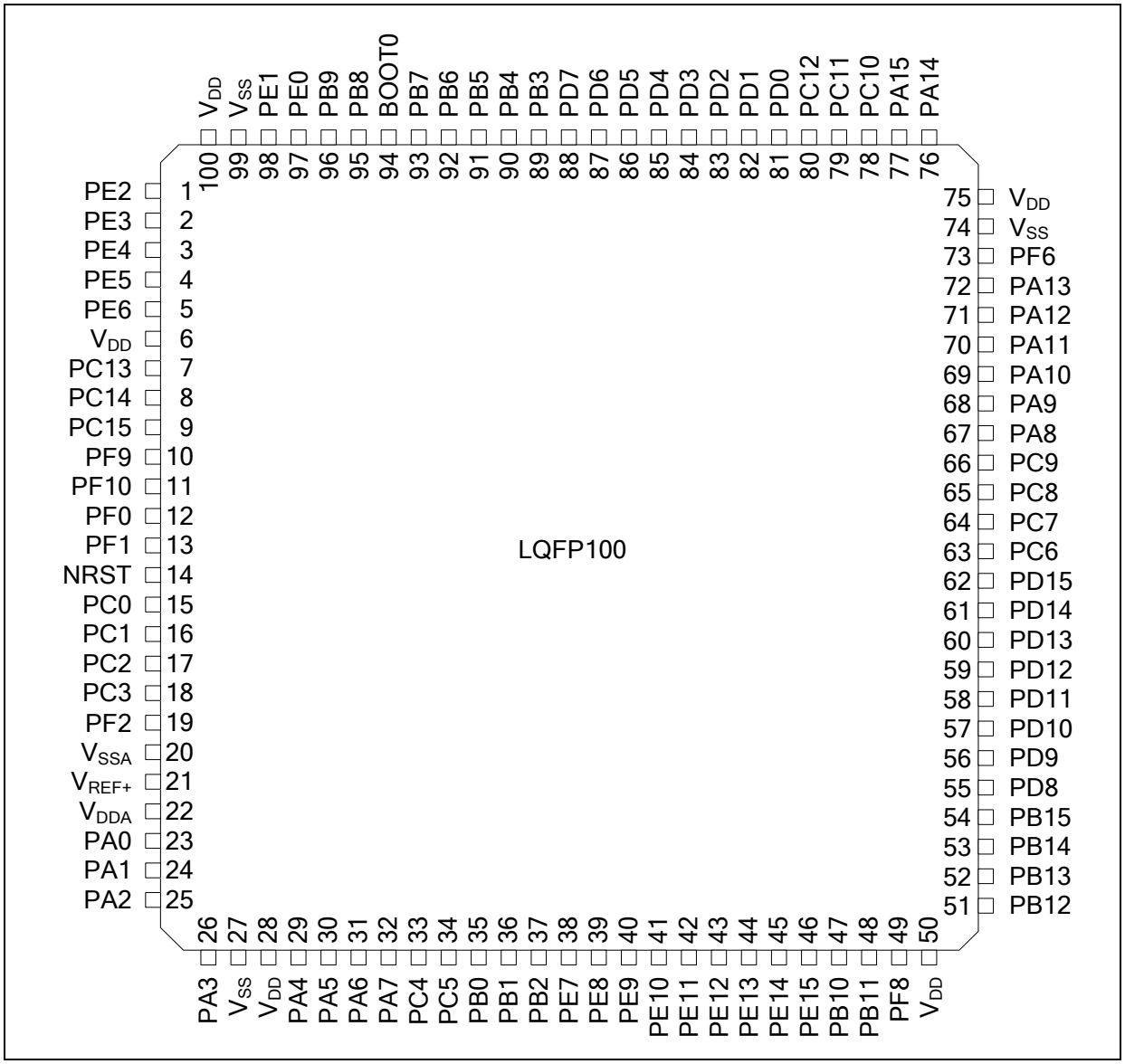


**Figure 2. AT32A423 LQFP64 pinout**

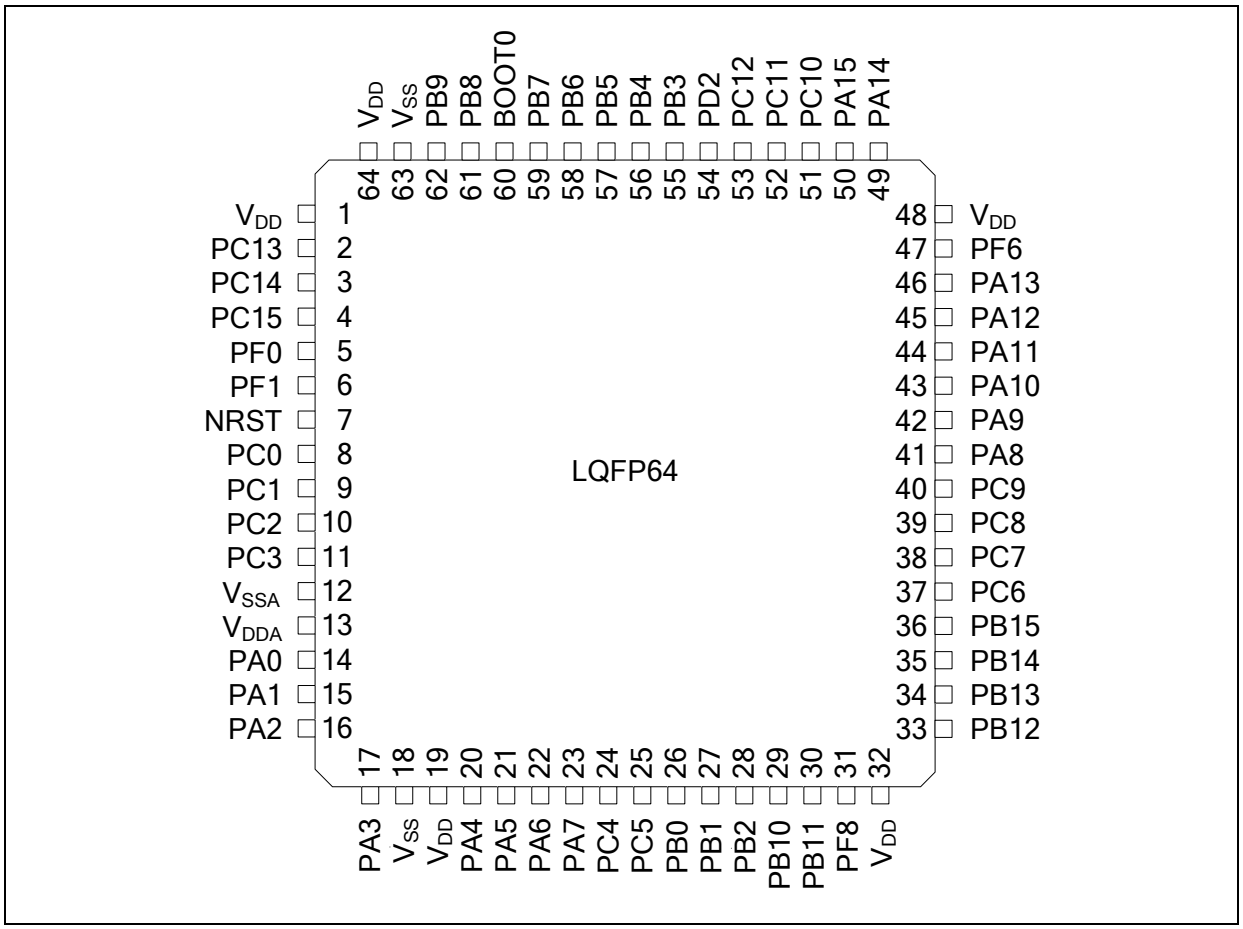



**Figure 3. AT32A423 LQFP48 pinout**

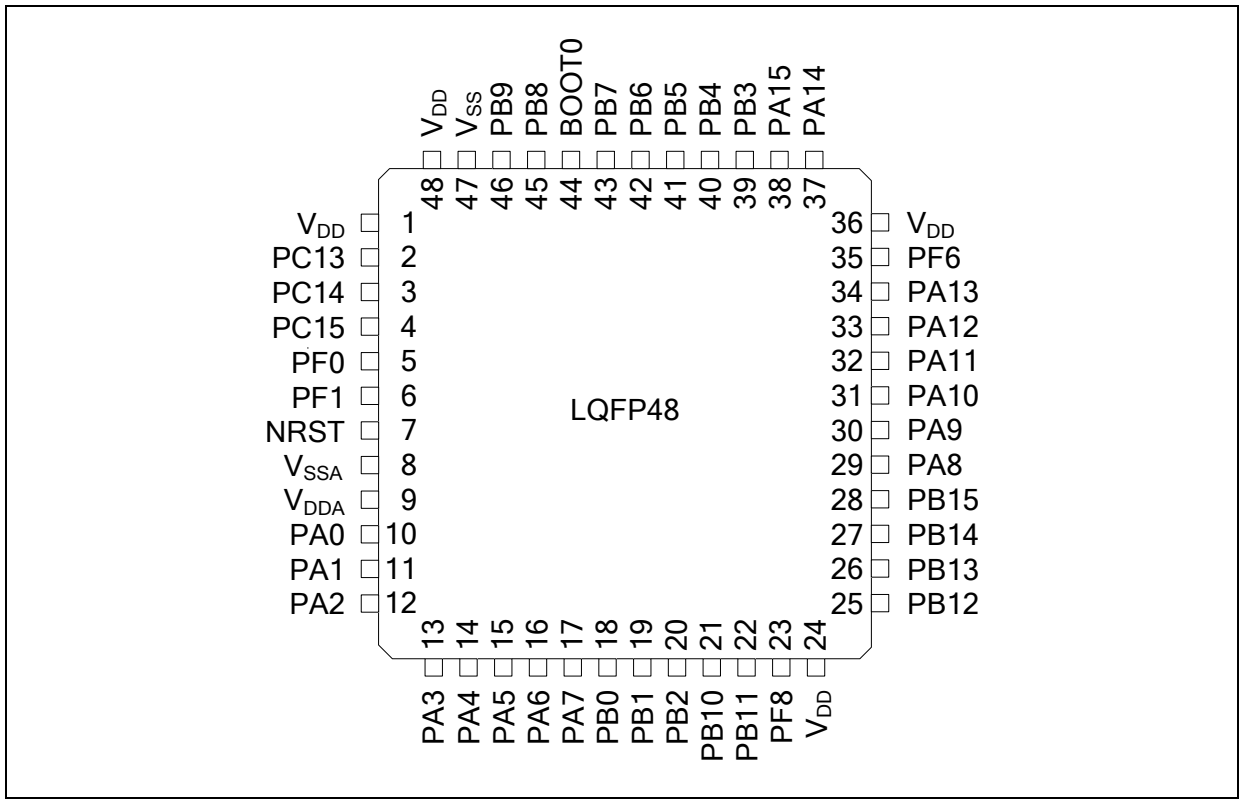


Figure 4. AT32A423 QFN48 pinout

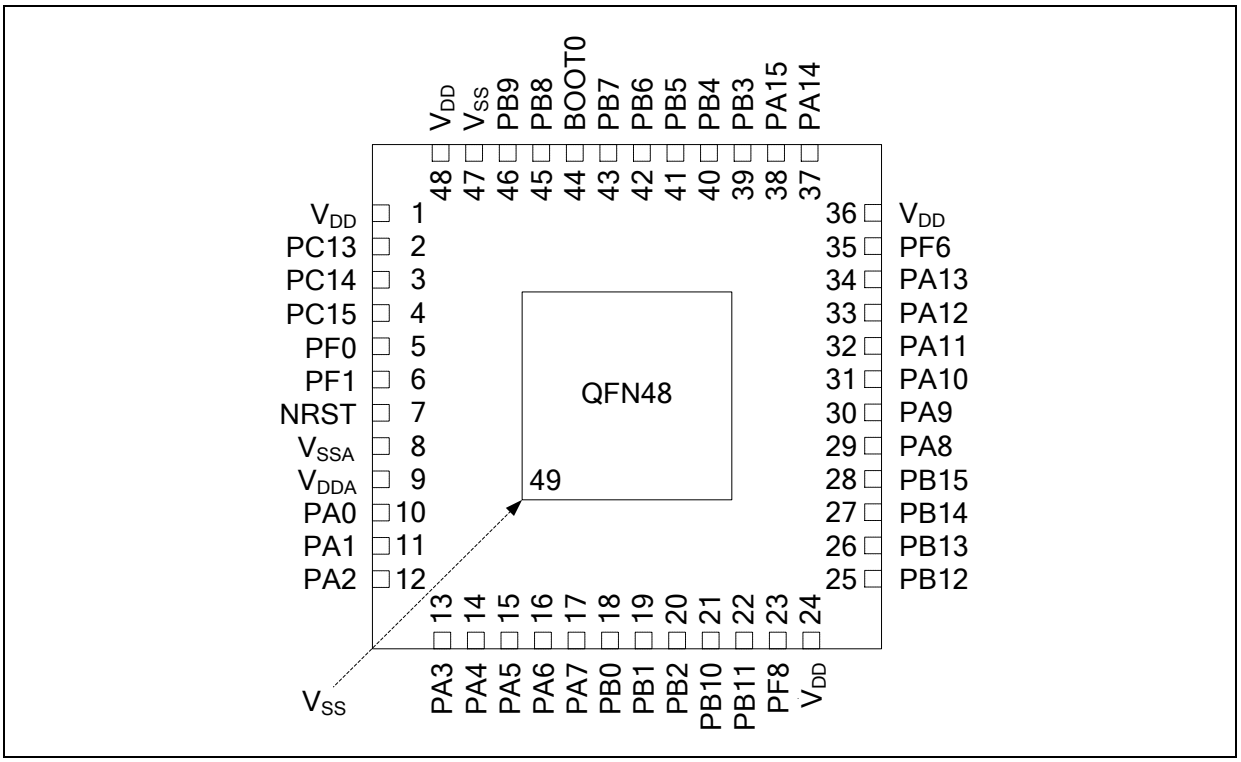



Figure 5. AT32A423 QFN36 pinout

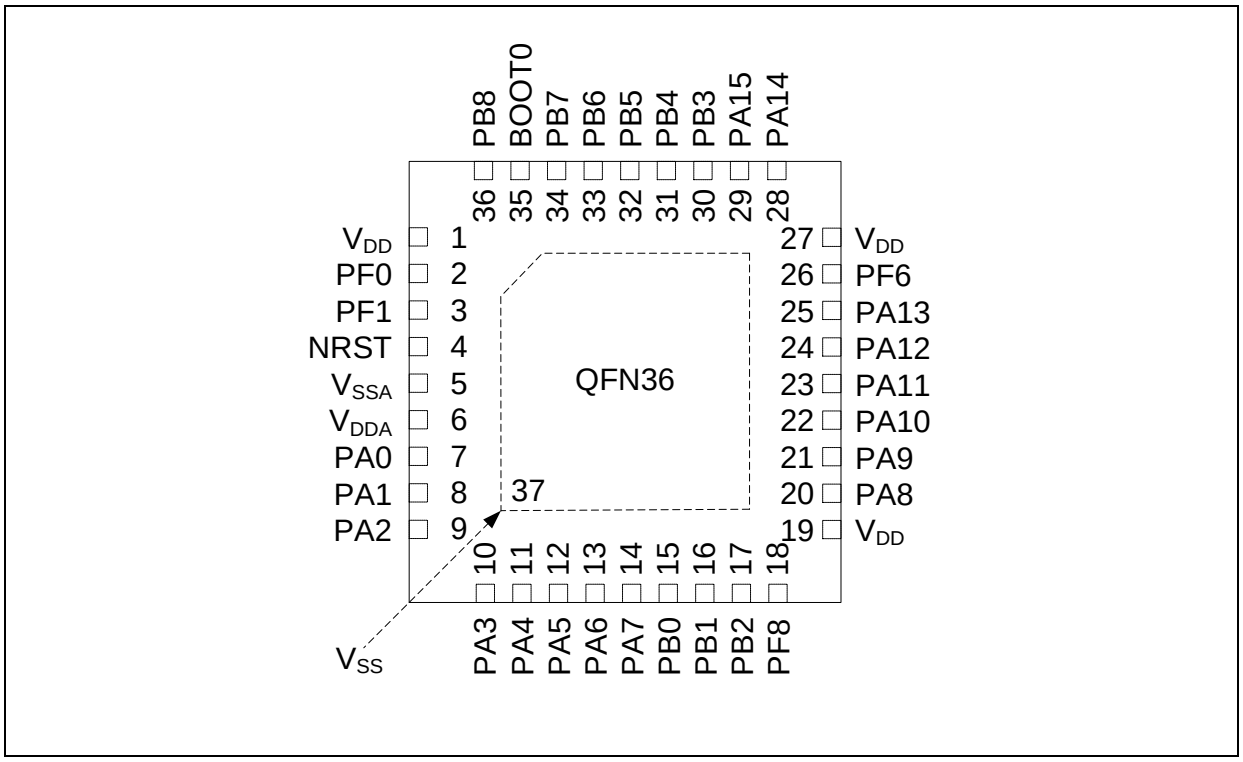
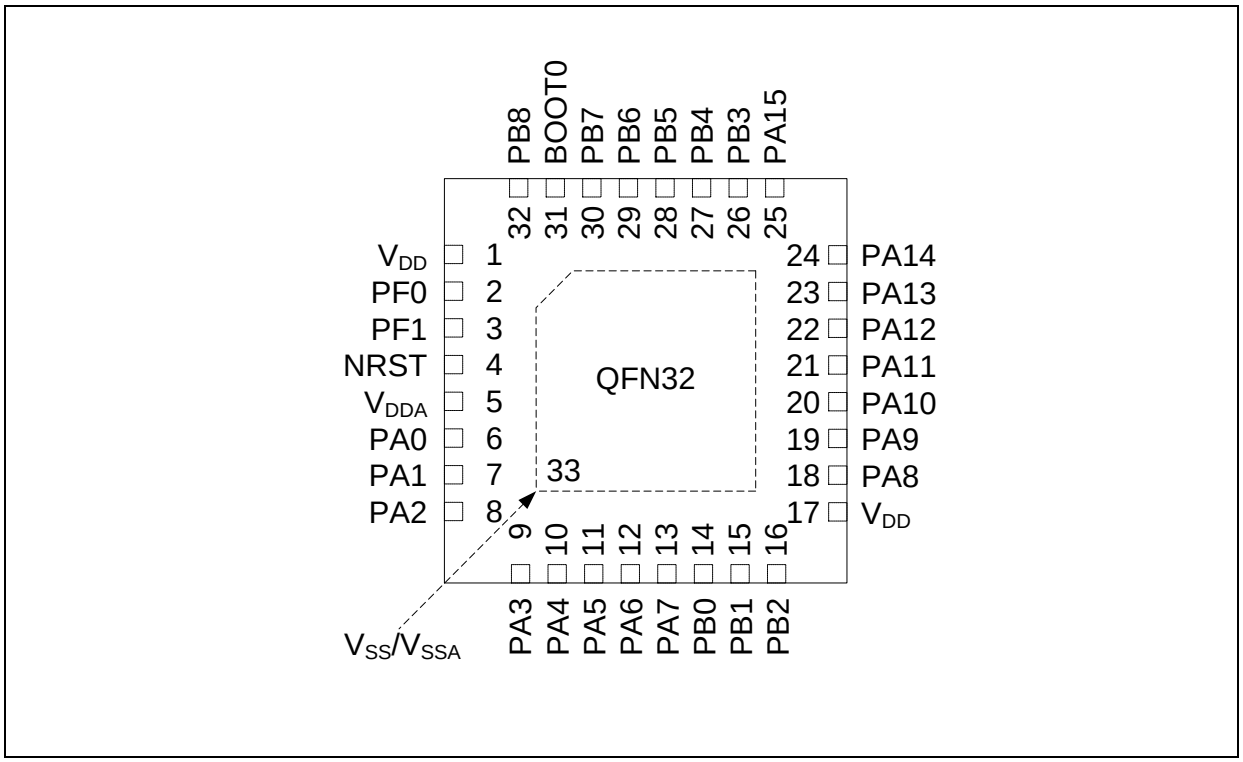


**Figure 6. AT32A423 QFN32 pinout**



The table below is the pin definition of the AT32A423 series. “-” represents that there is no such pinout on the related package. Unless descriptions in () under pin name, the functions during reset and after reset are the same as those of the actual pin name. Unless otherwise specified, all GPIOs are set as input floating during reset and after reset. Pin multiplexed functions are selected through GPIOx_MUXx registers and the additional functions are directly selected/enabled through peripheral registers.

**Table 6. AT32A423 series pin definitions**

| Pin numbers | | | | | Pin names (function after reset) | Type (1) | GPIO level (2) | Multiplexed functions(3) | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| QFN32 | QFN36 | LQFP48/ QFN48 | LQFP64 | LQFP100 | | | | | |
| - | - | - | - | 1 | PE2 | I/O | FT | TMR3_EXT / TMR9_BRK / TMR14_CH1C / XMC_A23 | - |
| - | - | - | - | 2 | PE3 | I/O | FT | TMR3_CH1 / TMR9_CH2C / TMR14_BRK / XMC_A19 | - |
| - | - | - | - | 3 | PE4 | I/O | FT | TMR3_CH2 / TMR9_CH1C / XMC_A20 | - |
| - | - | - | - | 4 | PE5 | I/O | FT | TMR3_CH3 / TMR9_CH1 / XMC_A21 | - |
| - | - | - | - | 5 | PE6 | I/O | FT | TMR3_CH4 / TMR9_CH2 / XMC_A22 | - |
| - | - | 1 | 1 | 6 | $V_{DD}$ | S | - | Digital power supply | |
| - | - | 2 | 2 | 7 | PC13(4)(5) | I/O | FT | - | ERTC_OUT / TAMP1 / WKUP2 |
| - | - | 3 | 3 | 8 | PC14(4) | I/O | TC | - | LEXT_IN |
| - | - | 4 | 4 | 9 | PC15(4) | I/O | TC | - | LEXT_OUT |
| - | - | - | - | 10 | PF9 | I/O | FT | TMR4_CH1 / USART6_TX / TMR12_CH1 | - |
| - | - | - | - | 11 | PF10 | I/O | FT | TMR4_CH2 / USART6_RX / TMR12_CH2 | - |
| 2 | 2 | 5 | 5 | 12 | PF0 | I/O | TC | TMR1_CH1 / I2C1_SDA | HEXT_IN |
| 3 | 3 | 6 | 6 | 13 | PF1 | I/O | TC | TMR1_CH2C / I2C1_SCL / SPI2_CS / I2S2_WS | HEXT_OUT |
| 4 | 4 | 7 | 7 | 14 | NRST | I/O | R | Device reset input / internal reset output (active low) | |
| - | - | - | 8 | 15 | PC0 | I/O | FTa | I2C3_SCL / I2C1_SCL / USART6_TX / USART7_TX | ADC1_IN10(6) |
| - | - | - | 9 | 16 | PC1 | I/O | FTa | I2C3_SDA / SPI3_MOSI / I2S3_SD / SPI2_MOSI / I2S2_SD / I2C1_SDA / USART6_RX / USART7_RX | ADC1_IN11(6) |
| - | - | - | 10 | 17 | PC2 | I/O | FTa | SPI2_MISO / I2S2_MCK / I2S_SDEXT / USART8_TX / XMC_NWE | ADC1_IN12(6) |
| | - | - | 11 | 18 | PC3 | I/O | FTa | SPI2_MOSI / I2S2_SD / USART8_RX / XMC_A0 | ADC1_IN13(6) |
| | - | - | - | 19 | PF2 | I/O | FT | SPI2_SCK / I2S2_CK / USART7_CK_RTS_DE | - |
| - | 5 | 8 | 12 | 20 | $V_{SSA}$ | S | - | Analog ground | |
| - | - | - | - | 21 | $V_{REF+}$ | S | - | Positive reference voltage | |
| 5 | 6 | 9 | 13 | 22 | $V_{DDA}$ | S | - | Analog power supply | |
| 6 | 7 | 10 | 14 | 23 | PA0 | I/O | FTa | TMR2_CH1 / TMR2_EXT / TMR9_CH2C / I2C2_SCL / USART2_RX / USART2_CTS / USART4_TX | ADC1_IN0(6) / TAMP2 / WKUP1 |

| Pin numbers | | | | | Pin names (function after reset) | Type (1) | GPIO level (2) | Multiplexed functions(3) | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| QFN32 | QFN36 | LQFP48/ QFN48 | LQFP64 | LQFP100 | | | | | |
| 7 | 8 | 11 | 15 | 24 | PA1 | I/O | FTa | TMR2_CH2 / TMR9_CH1C / I2C2_SDA / I2C1_SMBA / SPI3_CS / I2S3_WS USART2_RTS_DE / USART4_RX | ADC1_IN1(6) |
| 8 | 9 | 12 | 16 | 25 | PA2 | I/O | FTa | TMR2_CH3 / TMR9_CH1 / USART2_TX / CAN2_RX / XMC_D4 | ADC1_IN2 |
| 9 | 10 | 13 | 17 | 26 | PA3 | I/O | FTa | TMR2_CH4 / TMR9_CH2 / I2S2_MCK / USART2_RX / CAN2_TX / XMC_D5 | ADC1_IN3 |
| - | - | - | 18 | 27 | $V_{SS}$ | S | - | Digital ground | |
| - | - | - | 19 | 28 | $V_{DD}$ | S | - | Digital power supply | |
| 10 | 11 | 14 | 20 | 29 | PA4 | I/O | FTa | I2C1_SCL / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART2_CK / USART6_TX / TMR14_CH1 / OTGFS1_OE / XMC_D6 | ADC1_IN4 / DAC1_OUT |
| 11 | 12 | 15 | 21 | 30 | PA5 | I/O | FTa | TMR2_CH1 / TMR2_EXT / SPI1_SCK / I2S1_CK / USART3_CK / USART3_RX / USART6_RX / TMR13_CH1C / XMC_D7 | ADC1_IN5 / DAC2_OUT |
| 12 | 13 | 16 | 22 | 31 | PA6 | I/O | FTa | TMR1_BRK / TMR3_CH1 / SPI1_MISO / I2S1_MCK / I2S2_MCK / USART3_CTS / USART3_RX / TMR13_CH1 | ADC1_IN6 |
| 13 | 14 | 17 | 23 | 32 | PA7 | I/O | FTa | TMR1_CH1C / TMR3_CH2 / I2C3_SCL / SPI1_MOSI / I2S1_SD / USART3_TX / TMR14_CH1 | ADC1_IN7 |
| - | - | - | 24 | 33 | PC4 | I/O | FTa | TMR9_CH1 / I2S1_MCK / USART3_TX / TMR13_CH1 / XMC_NE4 | ADC1_IN14 |
| - | - | - | 25 | 34 | PC5 | I/O | FTa | TMR9_CH2 / I2C1_SMBA / USART3_RX / TMR13_CH1C / XMC_NOE | ADC1_IN15 |
| 14 | 15 | 18 | 26 | 35 | PB0 | I/O | FTa | TMR1_CH2C / TMR3_CH3 / SPI1_MISO / I2S1_MCK / SPI3_MOSI / I2S3_SD / USART2_RX / USART3_CK | ADC1_IN8 |
| 15 | 16 | 19 | 27 | 36 | PB1 | I/O | FTa | TMR1_CH3C / TMR3_CH4 / SPI1_MOSI / I2S1_SD / SPI2_SCK / I2S2_CK / USART2_CK / USART3_RTS_DE / TMR14_CH1 | ADC1_IN9 |
| 16 | 17 | 20 | 28 | 37 | PB2 | I/O | FTa | TMR2_CH4 / TMR3_EXT / I2C3_SMBA / SPI3_MOSI / I2S3_SD / TMR14_CH1C | ADC1_IN20 |
| - | - | - | - | 38 | PE7 | I/O | FTa | TMR1_EXT / USART5_CK / USART7_RX / XMC_D4 | ADC1_IN27 |
| - | - | - | - | 39 | PE8 | I/O | FT | TMR1_CH1C / USART4_TX / USART7_TX / XMC_D5 | - |
| - | - | - | - | 40 | PE9 | I/O | FT | TMR1_CH1 / USART4_RX / XMC_D6 | - |
| - | - | - | - | 41 | PE10 | I/O | FT | TMR1_CH2C / USART5_TX / XMC_D7 | - |
| - | - | - | - | 42 | PE11 | I/O | FT | TMR1_CH2 / USART5_RX / XMC_D8 | - |
| - | - | - | - | 43 | PE12 | I/O | FT | TMR1_CH3C / SPI1_CS / I2S1_WS / XMC_D9 | - |

| Pin numbers | | | | | Pin names (function after reset) | Type (1) | GPIO level (2) | Multiplexed functions(3) | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| QFN32 | QFN36 | LQFP48/ QFN48 | LQFP64 | LQFP100 | | | | | |
| - | - | - | - | 44 | PE13 | I/O | FT | TMR1_CH3 / SPI1_SCK / I2S1_CK / XMC_D10 | - |
| - | - | - | - | 45 | PE14 | I/O | FT | TMR1_CH4 / SPI1_MISO / I2S1_MCK / XMC_D11 | - |
| - | - | - | - | 46 | PE15 | I/O | FT | TMR1_BRK / SPI1_MOSI / I2S1_SD / XMC_D12 | - |
| - | - | 21 | 29 | 47 | PB10 | I/O | FTa | TMR2_CH3 / I2C2_SCL / SPI2_SCK / I2S2_CK / I2S3_MCK / USART3_TX / XMC_NOE | ADC1_IN21 |
| - | - | 22 | 30 | 48 | PB11 | I/O | FTa | TMR2_CH4 / I2C2_SDA / USART3_RX / TMR13_BRK | ADC1_IN22 |
| - | 18 | 23 | 31 | 49 | PF8 | I/O | FT | TMR2_CH2 / I2C2_SDA / USART7_TX | - |
| 17 | 19 | 24 | 32 | 50 | $V_{DD}$ | S | - | Digital power supply | |
| - | - | 25 | 33 | 51 | PB12 | I/O | FTa | TMR1_BRK / TMR12_BRK / I2C2_SMBA / SPI2_CS / I2S2_WS / SPI3_SCK / I2S3_CK / USART3_CK / CAN2_RX / XMC_D13 | ADC1_IN23 |
| - | - | 26 | 34 | 52 | PB13 | I/O | FTa | CLKOUT / TMR1_CH1C / TMR12_CH1C / I2C3_SMBA / SPI2_SCK / I2S2_CK / I2C3_SCL / USART3_CTS / CAN2_TX | ADC1_IN24 |
| - | - | 27 | 35 | 53 | PB14 | I/O | FTa | TMR1_CH2C / I2C3_SDA / SPI2_MISO / I2S2_MCK / I2S_SDEXT / USART3_RTS_DE / TMR12_CH1 / XMC_D0 | ADC1_IN25 |
| - | - | 28 | 36 | 54 | PB15 | I/O | FTa | ERTC_REFIN / TMR1_CH3C / TMR12_CH1C / I2C3_SCL / SPI2_MOSI / I2S2_SD / TMR12_CH2 | ADC1_IN26 / WKUP7 |
| - | - | - | - | 55 | PD8 | I/O | FT | USART3_TX / TMR12_CH2C / XMC_D13 | - |
| - | - | - | - | 56 | PD9 | I/O | FT | USART3_RX / XMC_D14 | - |
| - | - | - | - | 57 | PD10 | I/O | FT | USART3_CK / USART4_TX / XMC_D15 | - |
| - | - | - | - | 58 | PD11 | I/O | FT | I2C2_SMBA / USART3_CTS / XMC_A16 | - |
| - | - | - | - | 59 | PD12 | I/O | FTf | TMR4_CH1/ I2C2_SCL / USART3_RTS_DE / USART8_CK_RTS_DE / XMC_A17 | - |
| - | - | - | - | 60 | PD13 | I/O | FTf | TMR4_CH2/ I2C2_SDA / USART8_TX / XMC_A18 | - |
| - | - | - | - | 61 | PD14 | I/O | FT | TMR4_CH3 / I2C3_SCL / USART8_RX / XMC_D0 | - |
| | | - | - | 62 | PD15 | I/O | FT | TMR4_CH4 / I2C3_SDA / USART7_CK_RTS_DE / XMC_D1 | - |
| - | - | - | 37 | 63 | PC6 | I/O | FT | TMR1_CH1 / TMR3_CH1 / I2C1_SCL / I2S2_MCK / USART6_TX / USART7_TX / XMC_D1 | - |
| - | - | - | 38 | 64 | PC7 | I/O | FT | TMR1_CH2 / TMR3_CH2 / I2C1_SDA / SPI2_SCK / I2S2_CK / I2S3_MCK / USART6_RX / USART7_RX / XMC_NADV | - |
| - | - | - | 39 | 65 | PC8 | I/O | FT | TMR1_CH3 / TMR3_CH3 / USART8_TX / USART6_CK | - |

| Pin numbers | | | | | Pin names (function after reset) | Type (1) | GPIO level (2) | Multiplexed functions(3) | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| QFN32 | QFN36 | LQFP48/ QFN48 | LQFP64 | LQFP100 | | | | | |
| - | - | - | 40 | 66 | PC9 | I/O | FT | CLKOUT / TMR1_CH4 / TMR3_CH4 / I2C3_SDA / USART8_RX / I2C1_SDA / OTGFS1_OE | - |
| 18 | 20 | 29 | 41 | 67 | PA8 | I/O | FT | CLKOUT / TMR1_CH1 / TMR9_BRK / I2C3_SCL / USART1_CK / USART2_TX / USART7_RX / OTGFS1_SOF | - |
| 19 | 21 | 30 | 42 | 68 | PA9 | I/O | FT | CLKOUT / TMR1_CH2 / I2C3_SMBA / SPI2_SCK / I2S2_CK / USART1_TX / I2C1_SCL / TMR14_BRK / OTGFS1_VBUS | - |
| 20 | 22 | 31 | 43 | 69 | PA10 | I/O | FT | ERTC_REFIN / TMR1_CH3 / SPI2_MOSI / I2S2_SD / USART1_RX / I2C1_SDA / OTGFS1_ID | - |
| 21 | 23 | 32 | 44 | 70 | PA11 | I/O | TC | TMR1_CH4 / I2C2_SCL / SPI2_CS / I2S2_WS / I2C1_SMBA / USART1_CTS / USART6_TX / CAN1_RX | OTGFS1_D- |
| 22 | 24 | 33 | 45 | 71 | PA12 | I/O | TC | TMR1_EXT / I2C2_SDA / SPI2_MISO / I2S2_MCK / USART1_RTS_DE / USART6_RX / CAN1_TX | OTGFS1_D+ |
| 23 | 25 | 34 | 46 | 72 | PA13 (JTMS / SWDIO) | I/O | FT | PA13 / IR_OUT / I2C1_SDA / I2S_SDEXT / SPI3_MISO / I2S3_MCK / OTGFS1_OE | - |
| - | 26 | 35 | 47 | 73 | PF6 | I/O | FT | TMR2_CH1 / I2C2_SCL / USART7_RX | - |
| | - | - | - | 74 | $V_{SS}$ | S | - | Digital ground | |
| | 27 | 36 | 48 | 75 | $V_{DD}$ | S | - | Digital power supply | |
| 24 | 28 | 37 | 49 | 76 | PA14 (JTCK / SWCLK) | I/O | FT | PA14 / I2C1_SMBA / SPI3_MOSI / I2S3_SD / USART2_TX | - |
| 25 | 29 | 38 | 50 | 77 | PA15 (JTDI) | I/O | FT | PA15 / TMR2_CH1 / TMR2_EXT / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART1_TX / USART2_RX / USART7_TX / USART4_RTS_DE / XMC_NE2 | - |
| - | - | - | 51 | 78 | PC10 | I/O | FT | SPI3_SCK / I2S3_CK / USART3_TX / USART4_TX | - |
| - | - | - | 52 | 79 | PC11 | I/O | FT | I2S_SDEXT / SPI3_MISO / I2S3_MCK / USART3_RX / USART4_RX / XMC_D2 | - |
| - | - | - | 53 | 80 | PC12 | I/O | FT | TMR11_CH1 / I2C2_SDA / SPI3_MOSI / I2S3_SD / USART3_CK / USART4_CK / USART5_TX / XMC_D3 | - |
| - | - | - | - | 81 | PD0 | I/O | FT | SPI3_MOSI / I2S3_SD / SPI2_CS / I2S2_WS / USART4_RX / CAN1_RX / XMC_D2 | - |
| - | - | - | - | 82 | PD1 | I/O | FT | SPI2_SCK / I2S2_CK / SPI2_CS / I2S2_WS / USART4_TX / CAN1_TX / XMC_D3 | - |
| - | - | - | 54 | 83 | PD2 | I/O | FT | TMR3_EXT / USART3_RTS_DE / USART5_RX / XMC_NWE | - |

| Pin numbers | | | | | Pin names (function after reset) | Type (1) | GPIO level (2) | Multiplexed functions(3) | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| QFN32 | QFN36 | LQFP48/ QFN48 | LQFP64 | LQFP100 | | | | | |
| - | - | - | - | 84 | PD3 | I/O | FT | SPI2_SCK / I2S2_CK / SPI2_MISO / I2S2_MCK / USART2_CTS / XMC_CLK | - |
| - | - | - | - | 85 | PD4 | I/O | FT | SPI2_MOSI / I2S2_SD / USART2_RTS_DE / XMC_NOE | - |
| - | - | - | - | 86 | PD5 | I/O | FT | USART2_TX / XMC_NWE | - |
| - | - | - | - | 87 | PD6 | I/O | FT | SPI3_MOSI / I2S3_SD / USART2_RX / XMC_NWAIT | - |
| - | - | - | - | 88 | PD7 | I/O | FT | USART2_CK / XMC_NE1 | - |
| 26 | 30 | 39 | 55 | 89 | PB3 (JTDO) | I/O | FT | PB3 / SWO / TMR2_CH2 / I2C2_SDA / SPI1_SCK / I2S1_CK / SPI3_SCK / I2S3_CK / USART1_RX / USART1_RTS_DE / USART7_RX / USART5_TX | - |
| 27 | 31 | 40 | 56 | 90 | PB4 (NJTRST) | I/O | FT | PB4 / TMR3_CH1 / TMR11_BRK / I2C3_SDA / SPI1_MISO / I2S1_MCK / SPI3_MISO / I2S3_MCK / USART1_CTS / I2S_SDEXT / USART7_TX / USART5_RX | - |
| 28 | 32 | 41 | 57 | 91 | PB5 | I/O | FT | TMR3_CH2 / TMR10_BRK / I2C3_SMBA / SPI1_MOSI / I2S1_SD / SPI3_MOSI / I2S3_SD / USART1_CK / USART5_RX / CAN2_RX / USART5_RTS_DE | WKUP6 |
| 29 | 33 | 42 | 58 | 92 | PB6 | I/O | FT | TMR4_CH1 / TMR10_CH1C / I2C1_SCL / I2S1_MCK / SPI3_CS / I2S3_WS USART1_TX / USART5_TX / CAN2_TX / USART4_CK | - |
| 30 | 34 | 43 | 59 | 93 | PB7 | I/O | FT | TMR4_CH2 / TMR11_CH1C / I2C1_SDA / SPI3_SCK / I2S3_CK / USART1_RX / USART4_CTS / XMC_NADV | - |
| 31 | 35 | 44 | 60 | 94 | BOOT0 | I | B | Boot mode select 0 | |
| 32 | 36 | 45 | 61 | 95 | PB8 | I/O | FT | TMR2_CH1 / TMR2_EXT / TMR4_CH3 / TMR10_CH1 / I2C1_SCL / SPI3_MISO / I2S3_MCK / USART1_TX / USART5_RX / CAN1_RX | - |
| - | - | 46 | 62 | 96 | PB9 | I/O | FT | IR_OUT / TMR2_CH2 / TMR4_CH4 / TMR11_CH1 / I2C1_SDA / SPI2_CS / I2S2_WS / SPI3_MOSI / I2S3_SD / I2C2_SDA / USART5_TX / CAN1_TX / I2S1_MCK | - |
| - | - | - | - | 97 | PE0 | I/O | FT | TMR4_EXT / USART8_RX / TMR13_CH1 / XMC_LB | - |
| - | - | - | - | 98 | PE1 | I/O | FT | TMR1_CH2C / USART8_TX / TMR14_CH1 / XMC_UB | - |
| - | - | 47 | 63 | 99 | $V_{SS}$ | S | - | Digital ground | |
| 1 | 1 | 48 | 64 | 100 | $V_{DD}$ | S | - | Digital power supply | |
| - | 37 | -/49 | - | - | EPAD ($V_{SS}$) | S | - | Digital ground | |

| Pin numbers | | | | | Pin names (function after reset) | Type (1) | GPIO level (2) | Multiplexed functions(3) | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| QFN32 | QFN36 | LQFP48/ QFN48 | LQFP64 | LQFP100 | | | | | |
| 33 | - | - | - | - | EPAD ($V_{SS}$/$V_{SSA}$) | S | - | Digital ground / Analog ground | |

(1) I = input, O = output, S = power supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. Of those, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when analog mode. In this case, its input level should not be higher than VDD + 0.3 V.

(3) Function availability depend on the selected product part number. Any of GPIOs has EVENTOUT feature.

(4) PC13, PC14, and PC15 are supplied through power switch. Since the switch only drives a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited not to be used as a current source (e.g. to drive an LED).

(5) There are limitations to the use of PC13 and its additional functions. See AT32A423 Errata sheet for details.

(6) PA0, PA1, PC0, PC1, PC2 and PC3 represent fast ADC channel, others slow ADC channels.

# 4 Electrical characteristics

## 4.1 Test conditions

### 4.1.1 Minimum and maximum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

### 4.1.2 Typical values

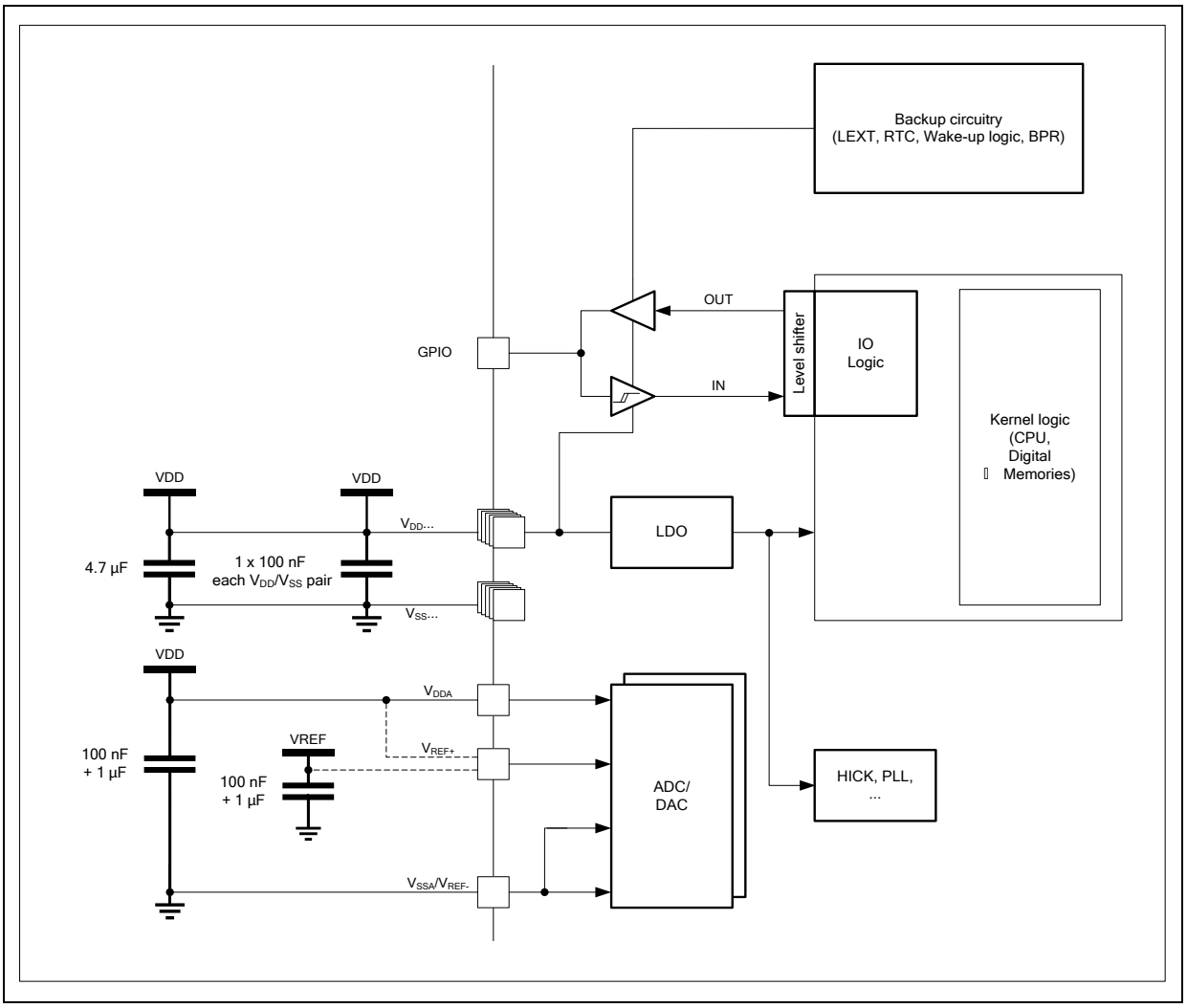
Typical values are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.

### 4.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

### 4.1.4 Power supply scheme

**Figure 7. Power supply scheme**



## 4.2 Absolute maximum values

### 4.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 7*, *Table 8* and *Table 9*, it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

**Table 7. Voltage characteristics**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DDx}$-$V_{SS}$ | External main supply voltage | -0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT and FTf GPIO | $V_{SS}$-0.3 | 6.0 | |
| | Input voltage on FTa GPIO (set as input floating, input pull-up, or input pull-down mode) | | | |
| | Input voltage on TC GPIO | $V_{SS}$-0.3 | 4.0 | |
| | Input voltage on FTa GPIO (set as analog mode) | | | |
| $\|\Delta V_{DDx}\|$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\|V_{SSx}$-$V_{SS}\|$ | Variations between all the different ground pins | - | 50 | |

**Table 8. Current characteristics**

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (source) | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink) | 150 | |
| $I_{IO}$ | Output current sunk by any GPIO and control pin | 25 | |
| | Output current source by any GPIO and control pin | -25 | |

**Table 9. Temperature characteristics**

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -60 ~ +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | |

### 4.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharge is applied to all device pins. This test is compliant with the AEC-Q100-002-REV-E-2013 and AEC-Q100-011-REV-D-2019 standards.

**Table 10. ESD values**

| Symbol | Parameter | Conditions | Class | Min | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforms to AEC-Q100-002-REV-E-2013 | 3A | ±4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforms to AEC-Q100-011-REV-D-2019 | C2B | ±750 | |

**Static latch-up**

Tests compliant with AEC-Q100-004-REV-D-2012 latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

**Table 11. Latch-up values**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C, conforms to AEC-Q100-004-REV-D-2012 | II level A (±200 mA) |

# 4.3 Specifications

## 4.3.1 General operating conditions

**Table 12. General operating conditions**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | LDO voltage | 1.3 V | 0 | 150 | MHz |
| | | | 1.2 V | 0 | 120 | |
| | | | 1.0 V | 0 | 64 | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | LDO voltage | 1.3 V | 0 | 120 | MHz |
| | | | 1.2 V, 1.0 V | 0 | $f_{HCLK}$ | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | | 0 | $f_{HCLK}$ | MHz |
| $V_{DD}$ | Digital operating voltage | - | | 2.4 | 3.6 | V |
| $V_{DDA}$ | Analog operating voltage | Must be the same potential as $V_{DD}$ | | $V_{DD}$ | | V |
| $P_D$ | Power dissipation: $T_A$ = 105 °C | LQFP100 – 14 x 14 mm | | - | 264 | mW |
| | | LQFP64 – 10 x 10 mm | | - | 238 | |
| | | LQFP64 – 7 x 7 mm | | - | 216 | |
| | | LQFP48 – 7 x 7 mm | | - | 216 | |
| | | QFN48 – 6 x 6 mm | | - | 350 | |
| | | QFN36 – 6 x 6 mm | | - | 350 | |
| | | QFN32 – 4 x 4 mm | | - | 280 | |
| $T_A$ | Ambient temperature | - | | -40 | 105 | °C |

## 4.3.2 Operating conditions at power-up / power-down

**Table 13. Operating conditions at power-up/power-down**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 0 | ∞(1) | ms/V |
| | $V_{DD}$ fall time rate | 20 | ∞ | μs/V |

(1) When $V_{DD}$ rise time rate is lower than 1.3 ms/V, it is necessary for code to wait 60 ms until the $V_{DD}$ is higher than 2.57 V before accessing battery powered domain registers. Refer to AT32A423 errata sheet for details.

## 4.3.3 Embedded reset and power control block characteristics

**Table 14. Embedded reset characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{POR}$ | Power on reset threshold | 1.81 | 2.1 | 2.4 | V |
| $V_{LVR}$ | Low voltage reset threshold | 1.68(2) | 1.9 | 2.08 | V |
| $V_{LVRhyst}$ | LVR hysteresis | - | 180 | - | mV |
| $T_{RESTTEMPO}$ | Reset temporization: CPU starts execution after $V_{DD}$ keeps higher than $V_{POR}$ for $T_{RESTTEMPO}$ | - | 3.5 | - | ms |

(1) Obtained by characterization results, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum $V_{LVR}$ value.

**Figure 8. Power on reset and low voltage reset waveform**

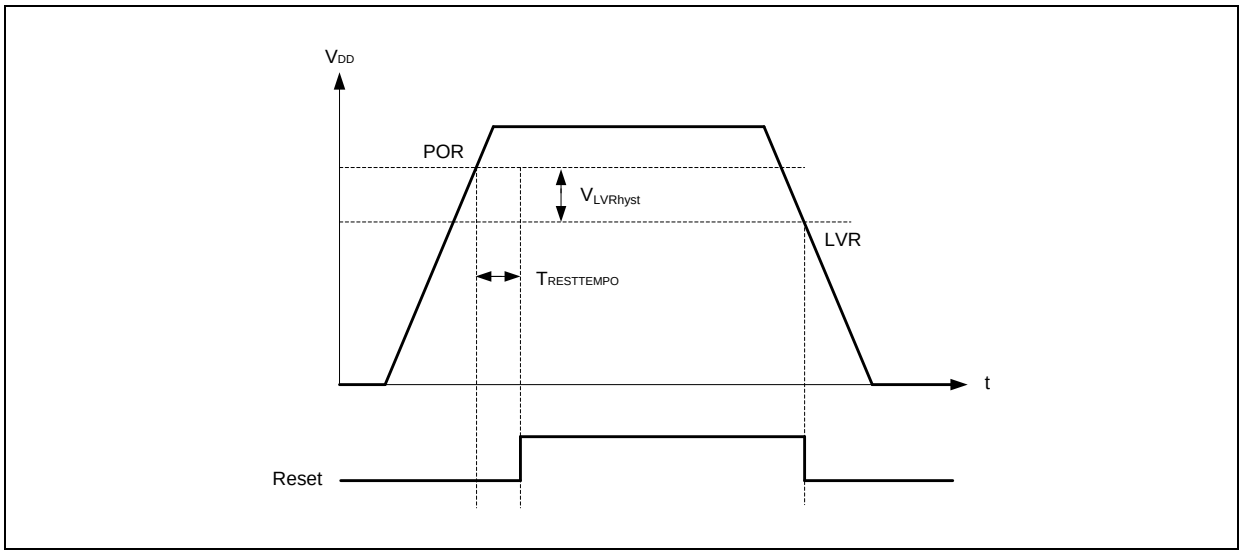



**Table 15. Programmable voltage monitoring characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVM1}$ | PVM threshold 1 (PVMSEL[2:0] = 001) | Rising edge(1) | 2.19 | 2.28 | 2.37 | V |
| | | Falling edge(1) | 2.09 | 2.18 | 2.27 | V |
| $V_{PVM2}$ | PVM threshold 2 (PVMSEL[2:0] = 010) | Rising edge(1) | 2.28 | 2.38 | 2.48 | V |
| | | Falling edge(1) | 2.18 | 2.28 | 2.38 | V |
| $V_{PVM3}$ | PVM threshold 3 (PVMSEL[2:0] = 011) | Rising edge(1) | 2.38 | 2.48 | 2.58 | V |
| | | Falling edge(1) | 2.28 | 2.38 | 2.48 | V |
| $V_{PVM4}$ | PVM threshold 4 (PVMSEL[2:0] = 100) | Rising edge(1) | 2.47 | 2.58 | 2.69 | V |
| | | Falling edge(1) | 2.37 | 2.48 | 2.59 | V |
| $V_{PVM5}$ | PVM threshold 5 (PVMSEL[2:0] = 101) | Rising edge(1) | 2.57 | 2.68 | 2.79 | V |
| | | Falling edge(1) | 2.47 | 2.58 | 2.69 | V |
| $V_{PVM6}$ | PVM threshold 6 (PVMSEL[2:0] = 110) | Rising edge(1) | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge(1) | 2.56 | 2.68 | 2.8 | V |
| $V_{PVM7}$ | PVM threshold 7 (PVMSEL[2:0] = 111) | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| $V_{HYS\_P}$(1) | PVM hysteresis | - | - | 100 | - | mV |
| $I_{DD\ (PVM)}$(1) | PVM current dissipation | - | - | 20 | 30 | µA |

(1) Obtained by characterization results, not tested in production.

## 4.3.4 Memory characteristics

**Table 16. Internal Flash memory characteristics(1)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{PROG}$ | Programming time | - | 40 | 42 | µs |
| $t_{SE}$ | Sector erase time (2 KB) | AT32A423xC | 13.2 | 16 | ms |
| | Sector erase time (1 KB) | AT32A423xB<br>AT32A423x8 | 6.6 | 8 | |
| $t_{ME}$ | Mass erase time | - | 8.2 | 10 | ms |

(1) Guaranteed by design, not tested in production.

**Table 17. Internal Flash memory endurance and data retention(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = -40 ~ 105 °C | 100 | - | - | kcycles |
| $t_{RET}$ | Data retention | $T_A$ = 105 °C | 10 | - | - | year |

(1) Guaranteed by design, not tested in production.

### 4.3.5 Supply current characteristics

The current consumption, obtained by characterization results and not tested in production, is subject to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code.

**Typical and maximum current consumption**

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on the $f_{HCLK}$ frequency (0 ~ 32 MHz: zero-wait state; 33 ~ 64 MHz: one wait state; 65 ~ 96 MHz: two wait states; 97 ~ 128 MHz: three wait states; 129 MHz and above: four wait states)
- Prefetch ON
- When peripherals are enabled:
  - If $f_{HCLK} > 120$ MHz, then $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/2$
  - If $f_{HCLK} \leq 120$ MHz, then $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/2$
- Unless otherwise specified, the typical values are measured with $V_{DD}$ = 3.3 V and $T_A$ = 25 °C condition, and the maximum values are measured with $V_{DD}$ = 3.6 V.

**Table 18. Typical current consumption in Run mode**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | LDO voltage (V) | Typ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode | High speed external crystal (HEXT)(1)(2) | 150 MHz | 1.3 | 38.4 | 16.8 | mA |
| | | | 120 MHz | 1.2 | 33.5 | 13.2 | |
| | | | 108 MHz | 1.2 | 30.2 | 12.0 | |
| | | | 72 MHz | 1.2 | 20.4 | 8.22 | |
| | | | 64 MHz | 1.0 | 15.3 | 6.29 | |
| | | | 48 MHz | 1.0 | 11.9 | 5.18 | |
| | | | 36 MHz | 1.0 | 9.13 | 4.07 | |
| | | | 24 MHz | 1.0 | 6.60 | 3.22 | |
| | | | 16 MHz | 1.0 | 4.64 | 2.39 | |
| | | | 8 MHz | 1.0 | 2.44 | 1.28 | |
| | | | 4 MHz | 1.0 | 1.62 | 0.99 | |
| | | | 2 MHz | 1.0 | 1.21 | 0.85 | |
| | | | 1 MHz | 1.0 | 1.01 | 0.78 | |
| | | High speed internal clock (HICK) (2) | 150 MHz | 1.3 | 38.4 | 16.8 | mA |
| | | | 120 MHz | 1.2 | 33.4 | 13.1 | |
| | | | 108 MHz | 1.2 | 30.1 | 11.9 | |
| | | | 72 MHz | 1.2 | 20.3 | 8.09 | |
| | | | 64 MHz | 1.0 | 15.2 | 6.15 | |
| | | | 48 MHz | 1.0 | 11.8 | 5.03 | |
| | | | 36 MHz | 1.0 | 9.02 | 3.92 | |
| | | | 24 MHz | 1.0 | 6.46 | 3.08 | |
| | | | 16 MHz | 1.0 | 4.50 | 2.23 | |
| | | | 8 MHz | 1.0 | 2.30 | 1.11 | |
| | | | 4 MHz | 1.0 | 1.47 | 0.84 | |
| | | | 2 MHz | 1.0 | 1.05 | 0.69 | |
| | | | 1 MHz | 1.0 | 0.85 | 0.62 | |

(1) External clock is 8 MHz.
(2) PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 19. Typical current consumption in Sleep mode**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | LDO voltage (V) | Typ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$ | Supply current in sleep mode | High speed external crystal (HEXT)(1)(2) | 150 MHz | 1.3 | 31.5 | 6.14 | mA |
| | | | 120 MHz | 1.2 | 27.0 | 5.18 | |
| | | | 108 MHz | 1.2 | 24.3 | 4.74 | |
| | | | 72 MHz | 1.2 | 16.5 | 3.42 | |
| | | | 64 MHz | 1.0 | 12.4 | 2.69 | |
| | | | 48 MHz | 1.0 | 9.73 | 2.47 | |
| | | | 36 MHz | 1.0 | 7.47 | 2.03 | |
| | | | 24 MHz | 1.0 | 5.50 | 1.87 | |
| | | | 16 MHz | 1.0 | 3.90 | 1.49 | |
| | | | 8 MHz | 1.0 | 2.08 | 0.83 | |
| | | | 4 MHz | 1.0 | 1.44 | 0.77 | |
| | | | 2 MHz | 1.0 | 1.12 | 0.74 | |
| | | | 1 MHz | 1.0 | 0.96 | 0.72 | |
| | | High speed internal clock (HICK) (2) | 150 MHz | 1.3 | 31.5 | 6.13 | mA |
| | | | 120 MHz | 1.2 | 26.9 | 5.05 | |
| | | | 108 MHz | 1.2 | 24.2 | 4.61 | |
| | | | 72 MHz | 1.2 | 16.4 | 3.28 | |
| | | | 64 MHz | 1.0 | 12.2 | 2.53 | |
| | | | 48 MHz | 1.0 | 9.59 | 2.32 | |
| | | | 36 MHz | 1.0 | 7.35 | 1.88 | |
| | | | 24 MHz | 1.0 | 5.35 | 1.72 | |
| | | | 16 MHz | 1.0 | 3.75 | 1.33 | |
| | | | 8 MHz | 1.0 | 1.93 | 0.67 | |
| | | | 4 MHz | 1.0 | 1.29 | 0.61 | |
| | | | 2 MHz | 1.0 | 0.97 | 0.58 | |
| | | | 1 MHz | 1.0 | 0.81 | 0.56 | |

(1) External clock is 8 MHz.
(2) PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 20. Maximum current consumption in Run mode**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | LDO voltage (V) | Max | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | High speed external crystal (HEXT)(1), all peripherals enabled | 150 MHz | 1.3 | 40.6 | 42.7 | mA |
| | | | 120 MHz | 1.2 | 34.4 | 35.2 | |
| | | | 108 MHz | 1.2 | 31.1 | 31.9 | |
| | | | 72 MHz | 1.2 | 21.2 | 22.0 | |
| | | | 64 MHz | 1.0 | 15.8 | 16.4 | |
| | | | 48 MHz | 1.0 | 12.5 | 13.0 | |
| | | | 36 MHz | 1.0 | 9.64 | 10.2 | |
| | | | 24 MHz | 1.0 | 7.11 | 7.61 | |
| | | | 16 MHz | 1.0 | 5.14 | 5.64 | |
| | | | 8 MHz | 1.0 | 3.02 | 3.54 | |
| | | High speed external crystal (HEXT)(1), all peripherals disabled | 150 MHz | 1.3 | 18.8 | 19.6 | mA |
| | | | 120 MHz | 1.2 | 13.9 | 14.6 | |
| | | | 108 MHz | 1.2 | 12.7 | 13.4 | |
| | | | 72 MHz | 1.2 | 8.91 | 9.60 | |
| | | | 64 MHz | 1.0 | 6.78 | 7.28 | |
| | | | 48 MHz | 1.0 | 5.66 | 6.16 | |
| | | | 36 MHz | 1.0 | 4.55 | 5.04 | |
| | | | 24 MHz | 1.0 | 3.71 | 4.21 | |
| | | | 16 MHz | 1.0 | 2.88 | 3.37 | |
| | | | 8 MHz | 1.0 | 1.77 | 2.26 | |

(1) External clock is 8 MHz, and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 21. Maximum current consumption in Sleep mode**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | LDO voltage (V) | Max | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | High speed external crystal (HEXT)(1), all peripherals enabled | 150 MHz | 1.3 | 32.8 | 34.8 | mA |
| | | | 120 MHz | 1.2 | 27.8 | 28.7 | |
| | | | 108 MHz | 1.2 | 25.2 | 26.0 | |
| | | | 72 MHz | 1.2 | 17.3 | 18.0 | |
| | | | 64 MHz | 1.0 | 12.9 | 13.4 | |
| | | | 48 MHz | 1.0 | 10.3 | 10.8 | |
| | | | 36 MHz | 1.0 | 7.99 | 8.49 | |
| | | | 24 MHz | 1.0 | 6.00 | 6.51 | |
| | | | 16 MHz | 1.0 | 4.40 | 4.90 | |
| | | | 8 MHz | 1.0 | 2.66 | 3.17 | |
| | | High speed external crystal (HEXT)(1), all peripherals disabled | 150 MHz | 1.3 | 6.97 | 7.56 | mA |
| | | | 120 MHz | 1.2 | 5.87 | 6.56 | |
| | | | 108 MHz | 1.2 | 5.43 | 6.11 | |
| | | | 72 MHz | 1.2 | 4.10 | 4.77 | |
| | | | 64 MHz | 1.0 | 3.19 | 3.68 | |
| | | | 48 MHz | 1.0 | 2.97 | 3.46 | |
| | | | 36 MHz | 1.0 | 2.53 | 3.02 | |
| | | | 24 MHz | 1.0 | 2.37 | 2.86 | |
| | | | 16 MHz | 1.0 | 1.98 | 2.47 | |
| | | | 8 MHz | 1.0 | 1.32 | 1.81 | |

(1) External clock is 8 MHz, and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 22. Typical and maximum current consumptions in Deepsleep and Standby modes**

| Symbol | Parameter | Conditions | Typ(1) | | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ = 2.4 V | $V_{DD}$ = 3.3 V | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Deepsleep mode | LDO in Run mode, HICK and HEXT OFF, WDT OFF | 281 | 286 | 330 | 910 | 1540 | µA |
| | | LDO in low-power mode, HICK and HEXT OFF, WDT OFF | 141 | 143 | 160 | 550 | 980 | |
| | Supply current in Standby mode | LEXT and ERTC OFF | 2.6 | 3.9 | 5.0 | 6.8 | 8.1 | µA |
| | | LEXT and ERTC ON | 3.6 | 5.4 | 6.5 | 8.8 | 12.9 | |

(1) Typical values are measured at $T_A$ = 25 °C.
(2) Obtained by characterization results, not tested in production.

**Figure 9. Typical current consumption in Deepsleep mode with LDO in run mode vs. temperature at different $V_{DD}$**

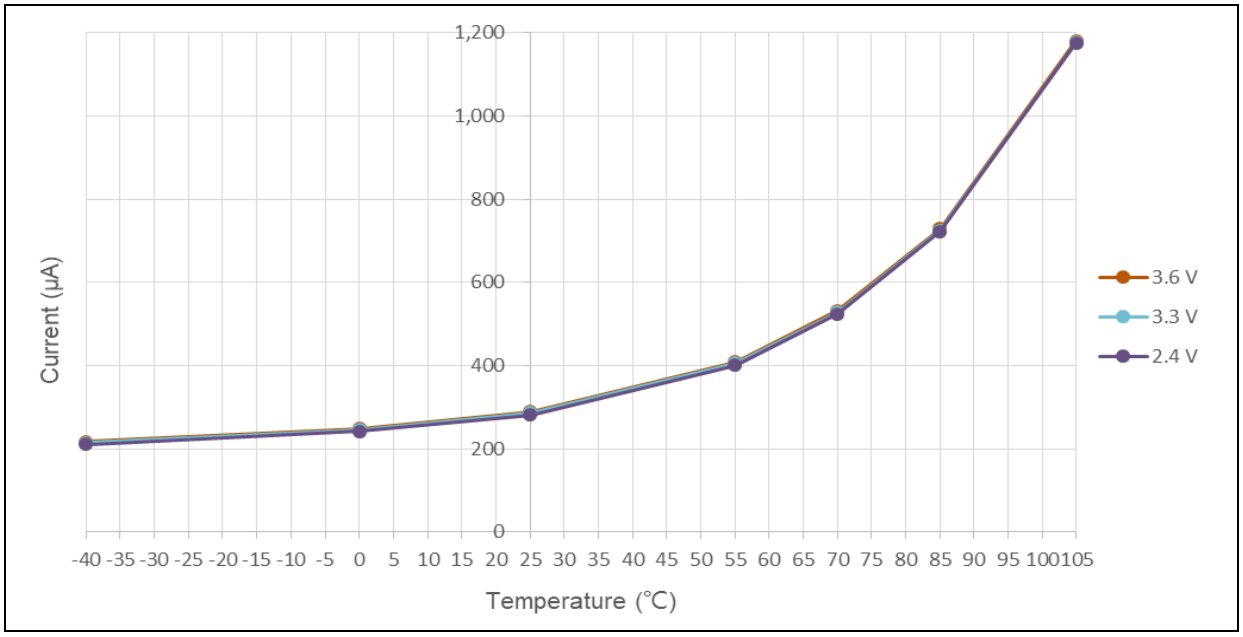


**Figure 10. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different $V_{DD}$**

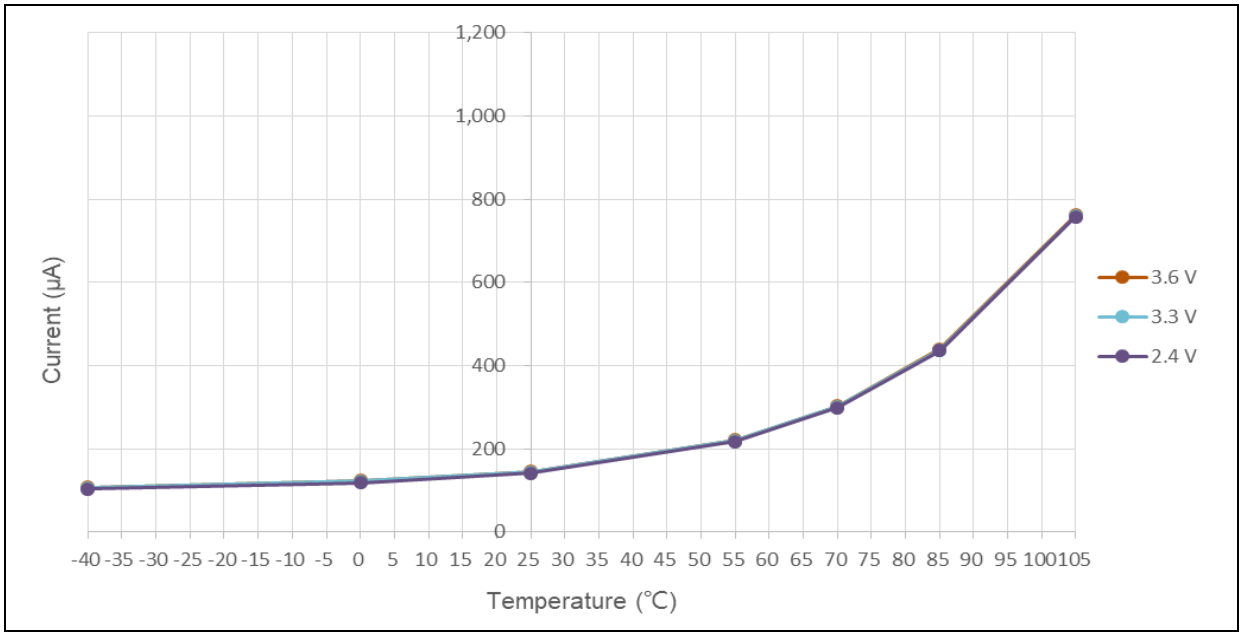
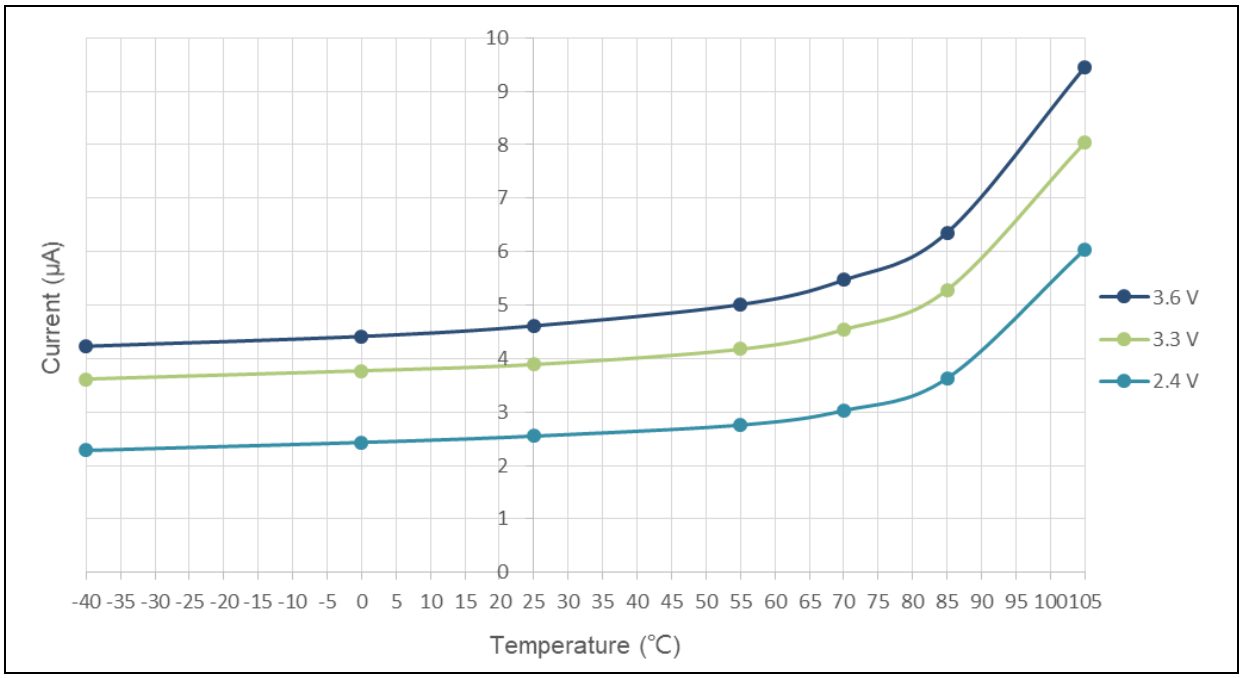



**Figure 11. Typical current consumption in Standby mode vs. temperature at different $V_{DD}$**




**On-chip peripheral current consumption**

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

**Table 23. Peripheral current consumption**

| Peripheral | | LDO voltage (V) | | | Unit |
|---|---|---|---|---|---|
| | | 1.3 | 1.2 | 1.0 | |
| AHB | DMA1 | 4.38 | 3.98 | 3.29 | μA/MHz |
| | DMA2 | 4.30 | 3.91 | 3.25 | |
| | SRAM | 1.02 | 0.93 | 0.77 | |
| | Flash | 12.47 | 11.25 | 9.58 | |
| | GPIOA | 0.75 | 0.68 | 0.56 | |
| | GPIOB | 0.72 | 0.66 | 0.54 | |
| | GPIOC | 0.74 | 0.68 | 0.56 | |
| | GPIOD | 0.67 | 0.61 | 0.50 | |
| | GPIOE | 0.69 | 0.62 | 0.52 | |
| | GPIOF | 0.76 | 0.71 | 0.58 | |
| | XMC | 5.31 | 4.82 | 3.98 | |
| | CRC | 0.51 | 0.47 | 0.39 | |
| | OTGFS1 | 25.34 | 23.04 | 19.14 | |
| APB1 | TMR2 | 9.98 | 9.12 | 7.62 | μA/MHz |
| | TMR3 | 7.10 | 6.49 | 5.41 | |
| | TMR4 | 7.12 | 6.49 | 5.40 | |
| | TMR6 | 0.85 | 0.78 | 0.66 | |
| | TMR7 | 0.84 | 0.77 | 0.64 | |
| | TMR12 | 6.89 | 6.27 | 5.22 | |
| | TMR13 | 4.19 | 3.82 | 3.17 | |
| | TMR14 | 4.26 | 3.89 | 3.21 | |
| | WWDT | 0.51 | 0.46 | 0.38 | |
| | SPI2/$I^2S2$ | 3.10 | 2.83 | 2.35 | |
| | SPI3/$I^2S3$ | 3.60 | 3.28 | 2.72 | |
| | USART2 | 5.30 | 4.86 | 4.04 | |
| | USART3 | 5.21 | 4.76 | 3.97 | |
| | USART4 | 2.68 | 2.45 | 2.03 | |
| | USART5 | 2.65 | 2.40 | 1.99 | |
| | $I^2C1$ | 6.67 | 6.09 | 5.08 | |
| | $I^2C2$ | 6.44 | 5.90 | 4.93 | |
| | $I^2C3$ | 6.57 | 5.99 | 4.97 | |
| | CAN1 | 3.05 | 2.77 | 2.31 | |
| | CAN2 | 2.53 | 2.31 | 1.93 | |
| | PWC | 0.89 | 0.83 | 0.69 | |
| | DAC | 3.67 | 1.90 | 1.56 | |
| | USART7 | 2.63 | 2.42 | 1.98 | |
| | USART8 | 2.64 | 2.42 | 1.99 | |

| Peripheral | | LDO voltage (V) | | | Unit |
|---|---|---|---|---|---|
| | | 1.3 | 1.2 | 1.0 | |
| APB2 | TMR1 | 10.14 | 9.26 | 7.73 | μA/MHz |
| | USART1 | 5.11 | 4.66 | 3.88 | |
| | USART6 | 2.72 | 2.48 | 2.06 | |
| | ADC1 | 9.12 | 8.33 | 6.93 | |
| | SPI1/I$^2$S1 | 3.23 | 2.97 | 2.48 | |
| | SCFG | 0.22 | 0.21 | 0.18 | |
| | TMR9 | 6.16 | 5.64 | 4.69 | |
| | TMR10 | 3.85 | 3.52 | 2.94 | |
| | TMR11 | 4.13 | 3.77 | 3.13 | |
| | ACC | 0.28 | 0.26 | 0.23 | |

## 4.3.6 External clock source characteristics

**High-speed external clock generated from a crystal / ceramic resonator**

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

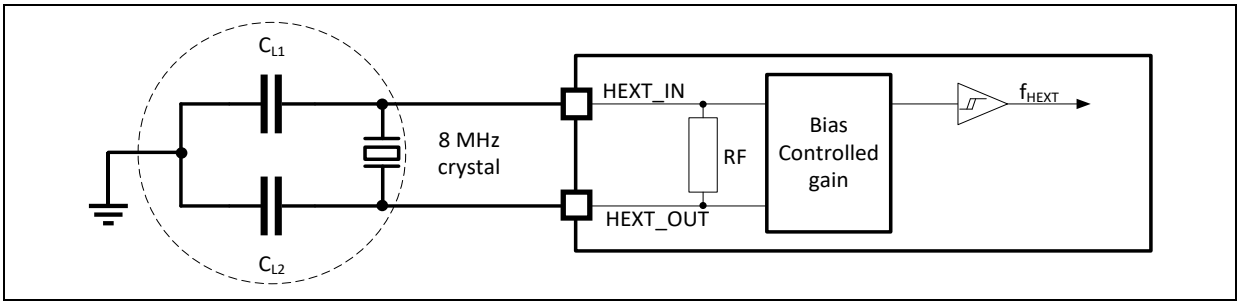
**Table 24. HEXT 4 ~ 25 MHz crystal characteristics (1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HEXT\_IN}$ | Oscillator frequency | - | 4 | 8 | 25 | MHz |
| $t_{SU(HEXT)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Obtained by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough estimate of the combined pin and board capacitance) when selecting $C_{L1}$ and $C_{L2}$.

**Figure 12. HEXT typical application with an 8 MHz crystal**



### High-speed external clock generated from an external source

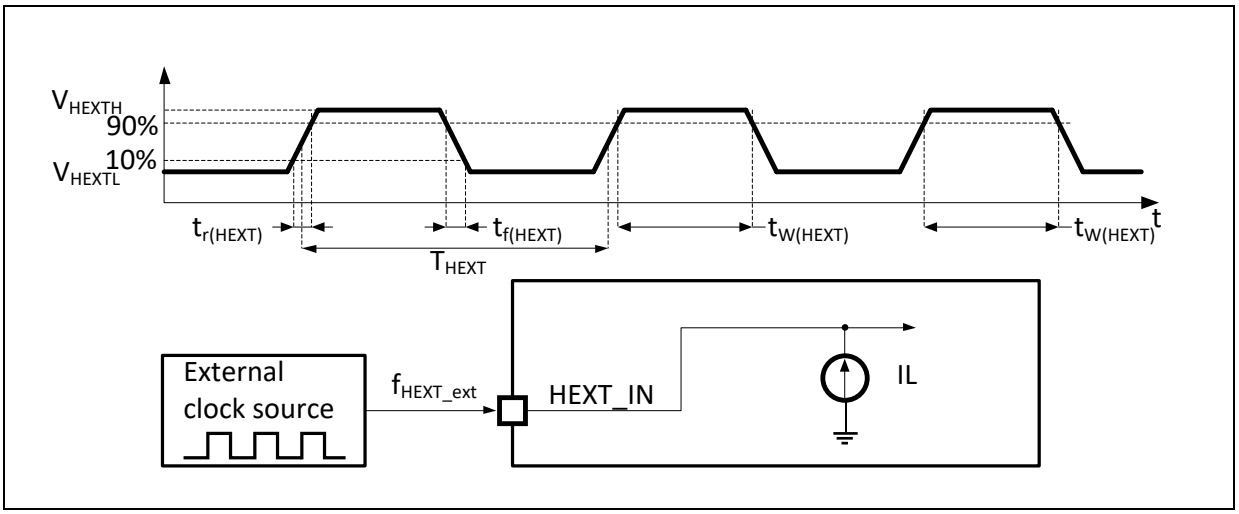
The characteristics given in the table below come from tests performed using a high-speed external clock source.

**Table 25. HEXT external source characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HEXT\_ext}$ | User external clock source frequency (1) | - | 1 | 8 | 25 | MHz |
| $V_{HEXTH}$ | HEXT_IN input pin high level voltage | | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HEXTL}$ | HEXT_IN input pin low level voltage | | $V_{SS}$ | - | 0.3$V_{DD}$ | |
| $t_{w(HEXT)}$ $t_{w(HEXT)}$ | HEXT_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HEXT)}$ $t_{f(HEXT)}$ | HEXT_IN rise or fall time(1) | | - | - | 20 | |
| $C_{in(HEXT)}$ | HEXT_IN input capacitance (1) | - | - | 5 | - | pF |
| $Duty_{(HEXT)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | HEXT_IN input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1 | μA |

(1) Guaranteed by design, not tested in production.

**Figure 13. High-speed external source AC timing diagram**



### Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 26. LEXT 32.768 kHz crystal characteristics (1)(2)**

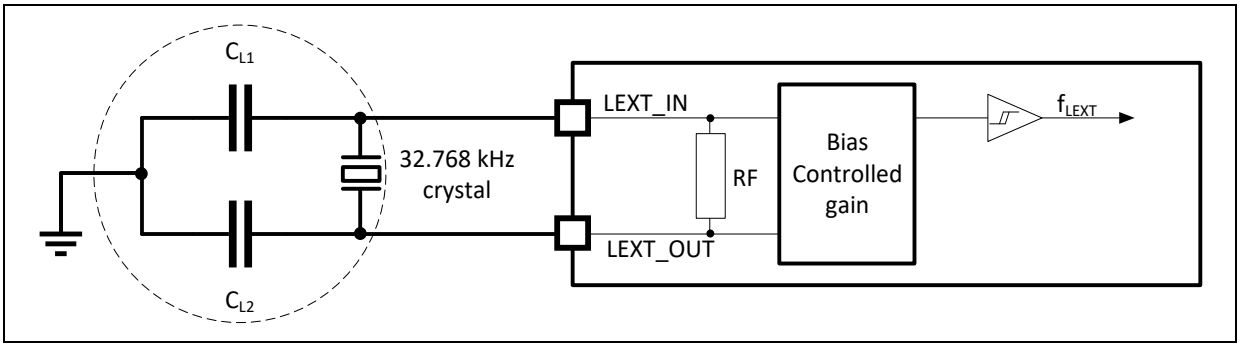
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SU(LEXT)}$ | Startup time | $V_{DD}$ is stabilized | - | 200 | - | ms |

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Obtained by characterization results, not tested in production.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range and select to meet the requirements of the crystal or resonator. $C_{L1}$ and $C_{L2}$, are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of $C_{L1}$ and $C_{L2}$.

Load capacitance $C_L$ is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where $C_{stray}$ is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

**Figure 14. LEXT typical application with a 32.768 kHz crystal**




*Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.*

### Low-speed external clock generated from an external source

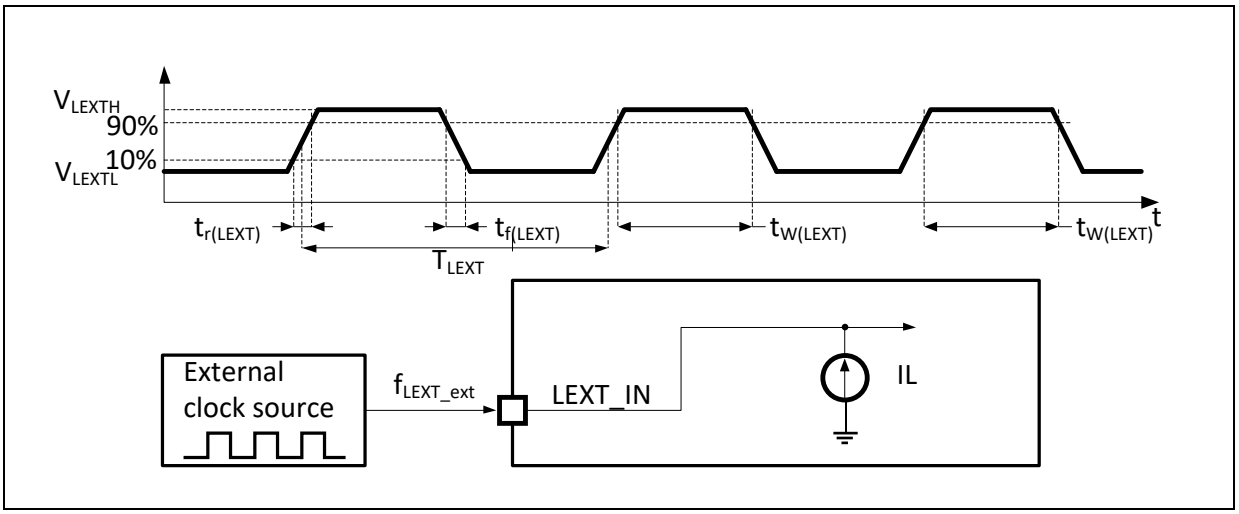
The characteristics given in the table below come from tests performed using a low-speed external clock source.

**Table 27. LEXT external source characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LEXT\_ext}$ | User External clock source frequency (1) | - | - | 32.768 | 1000 | kHz |
| $V_{LEXTH}$ | LEXT_IN input pin high level voltage | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LEXTL}$ | LEXT_IN input pin low level voltage | - | $V_{SS}$ | - | $0.3V_{DD}$ | V |
| $t_{w(LEXT)}$ $t_{w(LEXT)}$ | LEXT_IN high or low time (1) | - | 450 | - | - | ns |
| $t_{r(LEXT)}$ $t_{f(LEXT)}$ | LEXT_IN rise or fall time (1) | - | - | - | 50 | ns |
| $C_{in(LEXT)}$ | LEXT_IN input capacitance(1) | - | - | 5 | - | pF |
| $Duty_{(LEXT)}$ | Duty cycle | - | 30 | - | 70 | % |
| $I_L$ | LEXT_IN input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1 | µA |

(1) Guaranteed by design, not tested in production.

**Figure 15. Low-speed external source AC timing diagram**



## 4.3.7 Internal clock source characteristics

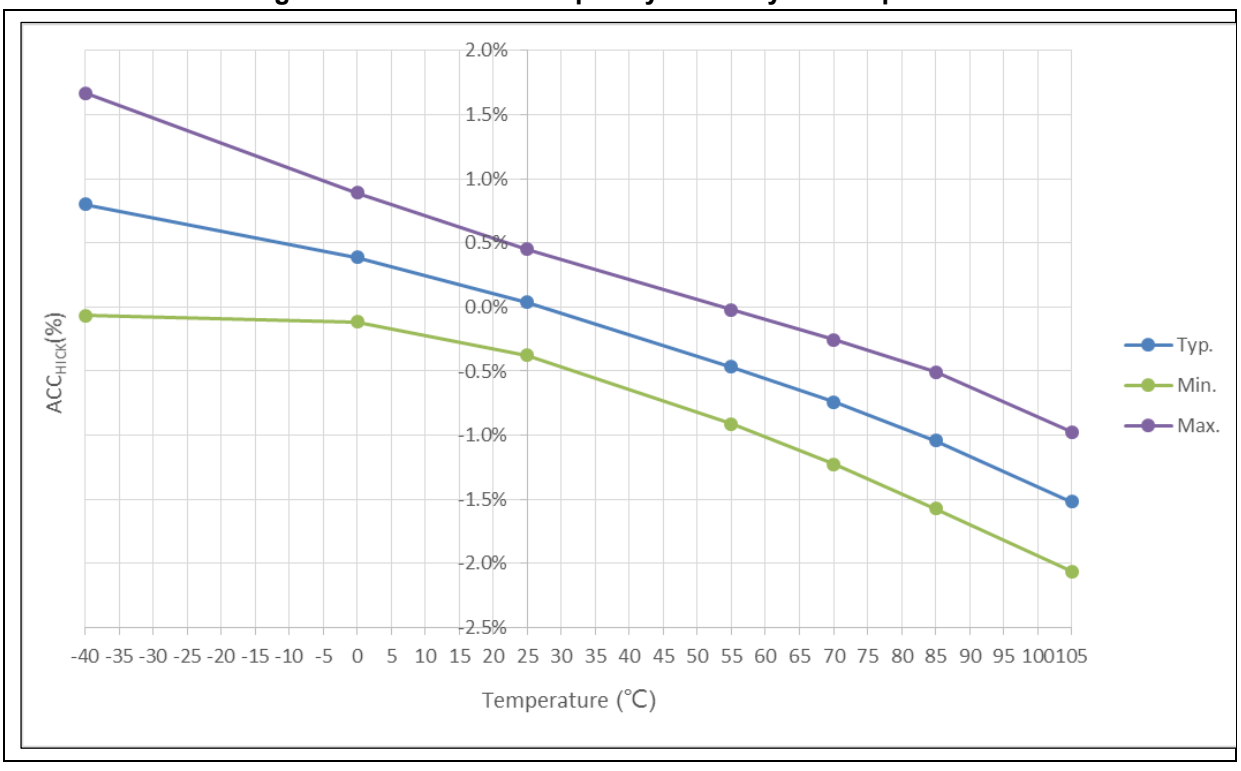
### High-speed internal clock (HICK)

**Table 28. HICK clock characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HICK}$ | Frequency | - | | - | 48 | - | MHz |
| $DuCy_{(HICK)}$ | Duty cycle | - | | 45 | - | 55 | % |
| $ACC_{HICK}$ | HICK clock accuracy | User-trimmed with the CRM_CTRL register (1) | | -1 | - | 1 | % |
| | | ACC-trimmed(1) | | -0.25 | - | 0.25 | |
| | | Factory-calibrated (2) | $T_A$ = -40 ~ 105 °C | -2.5 | - | 2.5 | |
| | | | $T_A$ = -40 ~ 85 °C | -2 | - | 2 | |
| | | | $T_A$ = 0 ~ 70 °C | -1.5 | - | 1.5 | |
| | | | $T_A$ = 25 °C | -1 | 0.5 | 1 | |
| $t_{SU(HICK)}$(2) | HICK clock startup time | - | | - | - | 10.5 | µs |
| $I_{DD(HICK)}$(2) | HICK clock power consumption | - | | - | 300 | 330 | µA |

(1) Guaranteed by design, not tested in production.
(2) Obtained by characterization results, not tested in production.

**Figure 16. HICK clock frequency accuracy vs. temperature**




### Low-speed internal clock (LICK)

**Table 29. LICK clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LICK}$(1) | Frequency | - | 25 | 35 | 45 | kHz |

(1) Obtained by characterization results, not tested in production.

### 4.3.8 PLL characteristics

**Table 30. PLL characteristics**

| Symbol | Parameter | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock (2) | 2 | 8 | 16 | MHz |
| | PLL input clock duty cycle | 40 | - | 60 | % |
| $f_{PLL\_OUT}$(3) | PLL multiplier output clock | 32 | - | 300 | MHz |
| $t_{LOCK}$ | PLL lock time | - | - | 200 | µs |
| Jitter | Cycle-to-cycle jitter | - | - | 300 | ps |

(1) Guaranteed by design, not tested in production.
(2) Use the appropriate multiplier factor to ensure that PLL input clock values are compatible with the range defined by $f_{PLL\_OUT}$.
(3) PLL/2 (divided by 2) is used as clock source of system clock. Refer to AT32A423 Reference Manual for details.

### 4.3.9 Wakeup time from low-power mode

The wakeup times given in the table below are measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK.

**Table 31. Low-power mode wakeup time**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | - | 3.7 | µs |
| $t_{WUDEEPSLEEP}$ | Wakeup from Deepsleep mode | LDO in Run mode | 450 | µs |
| | | LDO in low-power mode | 500 | |
| $t_{WUSTDBY}$ | Wakeup from Standby mode | - | 800 | µs |

### 4.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

**Functional EMS (electromagnetic susceptibility)**

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

**Table 32. EMS characteristics**

| Symb | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{EFT}$ | Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on $V_{DD}$ and $V_{SS}$ pins to induce a functional error. Both $V_{DD}$ and $V_{SS}$ have a 47 µF capacitor on their entries. Each $V_{DD}$ and $V_{SS}$ pair has an 0.1 µF bypass capacitor. | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 150 MHz, LDO 1.3 V. Conforms to IEC 61000-4-4 | 4A (±4 kV) |
| | | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 120 MHz, LDO 1.2 V. Conforms to IEC 61000-4-4 | |
| | | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 64 MHz, LDO 1.0 V Conforms to IEC 61000-4-4 | |

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

**Electromagnetic interference (EMI)**

The electromagnetic field emitted by the device is monitored while a Coremark program is running and outputting 20 kHz square wave through two GPIO pins (no load outside the device). This emission test is compliant with SAE J1752/3 standard.

**Table 33. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max. | Unit |
|---|---|---|---|---|---|
| $S_{EMI}$ | Peak value | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HICK}/f_{HCLK}$ = 8/150 MHz, LDO 1.3 V | 0.15 MHz ~ 30 MHz | 16.1 | dBµV |
| | | | 30 MHz ~ 130 MHz | < 0 | |
| | | | 130 MHz ~ 1 GHz | < 0 | |
| | Level | - | - | M11 | - |

## 4.3.11 GPIO port characteristics

**General input/output characteristics**

All GPIOs are CMOS and TTL compliant.

**Table 34. GPIO static characteristics**

| Symb | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | GPIO input low level voltage | - | -0.3 | - | 0.28 x $V_{DD}$ + 0.1 | V |
| $V_{IH}$ | TC GPIO input high level voltage | - | 0.31 x $V_{DD}$ + 0.8 | - | $V_{DD}$ + 0.3 | V |
| | FTa GPIO input high level voltage | Analog mode | | | | |
| | FT and FTf GPIO input high level voltage | - | | - | 5.5 | |
| | FTa GPIO input high level voltage | Input floating, input pull-up, or input pull-down mode | | | | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis(1) | - | 200 | - | - | mV |
| | | | 5% $V_{DD}$ | - | - | - |
| $I_{lkg}$ | Input leakage current (2) | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ TC GPIOs | - | - | ±1 | µA |
| | | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ ≤ $V_{IN}$ ≤ 5.5 V FT, FTa and FTf GPIOs | - | - | ±1 | |
| $R_{PU}$ | Weak pull-up equivalent resistor | $V_{IN}$ = $V_{SS}$ | 65 | 80 | 130 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor (3) | $V_{IN}$ = $V_{DD}$ | 65 | 70 | 130 | kΩ |
| $C_{IO}$ | GPIO pin capacitance | - | - | 9 | - | pF |

(1) Hysteresis voltage between Schmitt trigger switching levels. Obtained by characterization results, not tested in production.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.

(3) When the input is higher than $V_{DD}$ + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT, FTf and FTa pins.
(4) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

**Output driving current**

In the user application, the number of GPIO pins that can drive current must be controlled to respect the absolute maximum rating defined in *Section 4.2.1*

- The sum of the currents sourced by all GPIOs on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 8*).
- The sum of the currents sunk by all GPIOs on $V_{SS}$, plus the maximum Run consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 8*).

**Output voltage levels**

All GPIOs are CMOS and TTL compliant.

**Table 35. Output voltage characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Normal sourcing/sinking strength** | | | | | |
| $V_{OL}$ | Output low level voltage | CMOS port, $I_{IO}$ = 4 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-0.4 | - | |
| $V_{OL}$ | Output low level voltage | TTL port, $I_{IO}$ = 2 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 2.4 | - | |
| $V_{OL}$ | Output low level voltage | $I_{IO}$ = 9 mA | - | 1.3 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-1.3 | - | |
| $V_{OL}$ | Output low level voltage | $I_{IO}$ = 2 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.4 V ≤ $V_{DD}$ < 2.7 V | $V_{DD}$-0.4 | - | |
| **Large sourcing/sinking strength** | | | | | |
| $V_{OL}$ | Output low level voltage | CMOS port, $I_{IO}$ = 6 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-0.4 | - | |
| $V_{OL}$ | Output low level voltage | TTL port, $I_{IO}$ = 5 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 2.4 | - | |
| $V_{OL}$ | Output low level voltage | $I_{IO}$ = 18 mA | - | 1.3 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-1.3 | - | |
| $V_{OL}$ | Output low level voltage | $I_{IO}$ = 4 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.4 V ≤ $V_{DD}$ < 2.7 V | $V_{DD}$-0.4 | - | |
| **Maximum sourcing/sinking strength** | | | | | |
| $V_{OL}$ | Output low level voltage | CMOS port, $I_{IO}$ = 15 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-0.4 | - | |
| $V_{OL}$ | Output low level voltage | TTL port, $I_{IO}$ = 12 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 2.4 | - | |
| $V_{OL}$ | Output low level voltage | $I_{IO}$ = 12 mA | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | 2.4 V ≤ $V_{DD}$ < 2.7 V | $V_{DD}$-0.4 | - | |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Ultra high sinking strength** (2) | | | | | |
| $V_{OL}$ | Output low level voltage | $I_{IO}$ = 25 mA, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OL}$ | Output high level voltage | $I_{IO}$ = 18 mA, 2.4 V ≤ $V_{DD}$ < 2.7 V | | | |

(1) Obtained by characterization results, not tested in production.
(2) When GPIO ultra high sinking strength is enabled, its $V_{OH}$ is the same as that of maximum sourcing strength.

### Input AC characteristics

The definition and values of input AC characteristics are given as follows.

**Table 36. Input AC characteristics**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{EXINTpw}$(1) | Pulse width of external signals detected by EXINT controller | 10 | - | ns |

(1) Guaranteed by design, not tested in production.

## 4.3.12 NRST pin characteristics

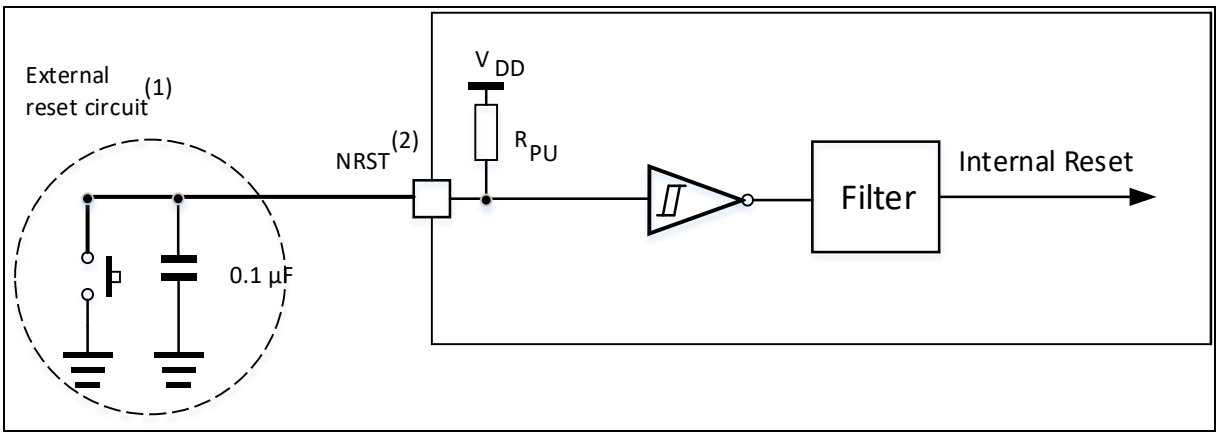
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see the table below).

**Table 37. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST input low level voltage | - | -0.3 | - | 0.8 | V |
| $V_{IH(NRST)}$(1) | NRST input high level voltage | - | 2 | - | $V_{DD}$ + 0.3 | |
| $V_{hys(NRST)}$(1) | NRST Schmitt trigger voltage hysteresis | - | - | 500 | - | mV |
| $R_{PU}$(2) | Weak pull-up equivalent resistor | $V_{IN}$ = $V_{SS}$ | 30 | 40 | 50 | kΩ |
| $t_{ILV(NRST)}$(1) | NRST input low level invalid time | - | - | - | 40 | μs |
| $t_{ILNV(NRST)}$(1) | NRST input low level valid time | - | 80 | - | - | μs |

(1) Guaranteed by design, not tested in production.
(2) Obtained by characterization results, not tested in production.

**Figure 17. Recommended NRST pin protection**




(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the $V_{IL\ (NRST)}$ max level specified in *Table 37*. Otherwise, the reset will not be performed by the device.

### 4.3.13 XMC characteristics

The parameters given in the table below are guaranteed by design and not tested in production.

**Asynchronous waveforms and timings of SRAM/PSRAM/NOR**

The results shown in these tables are obtained with the following XMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

**Table 38. Asynchronous multiplexed PSRAM/NOR read timings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | XMC_NE low time | $7t_{HCLK}$ - 2 | $7t_{HCLK}$ + 2 | ns |
| $t_{v(NOE\_NE)}$ | XMC_NE low to XMC_NOE low | $3t_{HCLK}$ - 0.5 | $3t_{HCLK}$ + 1.5 | ns |
| $t_{w(NOE)}$ | XMC_NOE low time | $4t_{HCLK}$ - 1 | $4t_{HCLK}$ + 2 | ns |
| $t_{h(NE\_NOE)}$ | XMC_NOE high to XMC_NE high hold time | -1 | - | ns |
| $t_{v(A\_NE)}$ | XMC_NE low to XMC_A valid | - | 0 | ns |
| $t_{v(NADV\_NE)}$ | XMC_NE low to XMC_NADV low | 3 | 5 | ns |
| $t_{w(NADV)}$ | XMC_NADV low time | $t_{HCLK}$ - 1.5 | $t_{HCLK}$ + 1.5 | ns |
| $t_{h(AD\_NADV)}$ | XMC_AD (address) valid hold time after XMC_NADV high | $t_{HCLK}$ + 3 | - | ns |
| $t_{h(A\_NOE)}$ | Address hold time after XMC_NOE high | $t_{HCLK}$ + 3 | - | ns |
| $t_{h(UBLB\_NOE)}$ | XMC_UB/LB hold time after XMC_NOE high | 0 | - | ns |
| $t_{v(UBLB\_NE)}$ | XMC_NE low to XMC_UB/LB valid | - | 0 | ns |
| $t_{su(Data\_NE)}$ | Data to XMC_NE high setup time | $2t_{HCLK}$ + 24 | - | ns |
| $t_{su(Data\_NOE)}$ | Data to XMC_NOE high setup time | $2t_{HCLK}$ + 25 | - | ns |
| $t_{h(Data\_NE)}$ | Data hold time after XMC_NE high | 0 | - | ns |
| $t_{h(Data\_NOE)}$ | Data hold time after XMC_NOE high | 0 | - | ns |

**Figure 18. Asynchronous multiplexed PSRAM/NOR read waveforms**

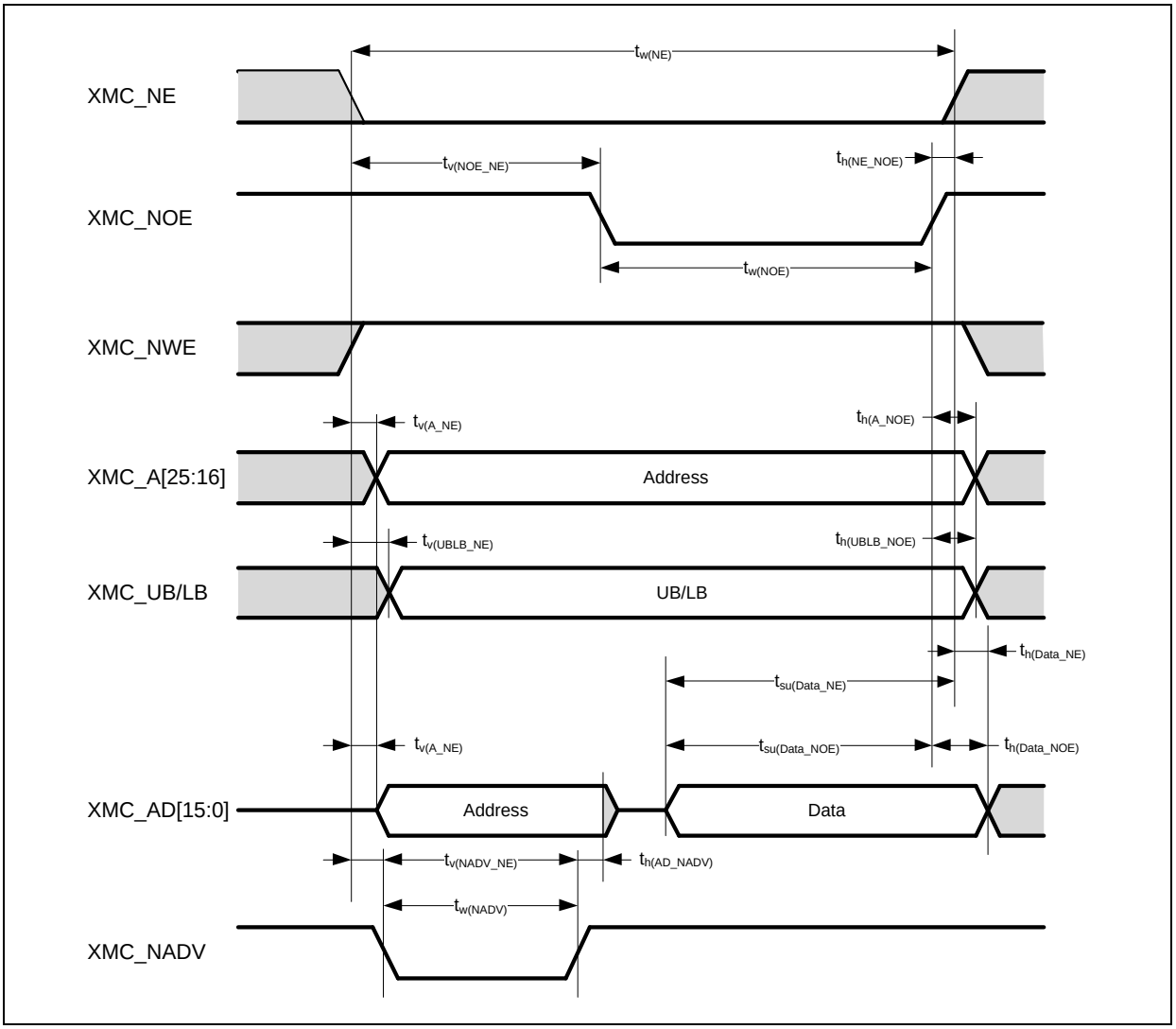
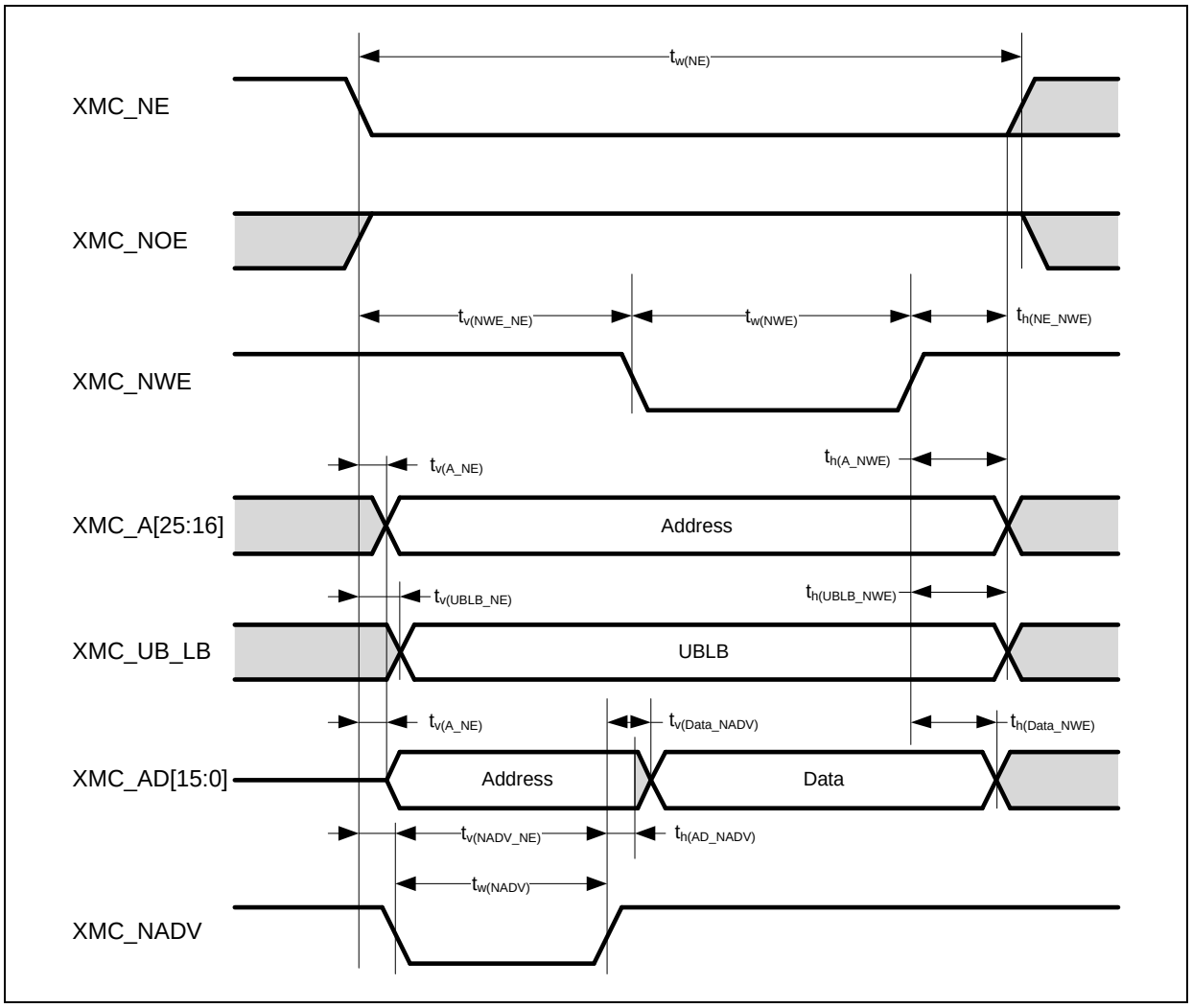



**Table 39. Asynchronous multiplexed PSRAM/NOR write timings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | XMC_NE low time | $5t_{HCLK}$ - 1 | $5t_{HCLK}$ + 2 | ns |
| $t_{v(NWE\_NE)}$ | XMC_NE low to XMC_NWE low | $2t_{HCLK}$ | $2t_{HCLK}$ + 1 | ns |
| $t_{w(NWE)}$ | XMC_NWE low time | $2t_{HCLK}$ - 1 | $2t_{HCLK}$ + 2 | ns |
| $t_{h(NE\_NWE)}$ | XMC_NWE high to XMC_NE high hold time | $t_{HCLK}$ - 1 | - | ns |
| $t_{v(A\_NE)}$ | XMC_NE low to XMC_A valid | - | 7 | ns |
| $t_{v(NADV\_NE)}$ | XMC_NE low to XMC_NADV low | 3 | 5 | ns |
| $t_{w(NADV)}$ | XMC_NADV low time | $t_{HCLK}$ - 1 | $t_{HCLK}$ + 1 | ns |
| $t_{h(AD\_NADV)}$ | XMC_AD (address) hold time after XMC_NADV high | $t_{HCLK}$ - 3 | - | ns |
| $t_{h(A\_NWE)}$ | Address hold time after XMC_NWE high | $4t_{HCLK}$ + 2.5 | - | ns |
| $t_{h(UBLB\_NWE)}$ | XMC_UB/LB hold time after XMC_NWE high | $t_{HCLK}$ - 1.5 | - | ns |
| $t_{v(UBLB\_NE)}$ | XMC_NE low to XMC_UB/LB valid | - | 1.6 | ns |
| $t_{v(Data\_NADV)}$ | XMC_NADV high to data valid | - | $t_{HCLK}$ + 1.5 | ns |
| $t_{h(Data\_NWE)}$ | Data hold time after XMC_NWE high | $t_{HCLK}$ - 5 | - | ns |

**Figure 19. Asynchronous multiplexed PSRAM/NOR write waveforms**



**Synchronous waveforms and timings of PSRAM/NOR**

The results given in these tables are obtained with the following XMC configuration:

- BurstAccessMode = XMC_BurstAccessMode_Enable; (Enable burst transfer mode)
- MemoryType = XMC_MemoryType_CRAM; (Memorty type is CRAM )
- WriteBurst = XMC_WriteBurst_Enable; (Enable write burst)
- CLKPrescale = 1 (1 memory cycle = 2 HCLK cycles) (Note: CLKPrescale is CLKPSC bit in XMC_BK1TMGx register. Refer to the AT32A423 reference manual.)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM (Note: DataLatency is DATLAT bit in XMC_BK1TMGx register. Refer to the AT32A423 reference manual.)

**Table 40. Synchronous multiplexed PSRAM/NOR read timings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | XMC_CLK period | 20 | - | ns |
| $t_{d(CLKL-NEL)}$ | XMC_CLK low to XMC_NE low | - | 1.5 | ns |
| $t_{d(CLKL-NEH)}$ | XMC_CLK low to XMC_NE high | 1 | - | ns |
| $t_{d(CLKL-NADVL)}$ | XMC_CLK low to XMC_NADV low | - | 4 | ns |
| $t_{d(CLKL-NADVH)}$ | XMC_CLK low to XMC_NADV high | 5 | - | ns |
| $t_{d(CLKL-AV)}$ | XMC_CLK low to XMC_A valid | - | 0 | ns |
| $t_{d(CLKL-AIV)}$ | XMC_CLK low to XMC_A invalid | 2 | - | ns |
| $t_{d(CLKH-NOEL)}$ | XMC_CLK high to XMC_NOE low | | 1 | ns |
| $t_{d(CLKL-NOEH)}$ | XMC_CLK low to XMC_NOE high | 0.5 | - | ns |
| $t_{d(CLKL-ADV)}$ | XMC_CLK low to XMC_AD valid | - | 12 | ns |
| $t_{d(CLKL-ADIV)}$ | XMC_CLK low to XMC_AD invalid | 0 | - | ns |
| $t_{su(ADV-CLKH)}$ | XMC_AD valid data setup time before XMC_CLK high | 6 | - | ns |
| $t_{h(CLKH-ADV)}$ | XMC_AD valid data hold time after XMC_CLK high | 6 | - | ns |
| $t_{su(NWAITV-CLKH)}$ | XMC_NWAIT valid setup time before XMC_CLK high | 8 | - | ns |
| $t_{h(CLKH-NWAITV)}$ | XMC_NWAIT valid hold time after XMC_CLK high | 6 | - | ns |

**Figure 20. Synchronous multiplexed PSRAM/NOR read waveforms**

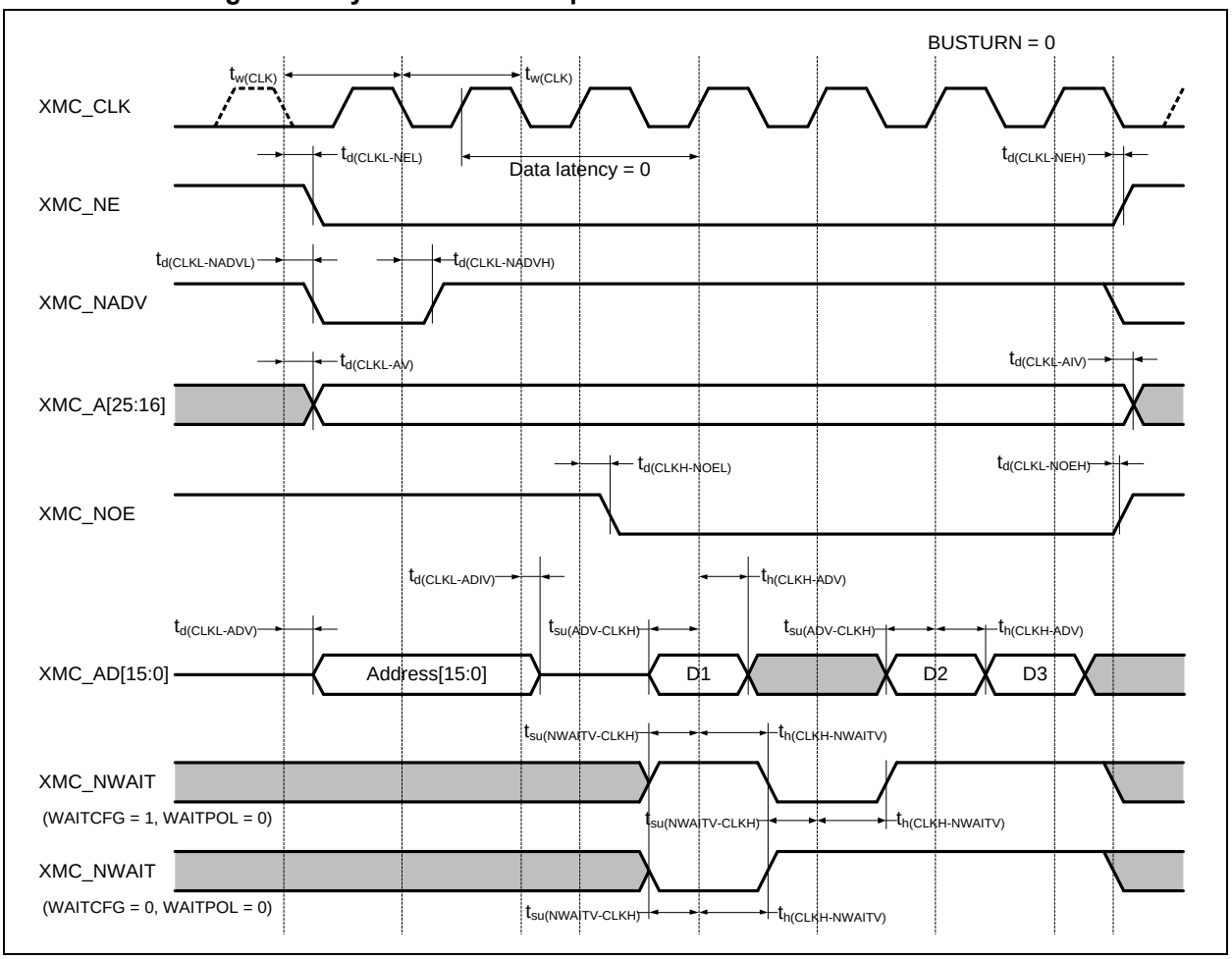
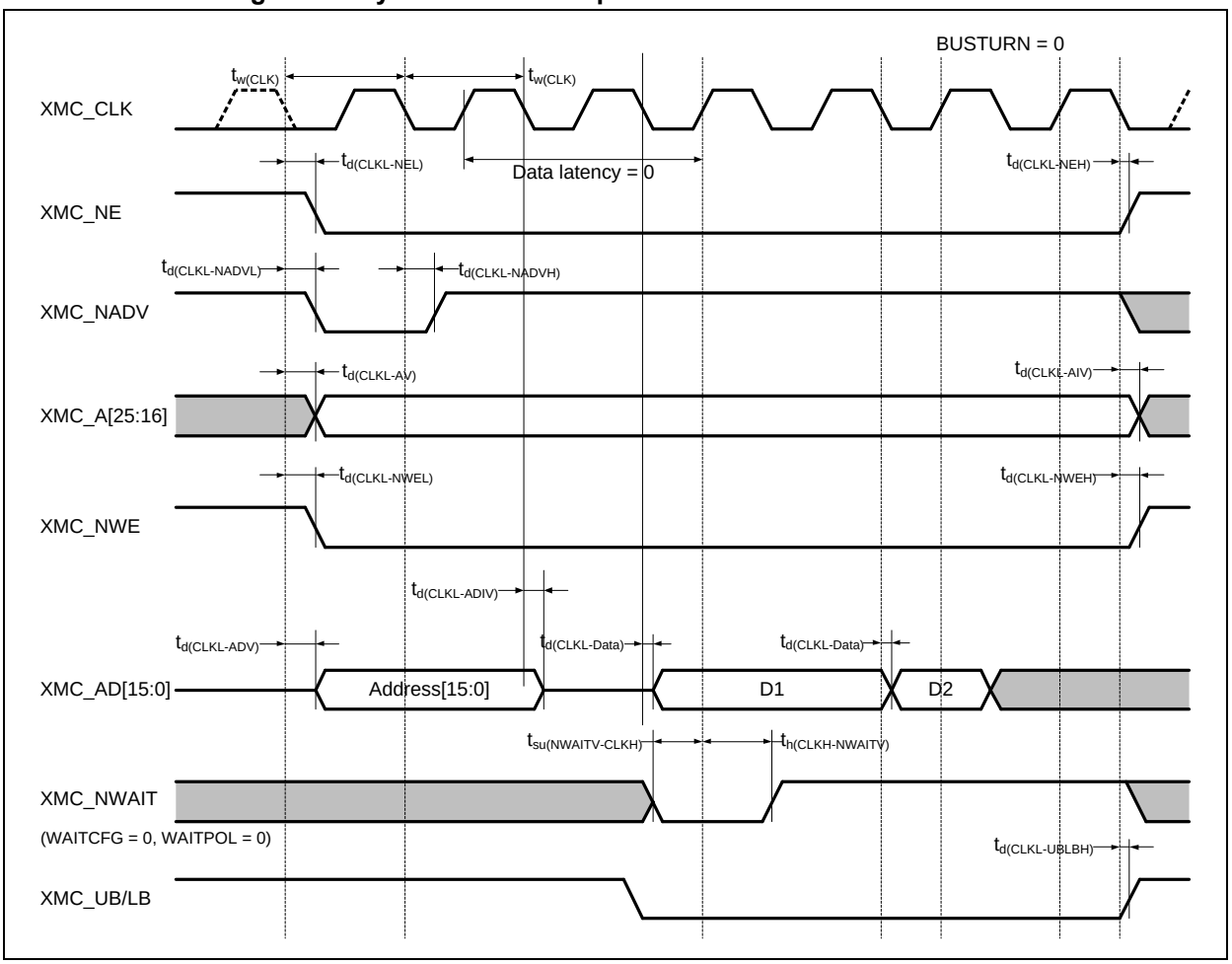


**Table 41. Synchronous multiplexed PSRAM write timings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | XMC_CLK period | 20 | - | ns |
| $t_{d(CLKL-NEL)}$ | XMC_CLK low to XMC_NE low | - | 2 | ns |
| $t_{d(CLKL-NEH)}$ | XMC_CLK low to XMC_NE high | 2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | XMC_CLK low to XMC_NADV low | - | 4 | ns |
| $t_{d(CLKL-NADVH)}$ | XMC_CLK low to XMC_NADV high | 5 | - | ns |
| $t_{d(CLKL-AV)}$ | XMC_CLK low to XMC_A valid | - | 0 | ns |
| $t_{d(CLKL-AIV)}$ | XMC_CLK low to XMC_A invalid | 2 | - | ns |
| $t_{d(CLKL-NWEL)}$ | XMC_CLK low to XMC_NWE low | - | 1 | ns |
| $t_{d(CLKL-NWEH)}$ | XMC_CLK low to XMC_NWE high | 0.5 | - | ns |
| $t_{d(CLKL-ADV)}$ | XMC_CLK low to XMC_AD valid | - | 12 | ns |
| $t_{d(CLKL-ADIV)}$ | XMC_CLK low to XMC_AD invalid | 3 | - | ns |
| $t_{d(CLKL-Data)}$ | XMC_AD after XMC_CLK low | - | 6 | ns |
| $t_{d(CLKL-UBLBH)}$ | XMC_CLK low to XMC_UB/LB high | 1 | - | ns |
| $t_{su(NWAITV-CLKH)}$ | XMC_NWAIT valid setup time before XMC_CLK high | 7 | - | ns |
| $t_{h(CLKH-NWAITV)}$ | XMC_NWAIT valid hold time after XMC_CLK high | 2 | - | ns |

**Figure 21. Synchronous multiplexed PSRAM write waveforms**



## 4.3.14 TMR timer characteristics

The parameters given in the table below are guaranteed by design and not tested in production.

**Table 42. TMR timer characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TMR)}$ | Timer resolution time | - | 1 | - | $t_{TMRxCLK}$ |
| | | $f_{TMRxCLK}$ = 150 MHz | 6.66 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | - | 0 | $f_{TMRxCLK}/2$ | MHz |

## 4.3.15 SPI characteristics

**Table 43. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $(1/t_{c(SCK)})^{(1)}$ | SPI clock frequency$^{(2)(3)}$ | Master mode | - | 32 | MHz |
| | | Slave receive mode | - | 32 | |
| | | Slave transmit mode | - | 25 | |
| $t_{su(CS)}^{(1)}$ | CS setup time | Slave mode | $4t_{PCLK}$ | - | ns |
| $t_{h(CS)}^{(1)}$ | CS hold time | Slave mode | $2t_{PCLK}$ | - | ns |
| $t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$ | SCK high and low time | Master mode Prescaler factor = 4 | $2t_{PCLK}$ - 3 | $2t_{PCLK}$ + 3 | ns |
| $t_{su(MI)}^{(1)}$ | Data input setup time | Master mode | 6 | - | ns |
| $t_{su(SI)}^{(1)}$ | | Slave mode | 5 | - | |
| $t_{h(MI)}^{(1)}$ | Data input hold time | Master mode | 4 | - | ns |
| $t_{h(SI)}^{(1)}$ | | Slave mode | 5 | - | |
| $t_{a(SO)}^{(1)(4)}$ | Data output access time | Slave mode | $t_{PCLK}$ - 2 | $2t_{PCLK}$ + 2 | ns |
| $t_{dis(SO)}^{(1)(5)}$ | Data output disable time | Slave mode | $t_{PCLK}$ - 2 | $2t_{PCLK}$ + 2 | ns |
| $t_{v(SO)}^{(1)}$ | Data output valid time | Slave mode (after enable edge) | - | 25 | ns |
| $t_{v(MO)}^{(1)}$ | Data output valid time | Master mode (after enable edge) | - | 10 | ns |
| $t_{h(SO)}^{(1)}$ | Data output hold time | Slave mode (after enable edge) | 9 | - | ns |
| $t_{h(MO)}^{(1)}$ | | Master mode (after enable edge) | 2 | - | |

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 22. SPI timing diagram – slave mode and CPHA = 0

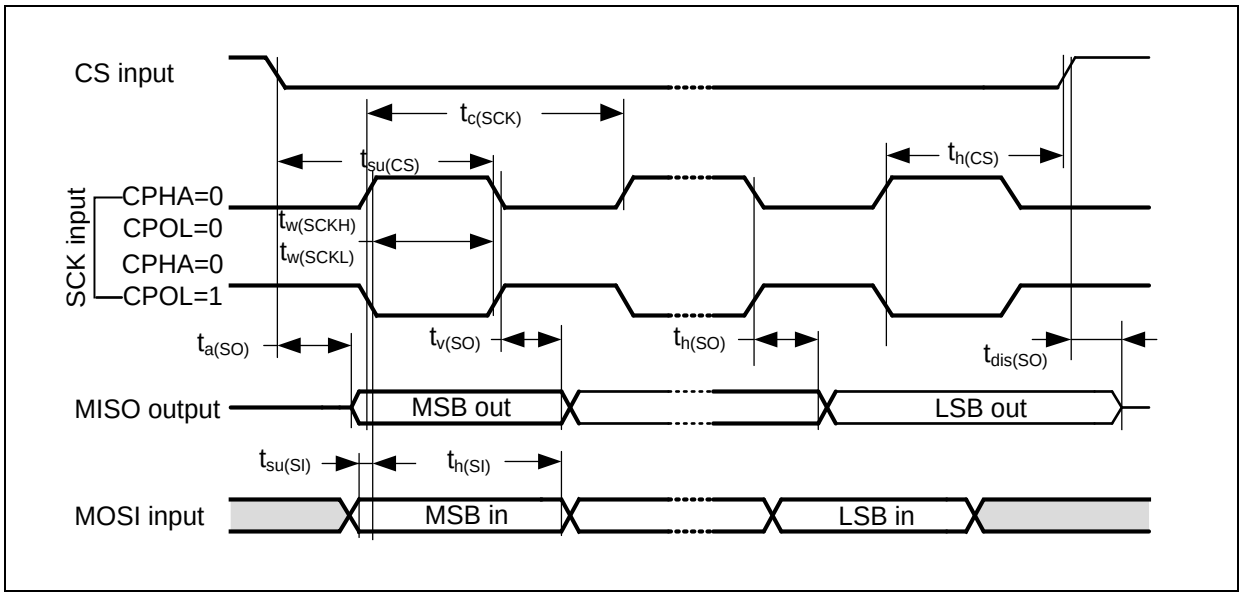



Figure 23. SPI timing diagram – slave mode and CPHA = 1

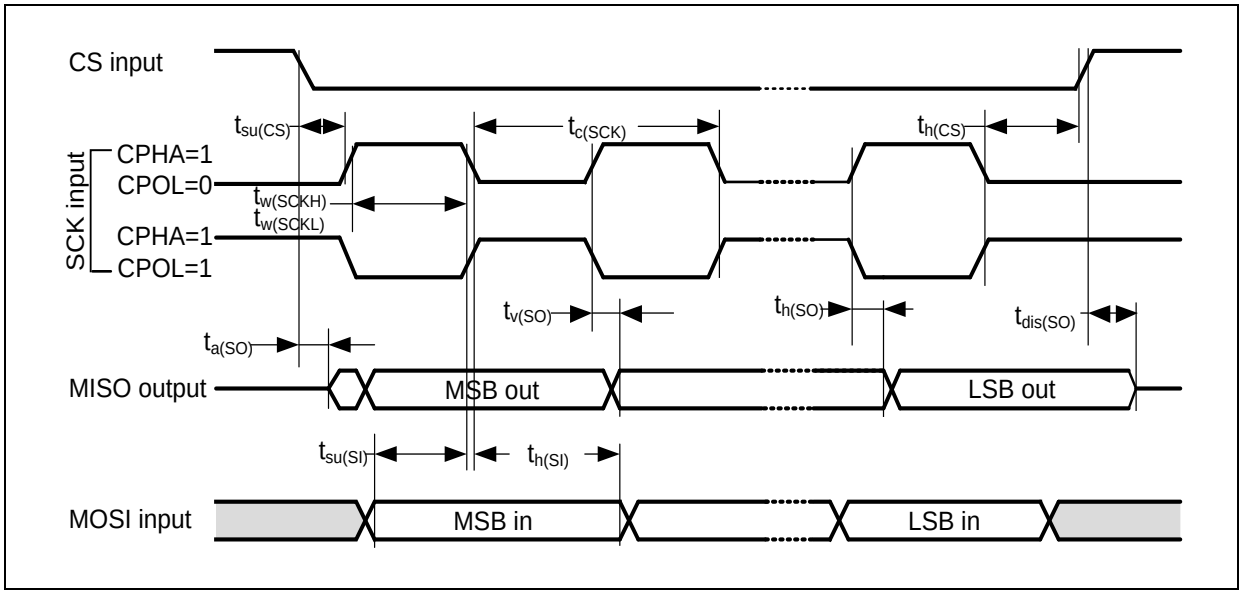
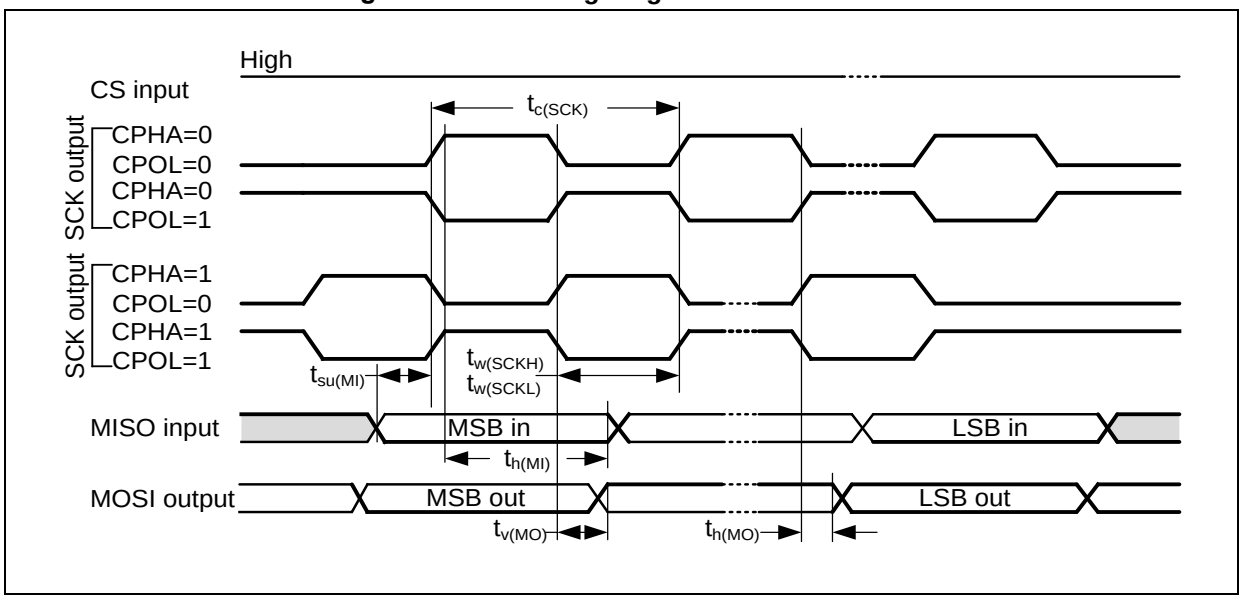



Figure 24. SPI timing diagram – master mode



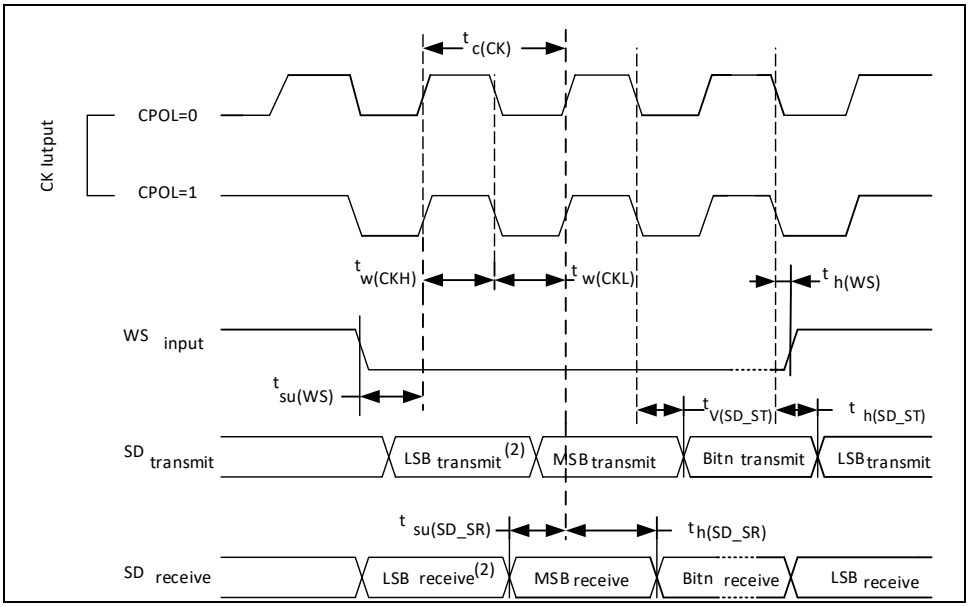
## 4.3.16 I²S characteristics

**Table 44. I²S characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{r(CK)}$<br>$t_{f(CK)}$ | I²S clock rise and fall time | Capacitive load: C = 15 pF | - | 12 | ns |
| $t_{v(WS)}$(1) | WS valid time | Master mode | 0 | 4 | |
| $t_{h(WS)}$(1) | WS hold time | Master mode | 0 | 4 | |
| $t_{su(WS)}$(1) | WS setup time | Slave mode | 9 | - | |
| $t_{h(WS)}$(1) | WS hold time | Slave mode | 0 | - | |
| $t_{su(SD\_MR)}$(1) | Data input setup time | Master receiver | 6 | - | |
| $t_{su(SD\_SR)}$(1) | | Slave receiver | 2 | - | |
| $t_{h(SD\_MR)}$(1)(2) | Data input hold time | Master receiver | 0.5 | - | |
| $t_{h(SD\_SR)}$(1)(2) | | Slave receiver | 0.5 | - | |
| $t_{v(SD\_ST)}$(1)(2) | Data output valid time | Slave transmitter (after enable edge) | - | 20 | |
| $t_{h(SD\_ST)}$(1) | Data output hold time | Slave transmitter (after enable edge) | 9 | - | |
| $t_{v(SD\_MT)}$(1)(2) | Data output valid time | Master transmitter (after enable edge) | - | 15 | |
| $t_{h(SD\_MT)}$(1) | Data output hold time | Master transmitter (after enable edge) | 0 | - | |

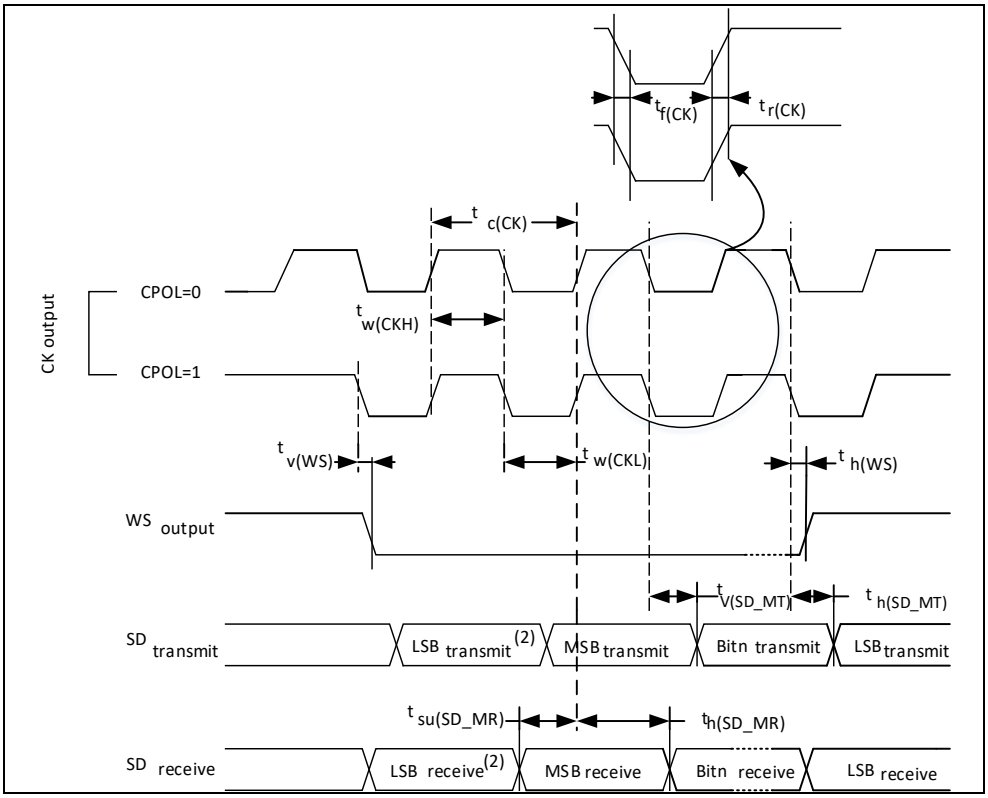
(1) Guaranteed by design, not tested in production.
(2) Depends on $f_{PCLK}$. For example, if $f_{PCLK}$=8 MHz, then $T_{PCLK}$ = 1/$f_{PCLK}$ =125 ns.

**Figure 25. I²S slave timing diagram (Philips protocol)**




(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 26. I²S master timing diagram (Philips protocol)**




(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

## 4.3.17 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and $V_{DD}$ is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz).

## 4.3.18 OTGFS characteristics

**Table 45. OTGFS startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | OTGFS transceiver startup time | 1 | µs |

(1) Guaranteed by design, not tested in production.

**Table 46. OTGFS DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| Input levels | $V_{DD}$ | OTGFS operating voltage | - | 3.0(2) | - | 3.6 | V |
| | $V_{DI}$(3) | Differential input sensitivity | I (OTGFS_D+/D-) | 0.2 | - | - | V |
| | $V_{CM}$(3) | Differential common mode range | Include $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{SE}$(3) | Single ended receiver threshold | - | 1.3 | - | 2.0 | |
| Output levels | $V_{OL}$ | Static output level low | 1.24 kΩ $R_L$ to 3.6 V(4) | - | - | 0.3 | V |
| | $V_{OH}$ | Static output level high | 15 kΩ $R_L$ to $V_{SS}$(4) | 2.8 | - | 3.6 | |
| $R_{PU}$ | | OTGFS_D+ internal pull-up value | $V_{IN}$ = $V_{SS}$ during idle | 0.97 | 1.24 | 1.58 | kΩ |
| | | | $V_{IN}$ = $V_{SS}$ during reception | 1.66 | 2.26 | 3.09 | |
| $R_{PD}$ | | OTGFS_D+/D- internal pull-down value | $V_{IN}$ = $V_{DD}$ | 15 | 19 | 25 | kΩ |

(1) All the voltages are measured from the local ground potential.
(2) The AT32A423 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics that are degraded in the 2.7 to 3.0 V $V_{DD}$ voltage range.
(3) Guaranteed by design, not tested in production.
(4) $R_L$ is the load connected to the USB drivers.

**Figure 27. OTGFS timings: definition of data signal rise and fall time**

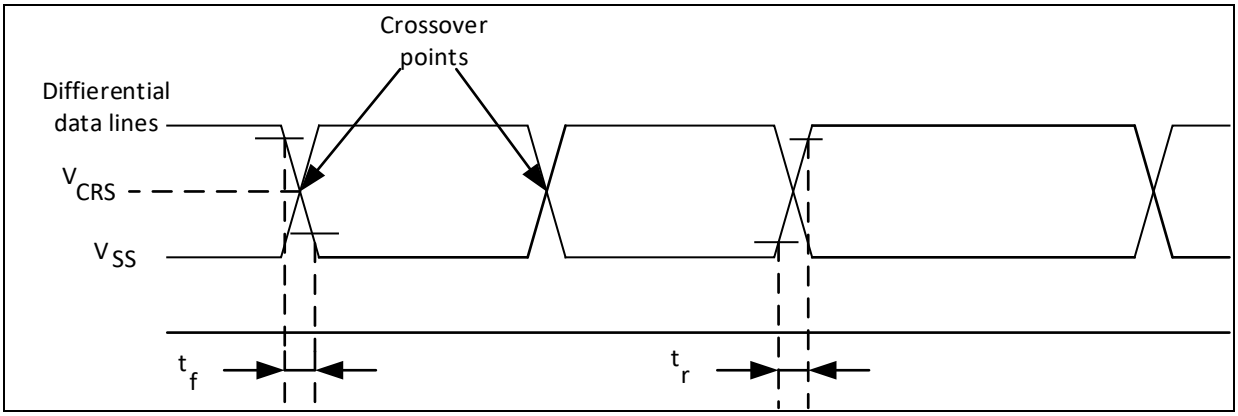



**Table 47. OTGFS electrical characteristics**

| Symbol | Parameter | Conditions | Min(1) | Max(1) | Unit |
|---|---|---|---|---|---|
| $t_r$ | Rise time (2) | $C_L$ ≤ 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time (2) | $C_L$ ≤ 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | 2.0 | V |

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

### 4.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 12*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 48. ADC characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | | 2.4 | - | 3.6 | V |
| $V_{REF+}$(1) | Positive reference voltage | - | | 2.0 | - | $V_{DDA}$ | V |
| $I_{DDA}$(2) | Current on the $V_{DDA}$ input pin | $f_{ADC}$ = 80 MHz | | - | 1000 | 1250 | μA |
| $I_{VREF+}$(1)(2) | Current on the $V_{REF+}$ input pin | $f_{ADC}$ = 80 MHz | | - | 470 | 510 | μA |
| $f_{ADC}$ | ADC clock frequency | $V_{REF+}$ ≥ 3.0 V | | 0.6 | - | 80 | MHz |
| | | $V_{REF+}$ < 3.0 V | | 0.6 | - | 30 | |
| $f_S$(3) | Sampling rate | 12-bit resolution | Fast channel | 0.04 | - | 5.33 | MSPS |
| | | | Slow channel | | | 4.21 | |
| | | 10-bit resolution | Fast channel | 0.047 | - | 6.15 | |
| | | | Slow channel | | | 4.71 | |
| | | 8-bit resolution | Fast channel | 0.055 | - | 7.27 | |
| | | | Slow channel | | | 5.33 | |
| | | 6-bit resolution | Fast channel | 0.067 | - | 8.88 | |
| | | | Slow channel | | | 6.15 | |
| $f_{TRIG}$(3) | External trigger frequency | $f_{ADC}$ = 80 MHz | | - | - | 4.44 | MHz |
| | | - | | - | - | 18 | $1/f_{ADC}$ |
| $V_{AIN}$(3) | Conversion voltage range (1) | - | | 0 ($V_{REF-}$ internally connected to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(3) | External input impedance | - | | See *Table 49* | | | Ω |
| $C_{ADC}$(3) | Internal sample and hold capacitor | - | | - | 10 | - | pF |
| $t_{CAL}$(3) | Calibration time | $f_{ADC}$ = 80 MHz | | 2.56 | | | μs |
| | | - | | 205 | | | $1/f_{ADC}$ |
| $t_{lat}$(3) | Preempted trigger conversion latency | $f_{ADC}$ = 80 MHz | | - | - | 37.5 | ns |
| | | - | | - | - | 3(4) | $1/f_{ADC}$ |
| $t_{latr}$(3) | Regular trigger conversion latency | $f_{ADC}$ = 80 MHz | | - | - | 25 | ns |
| | | - | | - | - | 2(4) | $1/f_{ADC}$ |
| $t_S$(3) | Sampling time | $f_{ADC}$ = 80 MHz | | 0.031 | - | 8.006 | μs |
| | | - | | 2.5 | - | 640.5 | $1/f_{ADC}$ |
| $t_{STAB}$(3) | Power-up time | - | | 45 | | | $1/f_{ADC}$ |
| $t_{CONV}$(3) | Total conversion time (including sampling time) | $f_{ADC}$ = 80 MHz in 12-bit resolution | | 0.188 | - | 8.163 | μs |
| | | 12-bit resolution | | 15 ~ 653 ($t_S$ for sampling + 12.5 for successive approximation) | | | $1/f_{ADC}$ |

(1) $V_{REF+}$ may be connected to $V_{DDA}$ internally, depending on packages.
(2) Obtained by characterization results, not tested in production.
(3) Guaranteed by design, not tested in production.
(4) For external triggers, a delay of 1/$f_{PCLK2}$ must be added to the latency specified in *Table 48*.

*Table 49* defines the maximum external impedance allowed for an error below 1 of LSB in 12-bit resolution.

**Table 49. $R_{AIN}$ max when $f_{ADC}$ = 80 MHz**

| $T_S$ (cycle) | $t_S$ (µs) | $R_{AIN}$ max (Ω)(1) | |
|---|---|---|---|
| | | Fast channel | Slow channel |
| 2.5 | 0.031 | 30 | Not support |
| 6.5 | 0.081 | 200 | 50 |
| 12.5 | 0.156 | 400 | 350 |
| 24.5 | 0.306 | 800 | 700 |
| 47.5 | 0.594 | 1700 | 1500 |
| 92.5 | 1.156 | 3000 | 2600 |
| 247.5 | 3.094 | 9000 | 8500 |
| 640.5 | 8.006 | 20000 | 19000 |

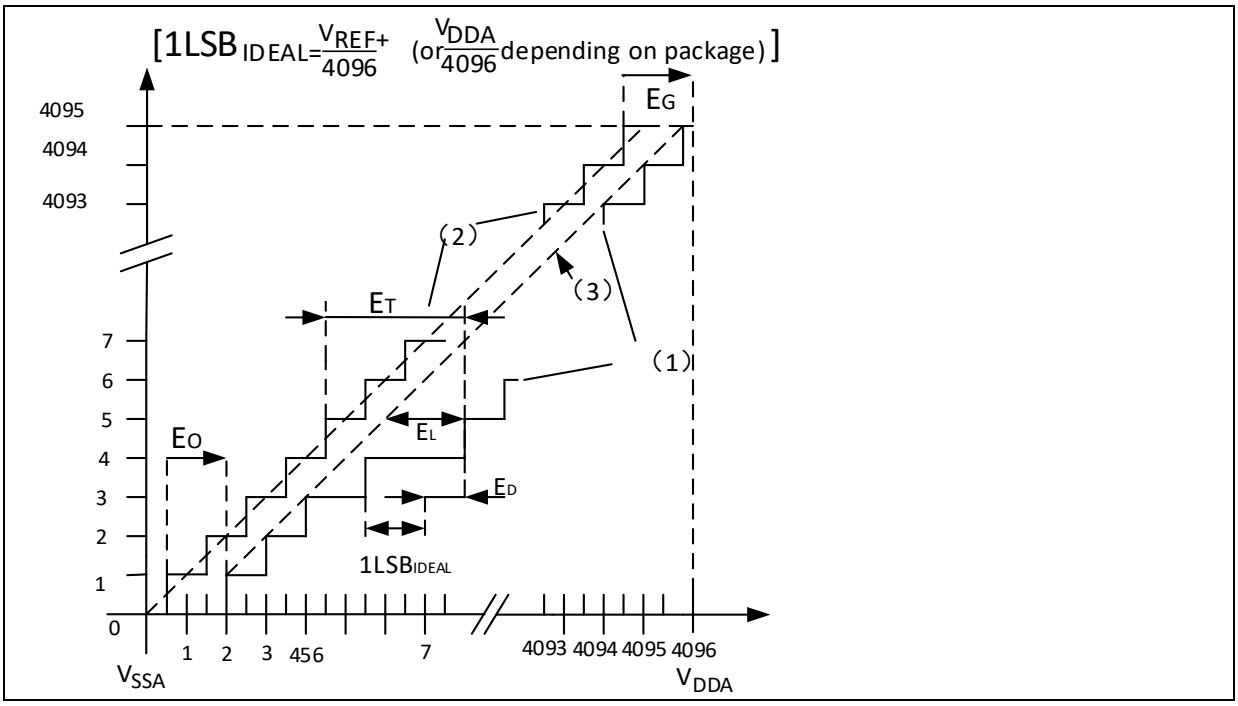
(1) Guaranteed by design.

**Table 50. ADC accuracy (1)(2)**

| Symbol | Parameter | Test Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ = 80 MHz, $R_{AIN}$ < 20 kΩ, $V_{DDA}$ = 3.0 ~ 3.6 V, $T_A$ =-40 ~ 105 °C, $V_{REF+}$ = $V_{DDA}$ | ±3 | ±5 | LSB |
| EO | Offset error | | -1 | +1/-2 | |
| EG | Gain error | | +2 | +3.5 | |
| ED | Differential linearity error | | +2.5 | +4/-1 | |
| EL | Integral linearity error | | +3 | ±4.5 | |
| ET | Total unadjusted error | $f_{ADC}$ = 30 MHz, $R_{AIN}$ < 20 kΩ, $V_{DDA}$ = 2.4 ~ 3.6 V, $T_A$ = -40 ~ 105 °C, $V_{REF+}$ = $V_{DDA}$ | ±2 | ±3.5 | LSB |
| EO | Offset error | | -0.5 | +1/-2 | |
| EG | Gain error | | +2 | +3 | |
| ED | Differential linearity error | | ±0.75 | ±1 | |
| EL | Integral linearity error | | ±1.5 | ±2 | |
| ET | Total unadjusted error | $f_{ADC}$ = 30 MHz, $R_{AIN}$ < 20 kΩ, $V_{DDA}$ = 2.4 ~ 3.6 V, $T_A$ = -40 ~ 105 °C $V_{REF+}$ = 2.0 ~ 2.4 V | ±2.5 | ±4 | LSB |
| EO | Offset error | | -1.5 | +1/-3.5 | |
| EG | Gain error | | +2 | +3.5 | |
| ED | Differential linearity error | | ±0.7 | +1.2/-1 | |
| EL | Integral linearity error | | ±1.2 | ±2 | |

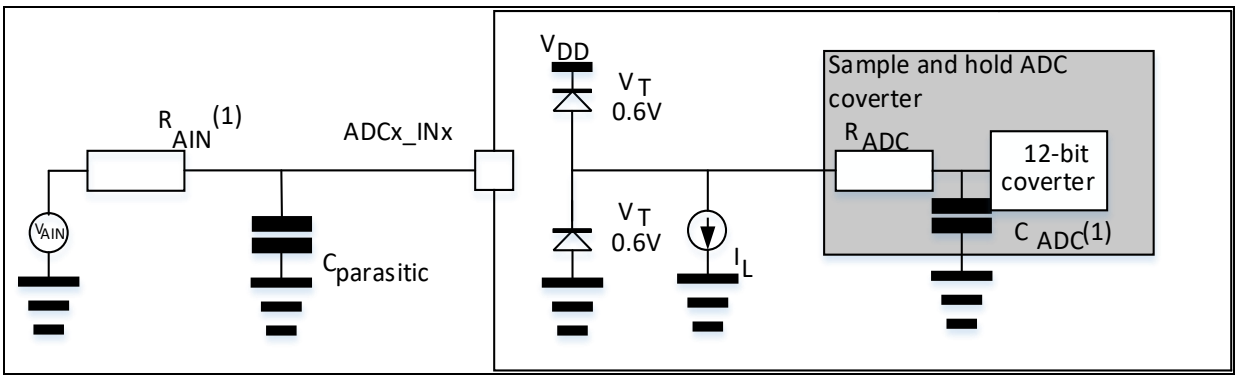
(1) ADC DC accuracy values are measured after internal calibration.
(2) Obtained by characterization results, not tested in production.

**Figure 28. ADC accuracy characteristics**




(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
$E_T$ = Maximum deviation between the actual and the ideal transfer curves.
$E_O$ = Deviation between the first actual transition and the first ideal one.
$E_G$ = Deviation between the last ideal transition and the last actual one.
$E_D$ = Maximum deviation between actual steps and the ideal one.
$E_L$ = Maximum deviation between any actual transition and the end point correlation line.

**Figure 29. Typical connection diagram using the ADC**

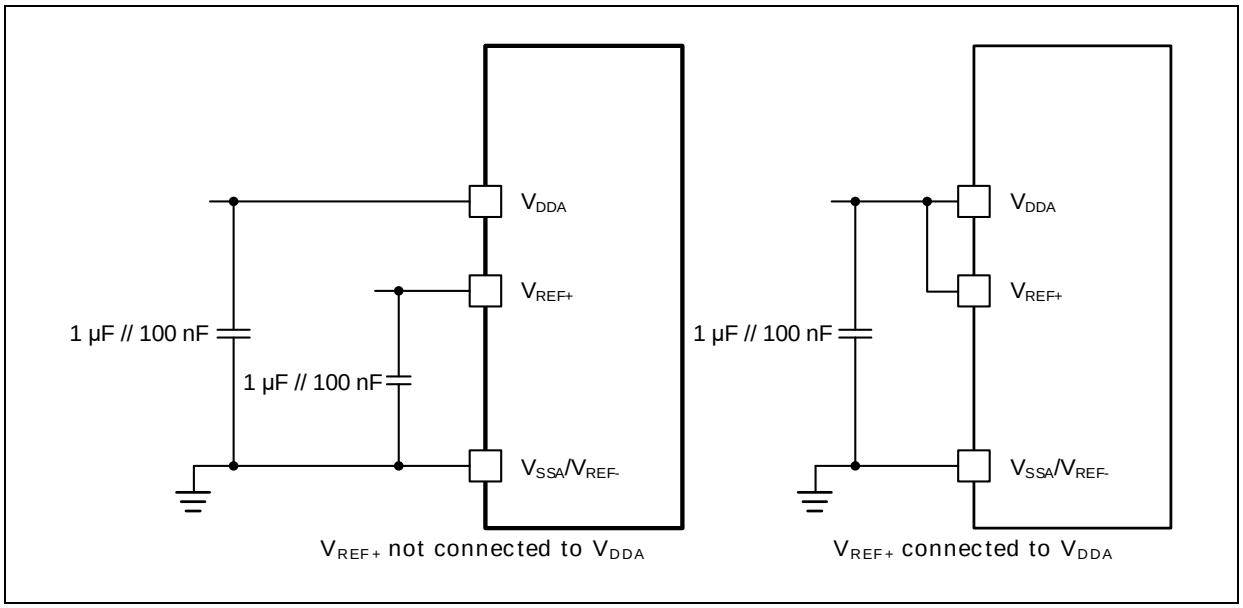



(1) Refer to *Table 48* for the values of $R_{AIN}$ and $C_{ADC}$.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

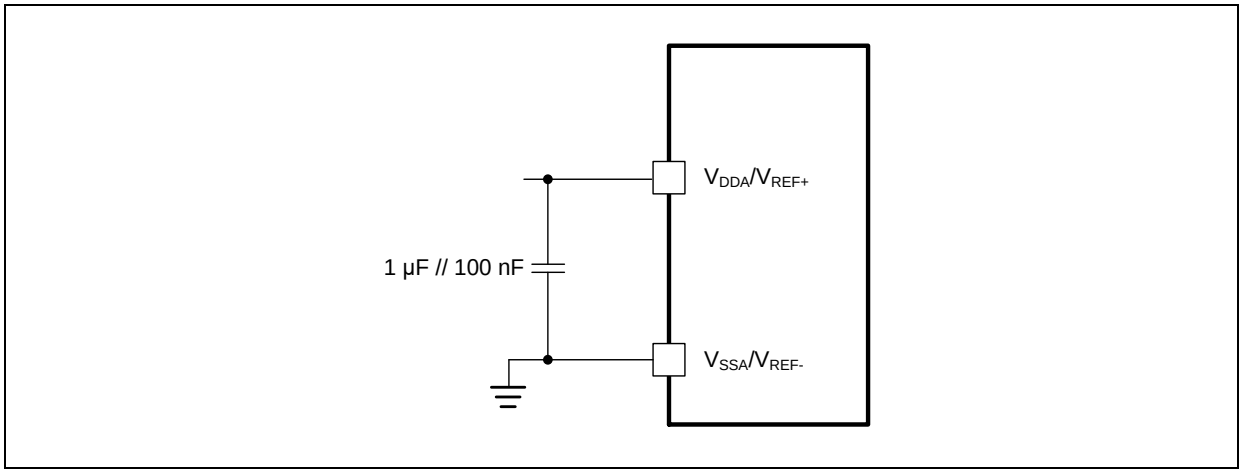
Power supply decoupling should be performed as shown in *Figure 30* or *Figure 31,* depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Figure 30. Power supply and reference decoupling (for packages with external $V_{REF+}$ pin)**




(1) $V_{REF+}$ input is available only on 100-pin package.

**Figure 31. Power supply and reference decoupling (for packages without $V_{REF+}$ pin)**




(1) $V_{REF+}$ input is available only on 100-pin package.

## 4.3.20 Internal reference voltage ($V_{INTRV}$) characteristics

**Table 51. Internal reference voltage characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INTRV}$(1) | Internal reference voltage | - | 1.16 | 1.20 | 1.24 | V |
| $T_{Coeff}$(1) | Temperature coefficient | - | - | 50 | 100 | ppm/°C |
| $T_{S\_VINTRV}$(2) | ADC sampling time when reading the internal reference voltage | - | 5 | - | - | µs |

(1) Obtained by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

### 4.3.21 Temperature sensor ($V_{TS}$) characteristics

**Table 52. Temperature sensor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_L$[1] | $V_{TS}$ linearity with temperature | $T_A$ = -20 ~ +85 °C | - | ±1 | ±2 | ºC |
| | | $T_A$ = -40 ~ +105 °C | - | - | ±3 | |
| Avg_Slope[1(2)] | Average slope | - | -4.06 | -4.26 | -4.47 | mV/ºC |
| $V_{25}$[1][2] | Voltage at 25 ºC | - | 1.20 | 1.29 | 1.38 | V |
| $t_{START}$[3] | Startup time | - | - | - | 100 | µs |
| $T_{S\_temp}$[3] | ADC sampling time when reading the temperature | - | 5 | - | - | µs |

(1) Obtained by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

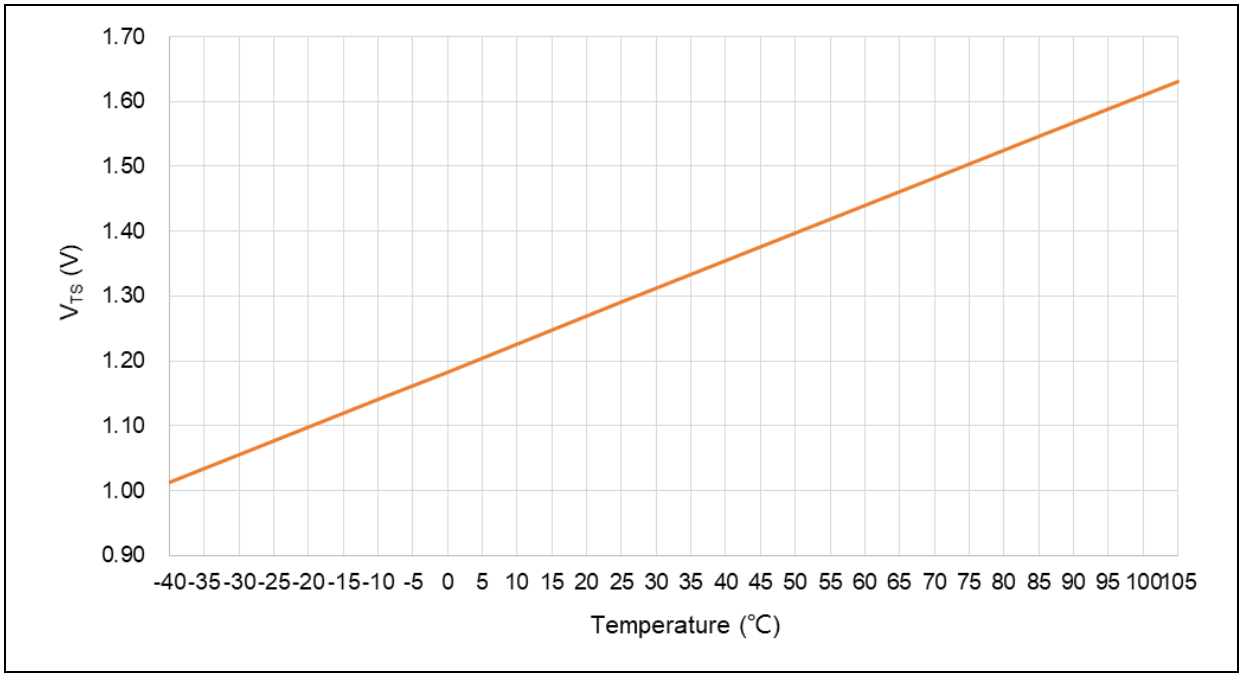
Temperature (in °C) = {($V_{25}$ - $V_{TS}$) / Avg_Slope} + 25.

Where,

$V_{25}$ = $V_{TS}$ value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. $V_{TS}$ (given in mV/° C).

**Figure 32. $V_{TS}$ vs. temperature**



## 4.3.22 12-bit DAC specifications

**Table 53. DAC characteristics**

| Symbol | Parameter | Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 2.4 | - | 3.6 | V |
| $V_{REF+}$(1) | Reference supply voltage | - | 2.0 | - | 3.6 | V |
| $V_{SSA}$ | Ground | - | 0 | - | 0 | V |
| $R_{LOAD}$(2) | Load resistance with buffer ON | - | 5 | - | - | kΩ |
| $R_O$(2) | Impedance output with buffer OFF | - | - | 13.2 | 16 | kΩ |
| $C_{LOAD}$(2) | Capacitive load (with buffer ON) | - | - | - | 50 | pF |
| DAC_OUT(2) | Lower DAC_OUT voltage with buffer ON | - | 0.2 | - | - | V |
| | Higher DAC_OUT voltage with buffer ON | - | - | - | $V_{REF+}$ - 0.2 | V |
| | Lower DAC_OUT voltage with buffer OFF | - | - | 0.5 | 5 | mV |
| | Higher DAC_OUT voltage with buffer OFF | - | - | - | $V_{REF+}$ - 5 mV | V |
| $I_{DDA}$(3) | DAC DC current consumption in quiescent mode | With no load, at $V_{REF+}$ = 3.6 V | - | 450 | 515 | μA |
| $I_{VREF+}$(1)(3) | DAC DC current consumption in quiescent mode | With no load, at $V_{REF+}$ = 3.6 V | - | 380 | 390 | μA |
| DNL(3) | Differential non linearity | - | - | ±0.5 | ±1 | LSB |
| INL(3) | Integral non linearity (difference between measured value at Code I and a line drawn between DAC_OUT min and DAC_OUT max) | - | - | ±1 | ±2 | LSB |
| Offset(3) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}$/2) | - | - | 10 | 15 | mV |
| | | | - | 10 | 20 | LSB |
| Gain(3) | Gain error | - | - | 0.2 | 0.4 | % |
| $t_{SETTLING}$(2) | Settling time | $R_{LOAD}$ ≥ 5 kΩ<br>$C_{LOAD}$ ≤ 50 pF | - | 1 | 4 | μs |
| Update rate(2) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1 LSB) | $R_{LOAD}$ ≥ 5 kΩ<br>$C_{LOAD}$ ≤ 50 pF | - | - | 1 | MSPS |
| $t_{WAKEUP}$(2) | Wakeup time from off state (setting the EN bit in the DAC Control register) | $R_{LOAD}$ ≥ 5 kΩ<br>$C_{LOAD}$ ≤ 50 pF | - | 1.2 | 4 | μs |

(1) $V_{REF+}$ can be internally connected to $V_{DDA}$ depending on the packages.
(2) Guaranteed by design, not tested in production.
(3) Obtained by characterization results, not tested in production.

# 5 Package information

## 5.1 LQFP100 – 14 x 14 mm

**Figure 33. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline**

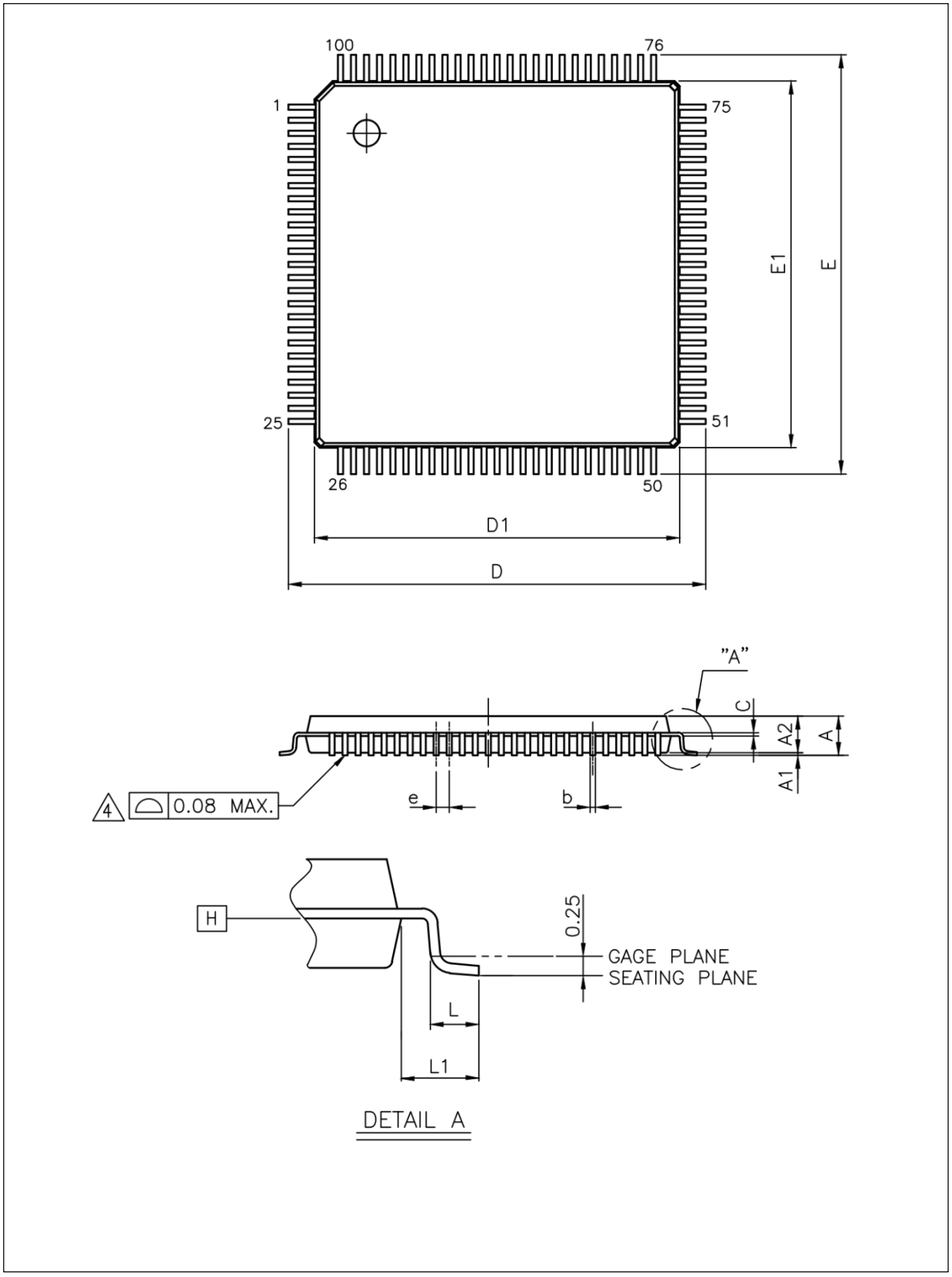


**Table 54. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.20 | 0.26 |
| c | 0.10 | 0.127 | 0.20 |
| D | 15.75 | 16.00 | 16.25 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.75 | 16.00 | 16.25 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | 0.50 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF. | | |

## 5.2 LQFP64 – 10 x 10 mm

**Figure 34. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline**

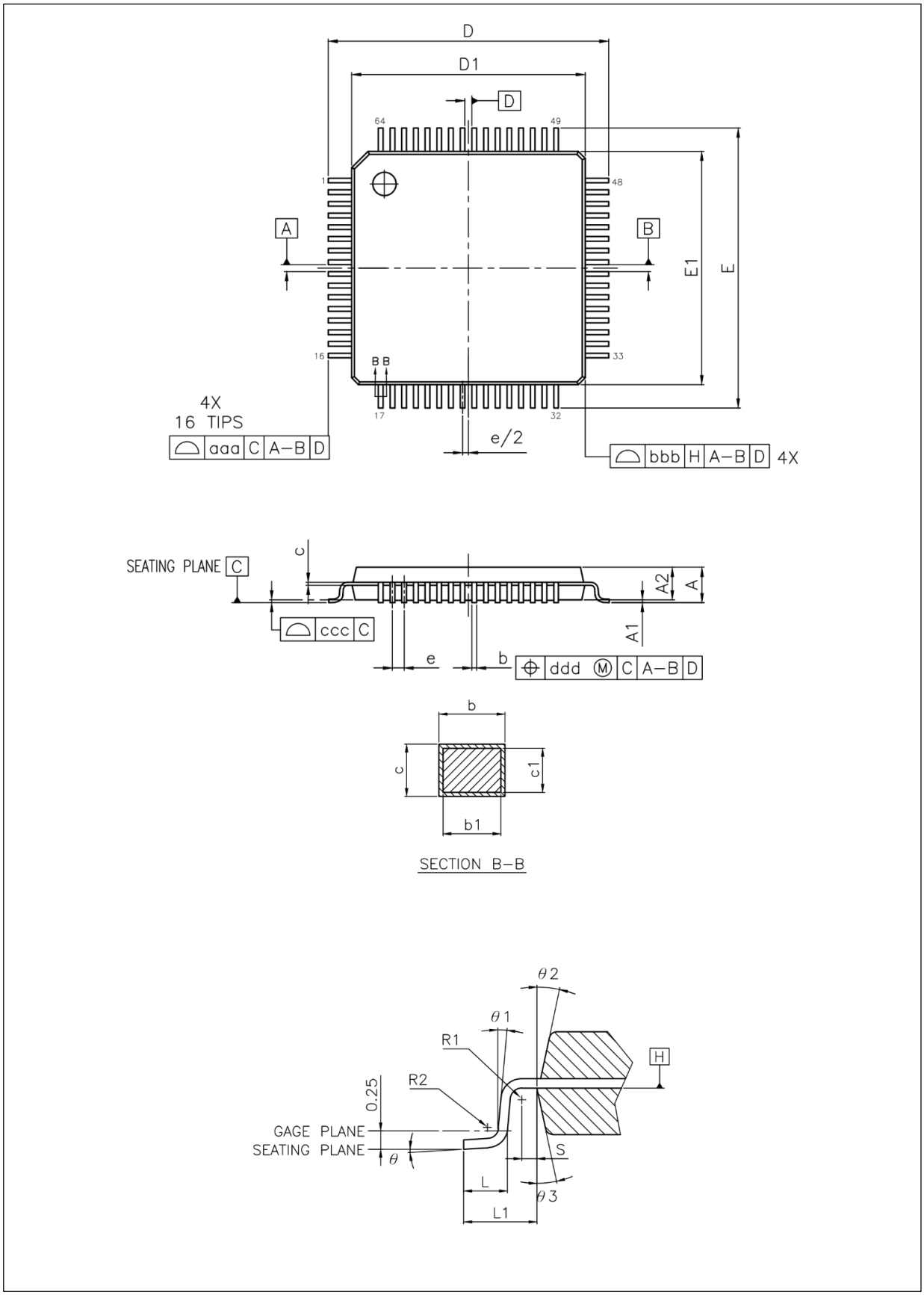


**Table 55. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.20 | 0.27 |
| c | 0.09 | - | 0.20 |
| D | 11.75 | 12.00 | 12.25 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.75 | 12.00 | 12.25 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | 0.50 BSC. | | |
| Θ | 3.5° REF. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF. | | |
| ccc | 0.08 | | |

## 5.3 LQFP64 – 7 x 7 mm

**Figure 35. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package outline**

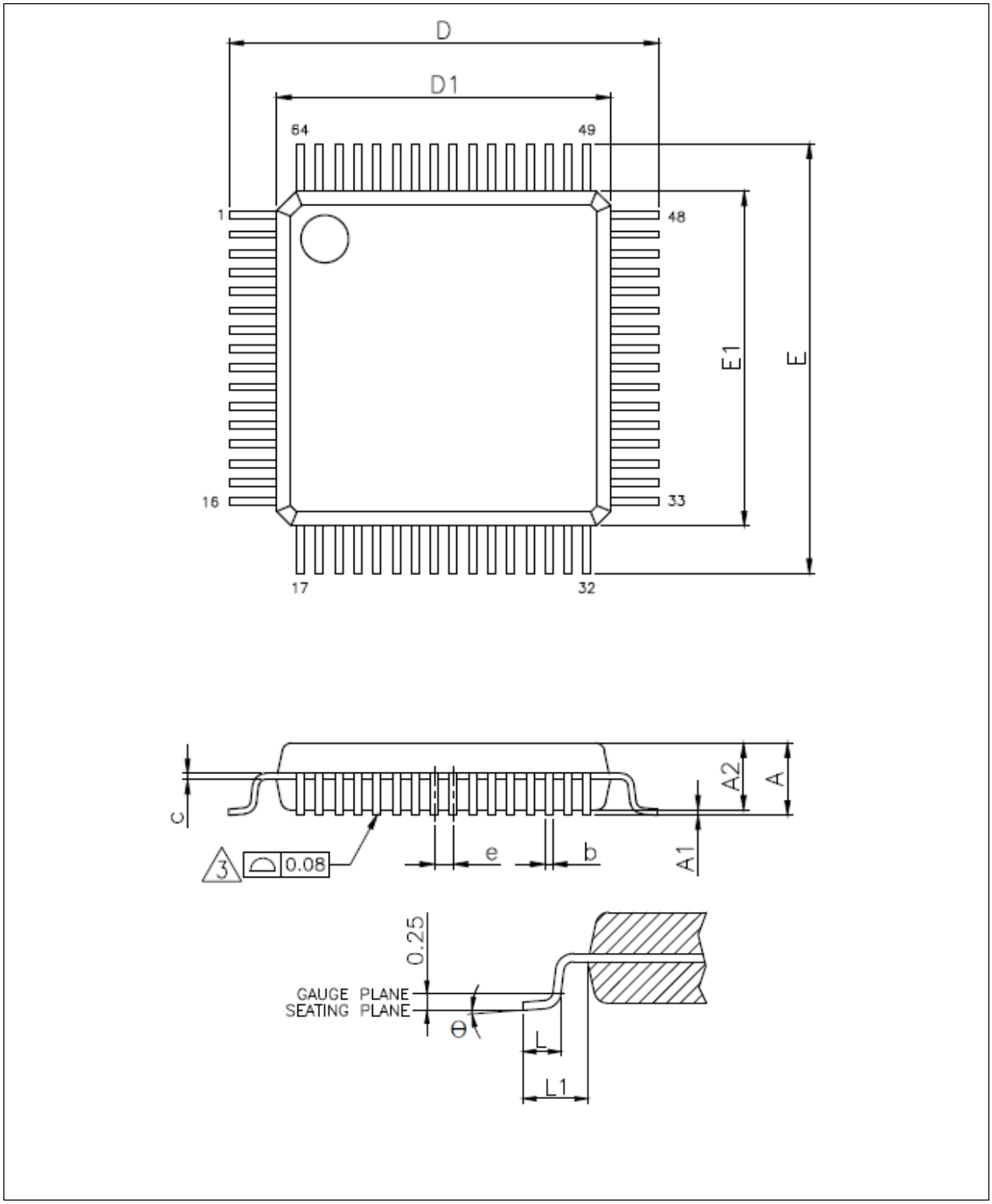


**Table 56. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.13 | 0.18 | 0.23 |
| c | 0.09 | - | 0.20 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | 0.40 BSC. | | |
| Θ | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF. | | |

## 5.4 LQFP48 – 7 x 7 mm

**Figure 36. LQFP48 – 7 x 7 mm 64 pin low-profile quad flat package outline**

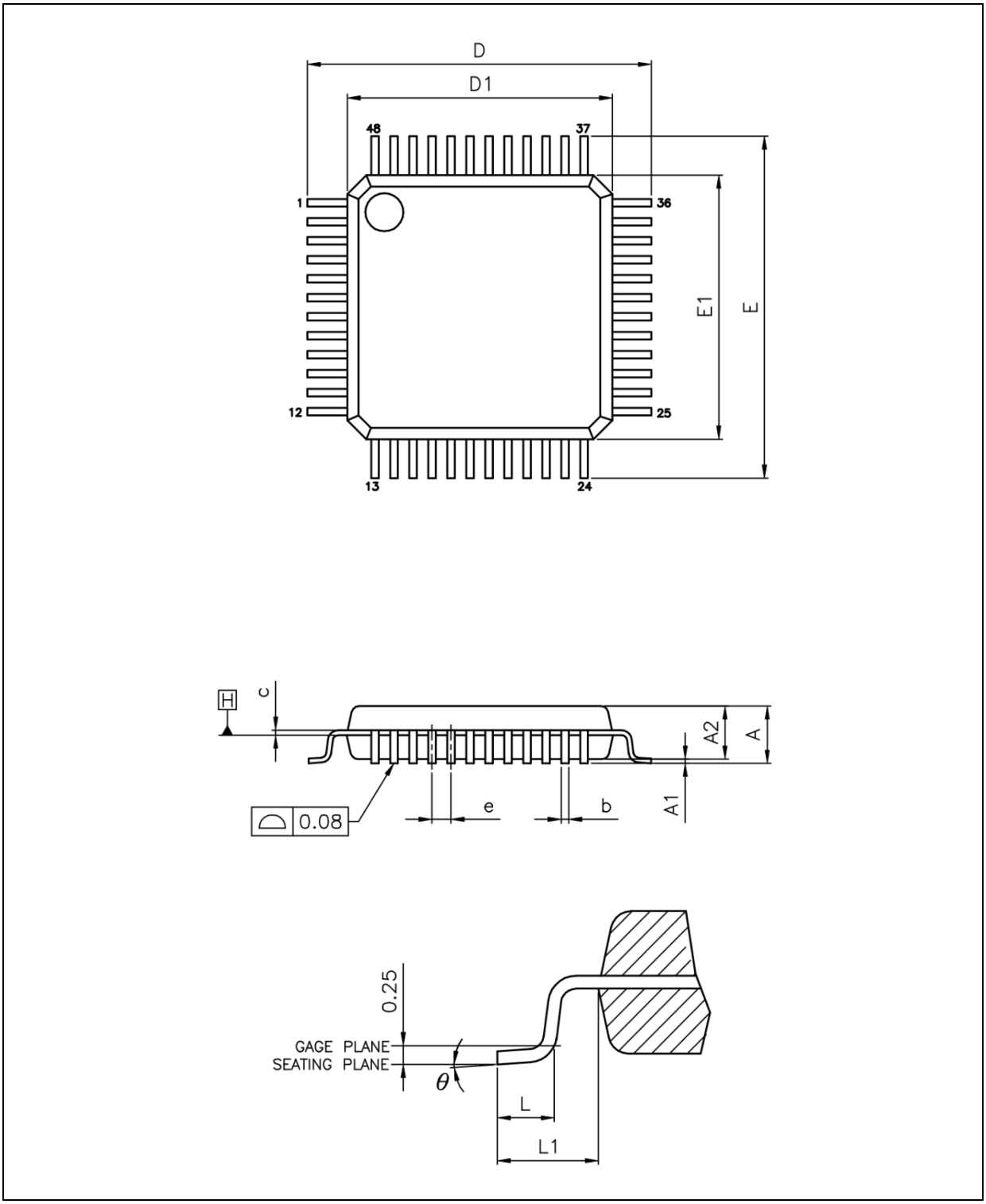


**Table 57. LQFP48– 7 x 7 mm 48 pin low-profile quad flat package outline**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | - | 0.20 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | 0.50 BSC. | | |
| Θ | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF. | | |

## 5.5 QFN48 – 6 x 6 mm

Figure 37. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline

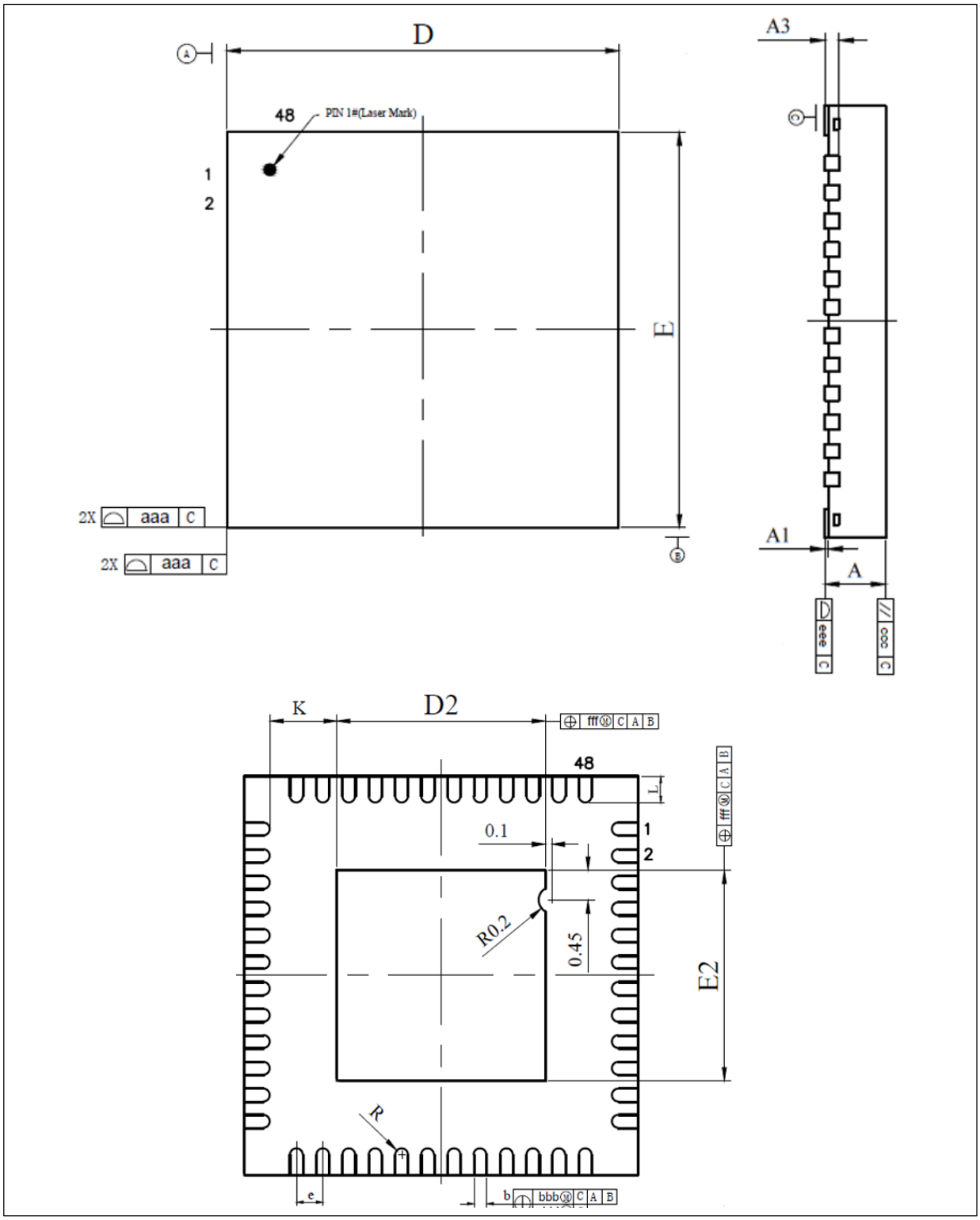


Table 58. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF. | |
| b | 0.15 | 0.20 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 3.07 | 3.17 | 3.27 |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 3.07 | 3.17 | 3.27 |
| e | | 0.40 BSC. | |
| K | 0.20 | - | - |
| L | 0.35 | 0.40 | 0.45 |

## 5.6 QFN36 – 6 x 6 mm

**Figure 38. QFN36 – 6 x 6 mm 36 pin quad flat no-leads package outline**

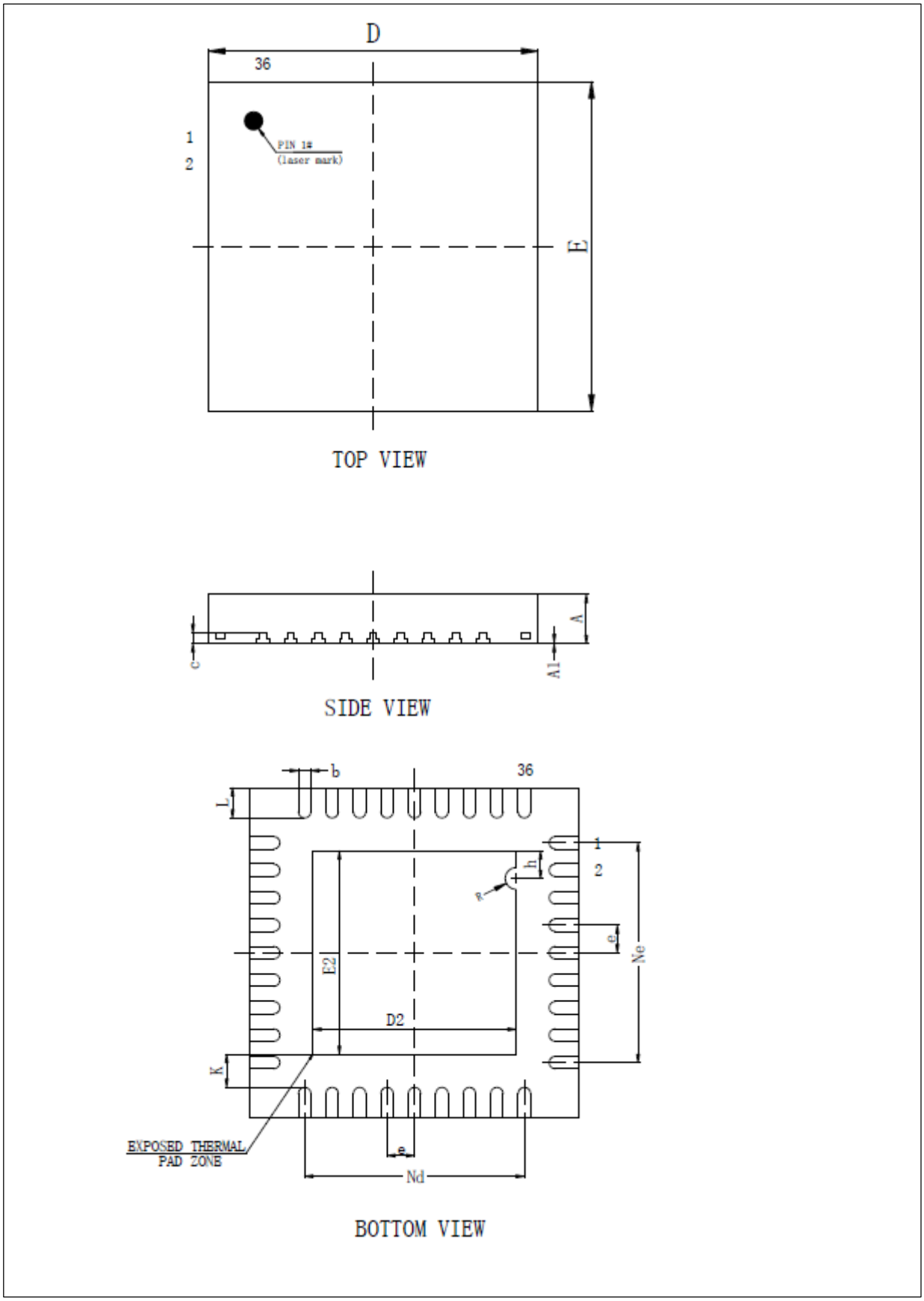


Table 59. QFN36 – 6 x 6 mm 36 pin quad flat no-leads package mechanical data

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.85 | 0.90 | 0.95 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.23 | 0.28 |
| c | 0.203 REF. | | |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 3.60 | 3.70 | 3.80 |
| Nd | 4.00 BSC. | | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 3.60 | 3.70 | 3.80 |
| Ne | 4.00 BSC. | | |
| e | 0.50 BSC. | | |
| L | 0.50 | 0.55 | 0.60 |
| K | 0.60 REF. | | |

## 5.7 QFN32 – 4 x 4 mm

Figure 39. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline

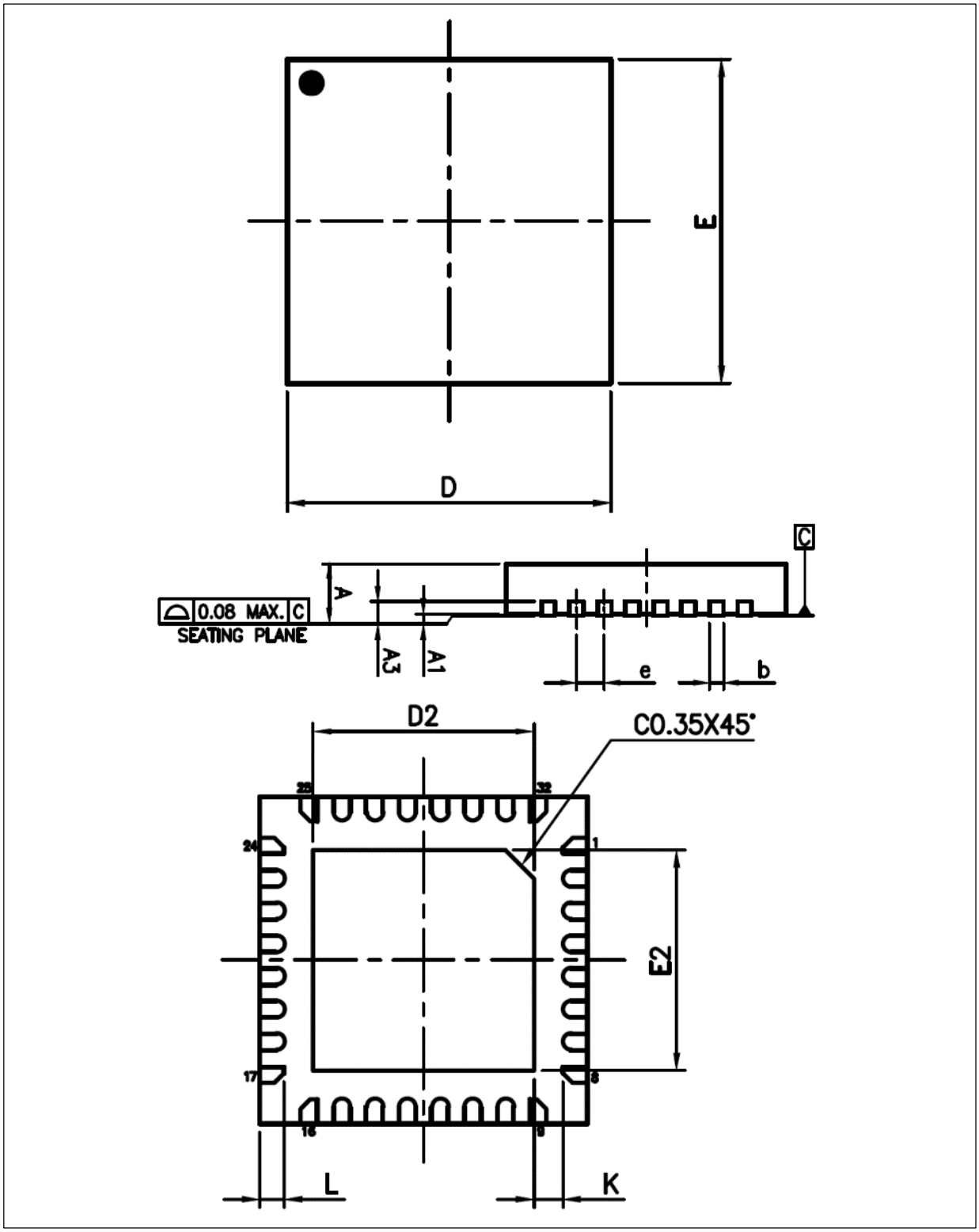


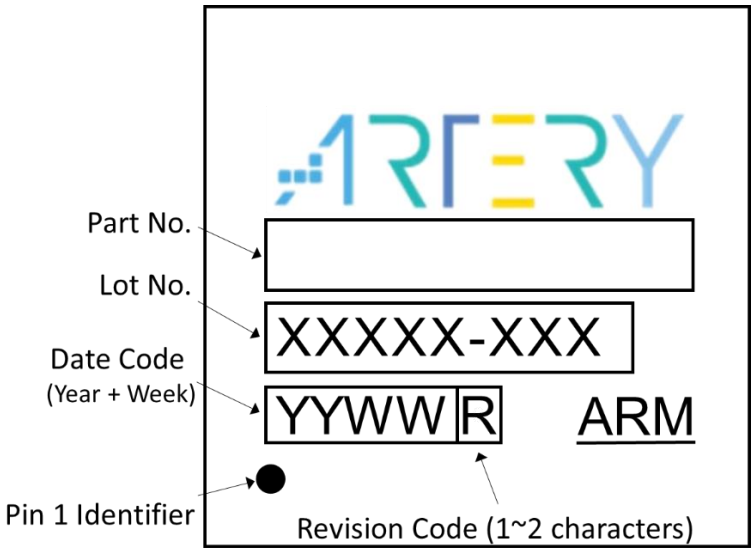
Table 60. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.65 | 2.70 | 2.75 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.65 | 2.70 | 2.75 |
| e | 0.40 BSC. | | |
| K | 0.20 | - | - |
| L | 0.25 | 0.30 | 0.35 |

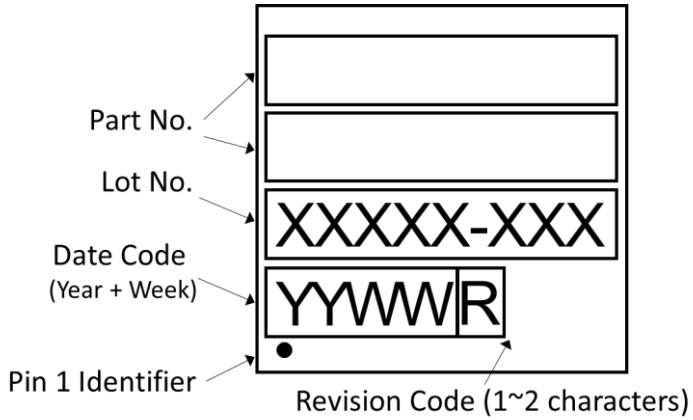
## 5.8 Device marking

**Figure 40. Marking example**

**LQFP100, LQFP64, LQFP48, QFN48, QFN36**




**QFN32**




(1) Not to scale.

## 5.9 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6mm thickness. They are guaranteed by design, not tested in production.

**Table 61. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP100 – 14 x 14 mm | 75.6 | °C/W |
| | Thermal resistance junction-ambient LQFP64 – 10 x 10 mm | 84.0 | |
| | Thermal resistance junction-ambient LQFP64 – 7 x 7 mm | 92.4 | |
| | Thermal resistance junction-ambient LQFP48 – 7 x 7 mm | 92.4 | |
| | Thermal resistance junction-ambient QFN48 – 6 x 6 mm | 57.0 | |
| | Thermal resistance junction-ambient QFN36 – 6 x 6 mm | 57.0 | |
| | Thermal resistance junction-ambient QFN32 – 4 x 4 mm | 71.3 | |

# 6 Part numbering

**Table 62. AT32A423 series part numbering**

Examples: AT32 A 4 2 3 R C T 7 -7

**Product family**

AT32 = ARM®-based 32-bit microcontroller

**Product type**

A = Automotive AEC Q-100 certification

**Core**

4 = Cortex®-M4

**Product series**

2 = Value line

**Product application**

3 = CAN + OTG series

**Pin count**

V = 100 pins R = 64 pins

C = 48 pins T = 36 pins

K = 32 pins

**Internal Flash memory size**

C = 256 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

**Package type**

T = LQFP

U = QFN

**Temperature range**

7 = -40 °C to +105 °C

**Package information**

-7 = LQFP64 - 7 x 7 mm

-4 = QFN32 - 4 x 4 mm

Blank = other packages

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

# 7 Document revision history

Table 63. Document revision history

| Date | Version | Revision note |
|---|---|---|
| 2024.4.26 | 2.00 | Initial release. |

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