ARM®-based 32-bit Cortex®-M4 MCU+FPU with 64 to 256 KB Flash, 12 timers, 2 ADCs, 13 communication interfaces (USBFS, 2 CANs)

Features

- **Core: ARM® 32-bit Cortex®-M4 CPU**
  - 200 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 64 to 256 KBytes of internal Flash memory
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - SPIM interface: Extra interfacing up to 16 Mbytes of the external SPI Flash (as instruction/data memory)
  - Up to 64 KBytes of SRAM
- **Power control (PWC)**
  - 2.6 to 3.6 V supply
  - Power on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep, and Standby modes
  - V_{BAT} supply for LEXT, RTC, and forty-two 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal (HEXT)
  - 48 MHz internal factory-trimmed clock (HICK), 1 % accuracy at T_A = 25 °C and 2.5 % accuracy at T_A = -40 to +105 °C, with automatic clock calibration (ACC)
  - 32 kHz crystal (LEXT)
  - Low-speed internal clock (LICK)
- **Analog**
  - 2 x 12-bit 2 MSPS A/D converters, up to 16 input channels
  - Temperature sensor (V_{TS}), internal reference voltage (V_{INTRV})
- **DMA: 14-channel DMA controller**
- **Up to 55 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 12 timers (TMR)**
  - Up to 2 x 16-bit motor control PWM advanced timers with dead-time generator and emergency stop
  - Up to 5 x 16-bit timers + 2 x 32-bit timers, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **Up to 13 communication interfaces**
  - Up to 2 x I²C interfaces, support SMBus/PMBus
  - Up to 5 x USARTs, support ISO7816 interface, LIN, IrDA capability, modem control
  - Up to 2 x SPIs (36 Mbit/s), all with I²S interface multiplexed
  - Up to 2 x CAN interfaces (2.0B Active)
  - USB 2.0 full speed interface supporting crystal-less
  - SDIO interface
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug mode**
  - Serial wire debug (SWD) and JTAG interfaces
- **Operating temperatures: -40 to +105 °C**
- **Packages**
  - LQFP64 10 x 10 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm
  - QFN32 4 x 4 mm

Table 1. AT32F413 device summary

Internal Flash	Part number
256 KBytes	AT32F413RCT7, AT32F413CCT7, AT32F413CCU7, AT32F413KCU7-4
128 KBytes	AT32F413RBT7, AT32F413CBT7, AT32F413CBU7, AT32F413KBU7-4
64 KBytes	AT32F413C8T7

Contents

List of Tables

List of figures

1 Descriptions

The AT32F413 series is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 200 MHz. The Cortex®-M4 core features a single-precision Floating Point Unit (FPU) that supports all ARM single-precision data processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F413 series incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, 64 Kbytes of SRAM), external SPI Flash (up to 16 Mbytes addressing capability), and a wide range of enhanced I/Os and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the sLib, functioning as a security area with code-executable only.

The AT32F413 series offers two 12-bit ADCs, five general-purpose 16-bit timers plus two general-purpose 32-bit timers, and up to two PWM timers for motor control. They also feature standard and advanced communication interfaces, including up to two I^2Cs, two SPIs (all multiplexed as I^2Ss), an SDIO, five USARTs/UARTs, an USBFS, and two CANs.

The AT32F413 series operates in the -40 to +105 °C temperature range, from a 2.6 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32F413 seriesmoffers devices in different package types. They are fully pin-to-pin, software and functionality compatible among the entire AT32F413 series devices, except that the configurations of peripherals are not completely identical, depending on the package types.

Table 2. AT32F413 features and peripheral counts

Part Number		AT32F413xxU7-4		AT32F413xxU7		AT32F413xxT7				
		KB	KC	CB	CC	C8	CB	CC	RB	RC
CPU frequency (MHz)		200								
Int. Flash (1)(2)	ZW (KBytes)	96		96		64	96		96	
	NZW (KBytes)	32	160	32	160	0	32	160	32	160
	Total (KBytes)	128	256	128	256	64	128	256	128	256
SRAM (KBytes)[2]		32 / 64 / 16 (configurable)				32	32 / 64 / 16 (configurable)			
SPIM[3]		1 ch / up to 16 MB								
Timers	Advanced-control[4]	1	1	1	2	1	1	2	1	2
	32-bit general-purpose	2		2		2			2	
	16-bit general-purpose	5		5		5			5	
	SysTick	1		1		1			1	
	WDT	1		1		1			1	
	WWDT	1		1		1			1	
	RTC	1		1		1			1	
Communication	I^2C	2		2		2			2	
	SPI[5]	2		2		2			2	
	I^2S (half-duplex) [5]	2[6]		2[6]		2[5]			2	
	USART+UART	2[7]+0		3+0		3+0			3+2	
	SDIO	1[8]		1[8]		1[7]			1	
	USBFS device	1		1		1			1	
	CAN	2		2		2			2	
Analog	12-bit ADC numbers/channels	2								
		10		10		10			16	
GPIO		27		39		39			55	
Operating temperatures		-40 to +105 °C								
Packages		QFN32 4 x 4 mm		QFN48 6 x 6 mm		LQFP48 7 x 7 mm			LQFP64 10 x 10 mm	

(1) ZW = zero wait-state, up to SYSCLK 200 MHz
NZW = non-zero wait-state
(2) The internal Flash and SRAM sizes are configurable with user system data. Take the AT32F413RCT7 as an example, on which the Flash/SRAM can be configured into three options below:
- ZW: 96 KBytes, NZW: 160 KBytes, SRAM: 32 KBytes (factory-shipping default);
- ZW: 64 KBytes, NZW: 192 KBytes, SRAM: 64 KBytes;
- ZW: 112 KBytes, NZW: 144 KBytes, SRAM: 16 KBytes.

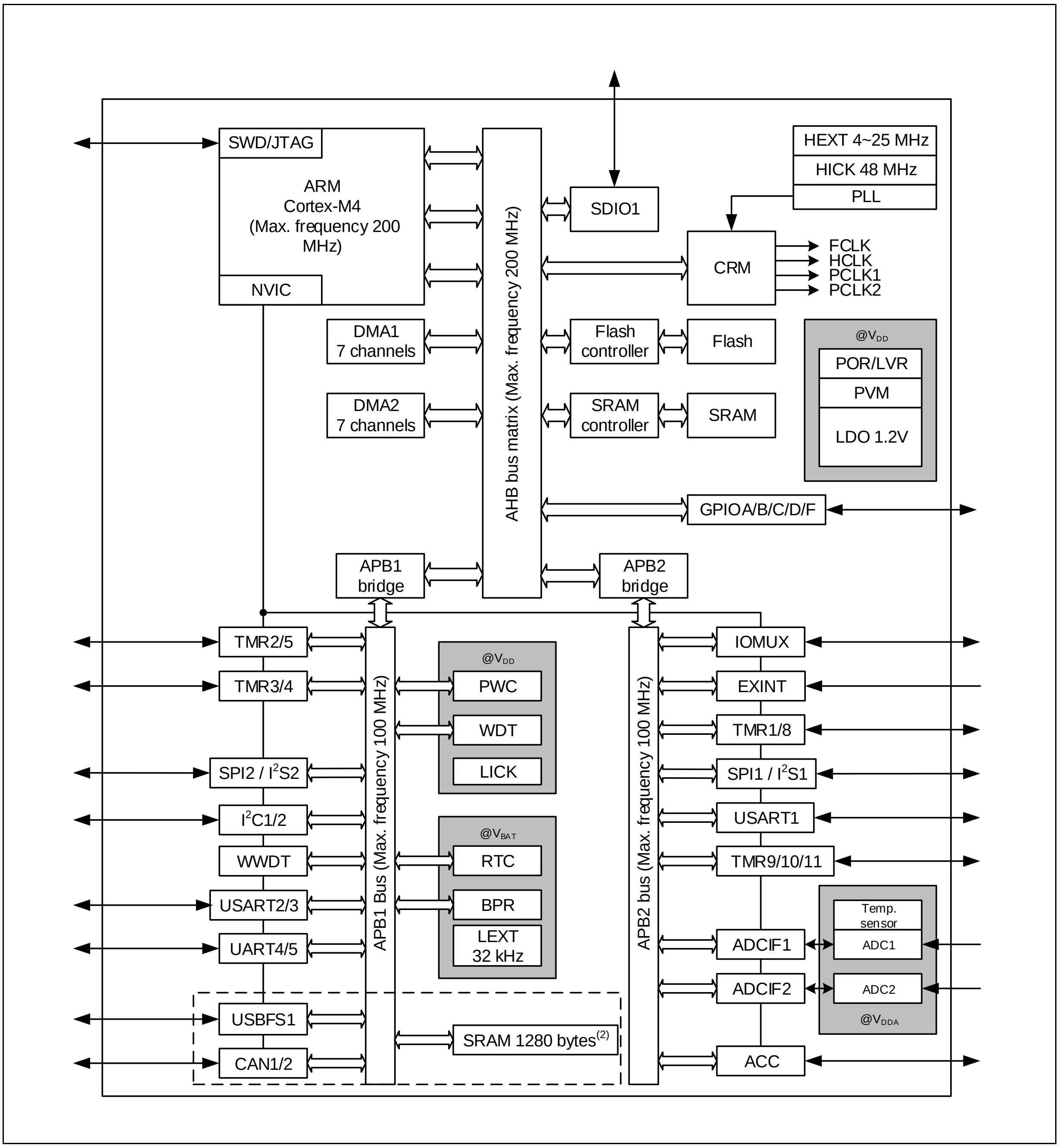
(3) SPIM = External SPI Flash memory extension (for both program execution and data storage) with encryption capability.
(4) For advanced-control timers, AT32F413RCT7 and AT32F413CCx7 support TMR1 and TMR8, others support only TMR1.
(5) Half-duplex I^2S shares the same pin with SPI.
(6) For LQFP48, QFN48 and QFN32 packages, only I^2S1 supports MCK pin.
(7) USART3 is not available on QFN32 packages.
(8) For LQFP48, QFN48 and QFN32 packages, SDIO supports maximum 4-bit (D0~D3) mode.

2 Functional overview

2.1 ARM® Cortex®-M4 with FPU

The ARM Cortex®-M4 processor is the latest generation of ARM processors for embedded systems. It is a 32-bit RISC processor that features exceptional code efficiency, outstanding computational performance and advanced interrupt response mechanism. The processor supports a set of DSP instructions which enable efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up floating point calculation while avoiding saturation. *Figure 1* shows the general block diagram of the AT32F413.

Figure 1. AT32F413 block diagram



(1) USBFS and CAN share dedicated 1280-Byte buffers, which offer four configuration options:

- USBFS1: 1280 Bytes ;
- USBFS1: 1024 Bytes, CAN1: 256 Bytes;
- USBFS1: 1024 Bytes, CAN2: 256 Bytes;
- USBFS1: 768 Bytes, CAN1: 256 Bytes, CAN2: 256 Bytes.

2.2 Memory

2.2.1 Internal Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data. Any part of the embedded Flash memory can be protected by the sLib (security library), a security area that is code-executable only but non-readable. The sLib is a mechanism designed to protect the intelligence of solution vendors and facilitate the second-level development by customers.

The AT32F413 provides an extra interface called SPIM (SPI memory), which interfaces the external SPI Flash memory for program and data storage. With up to 16 MBytes addressing capability, SPIM can be used as an extensive Flash memory Bank 3. Besides, SPIM can be encrypted through the User System Data block to ensure data security, and the encryption range can be configured through the corresponding control register.

There is another 18-KByte boot code area in which the bootloader is stored.

A User System Data block is included, which is used to configure such hardware behaviors as read/erase/write protection and watchdog self-enable. User System Data allows to set erase/write and read protection individually.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the entire 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 Embedded SRAM

The device offers up to 64 Kbytes of embedded SRAM that is accessible (read/write) at CPU clock speed with 0 wait states.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F413 series embeds a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus 16 interrupt lines of the Cortex®-M4 core. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 19 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.6～3.6 V: external power supply for GPIOs and the internal block such as regulator (LDO), provided externally through V_{DD} pins.
- V_{DDA} = 2.6～3.6 V: external analog power supply for ADCs. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8～3.6 V: power supply for V_{BAT} domain through an external battery or external super capacitor, or through V_{DD} when the external battery or super capacitor is not present. V_{BAT} (through power switch) supplies RTC, external crystal 32 kHz (LEXT), and battery powered registers (BPR) when V_{DD} is not present.

2.4.2 Reset and power voltage monitor (POR / LVR / PVM)

The device has an integrated power-on reset (POR)/low voltage reset (LVR) circuitry. It is always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has two operating modes: normal and power down.

- Normal mode: It is used in Run/Sleep mode and in Deepsleep mode;
- Power-down mode: It is used in Standby mode: The regulator output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

The LDO operates always in normal mode after reset.

2.4.4 Low-power modes

The AT32F413 supports three low-power modes:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep mode**

  Deepsleep mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock, and the HEXT crystal oscillators. The voltage regulator can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, the RTC alarm or the USBFS wakeup signals.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire LDO power domain is powered off. The PLL, the HICK clock and the HEXT crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for RTC registers, the BPR domain registers and Standby circuitry.

  The device leaves Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, IWDG and the corresponding clock sources are not stopped while entering Deepsleep or Standby mode.

2.5 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from the internal Flash memory;
- Boot from boot code area;
- Boot from embedded SRAM.

The bootloader is stored in boot code area. It is used to reprogram the Flash memory through USART1, USART2, or USBFS1. Of them, USBFS1 supports crystal-less operation. If SPIM_IO0/1 pins are mapped on USB pins, the Flash memory Bank 3 cannot be reprogrammed through USBFS1. *Table 3* presents AT32F413 pin configurations relative to Bootloader.

Table 3. Bootloader pin configurations

Peripheral	Pin
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX(1) PA3: USART2_RX(1)
USBFS1	PA11: USBFS1_D- PA12: USBFS1_D+

(1) Note that pins used are not 5 V tolerant.

2.6 Clocks

On reset, the internal 48 MHz clock (HICK) divided by 6 (that is 8 MHz) is selected as the default CPU clock. The application can select an external 4 to 25 MHz clock (HEXT) source as a system clock. This clock can be monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system take the same action as soon as HEXT fails when it is used as the source of PLL.

Several prescalers are available to allow the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 200 MHz. The maximum allowed frequency of the APB domains is 100 MHz.

The AT32F413 series embeds an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK clock, assuring the most precise accuracy of the HICK over the full operating temperatures.

2.7 General-purpose inputs / outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as multiple peripheral function. Most of the GPIO pins are shared with digital or analog multiple functions. All GPIOs are high current-capable.

The GPIO configuration can be locked, if needed, in order to avoid false writing to the GPIO registers by following a specific sequence.

2.8 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details, refer to *Table 5*, which gives a list of remappable alternate functions and the pins onto which they can be remapped. See the AT32F413 reference manual for software configurations.

2.9 Direct Memory Access Controller (DMA)

The device features two general-purpose dual-port DMAs (7 channels for DMA1 and 7 channels for DMA2). They are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA request logic, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^{2}C, USART, general-purpose and advanced-control timers TMRx, I^{2}S, SDIO, and ADC.

2.10 Timers (TMR)

The AT32F413 device includes two advanced timers, seven general-purpose timers, two basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 4. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels
TMR1, TMR8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TMR2, TMR5	16-bit or 32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR3, TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR9	16-bit	Up	Any integer between 1 and 65536	No	2	No
TMR10, TMR11	16-bit	Up	Any integer between 1 and 65536	No	1	No

2.10.1 Advanced timers (TMR1 and TMR8)

The two advanced timers (TMR1 and TMR8) can each be seen three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable dead-time insertion. Each of these timers can also be seen as a complete general-purpose timer.

Their four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-cycle mode output

If configured as standard 16-bit timers, they have the same features as the TMRx timers. If configured as 16-bit PWM generators, they have full modulation capability (0 to 100%).

In debug mode, the counter can be frozen and the PWM output can be disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose timers which have the same architecture. The advanced timer can therefore work together with the general-purpose timers via the timer link feature for synchronization or event chaining.

2.10.2 General-purpose timers (TMRx)

There are seven synchronizable general-purpose timers embedded in the AT32F413 series.

- **TMR2, TMR3, TMR4, and TMR5**

  The AT32F413 has four full- featured general-purpose timers: TMR2, TMR3, TMR4, and TMR5. The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload up/down counter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture/output compare, PWM or one-cycle mode outputs.

  These general-purpose timers can work with the advanced timers via the link feature for synchronization or event chaining. In debug mode, their counter can be frozen. Any of these general-purpose timers can be used to generate PWM outputs. Each timer has its individual DMA request mechanism.

  These timers are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

- **TMR9**

  TMR9 is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TMR10 and TMR11**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channel for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

2.10.3 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. Its features include:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HICK or HICK/8)

2.11 Watchdog (WDT)

The watchdog consists of a 12-bit down counter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabled through User System Data. The counter can be frozen in debug mode.

2.12 Window watchdog (WWDT)

The window watchdog embeds a 7-bit down counter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.13 Real-time clock (RTC) and battery powered registers (BPR)

The RTC and the battery powered registers are supplied through a power switch that is powered either from V_{DD} When present or from the V_{BAT} pin. The battery powered registers are forty-two 16-bit registers used to store 84 bytes of user application data. They are not reset by a system, power reset or when the device wakes up from Standby mode.

The real-time clock consists of a continuous-running counter.The RTC provides clock calendar, and alarm interrupt and periodic interrupt functions through software. It is clocked by a 32.768 kHz external crystal (LEXT), the internal low-power RC oscillator (LICK), or the high-speed external clock (HEXT) divided by 128. The RTC can be calibrated using a divied-by-64 output of TAMPER pin to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter that allows long time measurement with the help of the compare register. A prescaler is used as the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.14 Communication interfaces

2.14.1 Serial peripheral interface (SPI)

There are two SPI interfaces able to communicate at up to 36 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The prescaler generates multiple master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card/MMC/SDHC modes. All SPIs can be served by the DMA controller.

2.14.2 Inter-integrated sound interface (I^2S)

Two standard I^2S interfaces (multiplexed with SPI) are available which can be operated in master or slave mode in half-duplex mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When I^2S is configured in master mode, the master clock can be output at 256 times the sampling frequency. All I^2Ss can be served by the DMA controller.

2.14.3 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32F413 series embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2, and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. These five interfaces are able to communicate at a speeds of up to 6.25 Mbit/s.

USART1, USART2, and USART3 provide hardware management of the CTS and RTS signals. They also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except UART5.

2.14.4 Inter-integrated-circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multi-master and slave modes. They support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz). For more details about the complete solution, please contact your local Artery sales representative.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.14.5 Secure digital input / output interface (SDIO)

One SD/SDIO/MMC host interface is available to support MultiMediaCard System Specification Version 4.2 in three different data bus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different data bus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.14.6 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bit rate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive buffers with 3 stages, and 14 scalable filter banks.

To guarantee CAN transmission quality, the CAN 2.0 protocol states that its clock souce must come from the HEXT-based PLL clock.

2.14.7 Universal serial bus full-speed (USBFS)

AT32F413 series embeds a USB full-speed device (12 Mbit/s) with integrated transceivers (PHY). It has software-configurable endpoint setting and suspend/resume support. The USB requires a dedicated 48 MHz clock that is generated by the HEXT-based PLL or directly from the 48 MHz HICK.

2.15 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.16 Analog-to-digital converter (ADC)

Two 12-bit analog-to-digital converters are embedded into AT32F413 devices and they share up to 16 external channels, performing conversions in single-shot or sequencel modes. In sequence mode, automatic conversion is performed on a selected group of analog channels.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hole
- Single-shot sample

The ADC can be served by the DMA controller.

The voltage monitoring feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced-control timers (TMR1 and TMR8) can be internally connected to the ADC regular trigger and injection trigger, respectively, to allow the application to synchronize ADC conversion and timers.

2.16.1 Temperature sensor (V_{TS})

The temperature sensor generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel that is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.16.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage source for ADC. The V_{INTRV} is internally connected to the ADC1_IN17 input channel.

2.17 Serial wire (SWD) / JTAG debug port

The ARM® SWJ-DP Interface is embedded, consisting of a serial wire and JTAG debug port. It enables either a serial wire debug or a JTAG probe to be connected to the target for programming and debug operation. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK.

3 Pin functional definitions

Figure 2. AT32F413 LQFP64 pinout

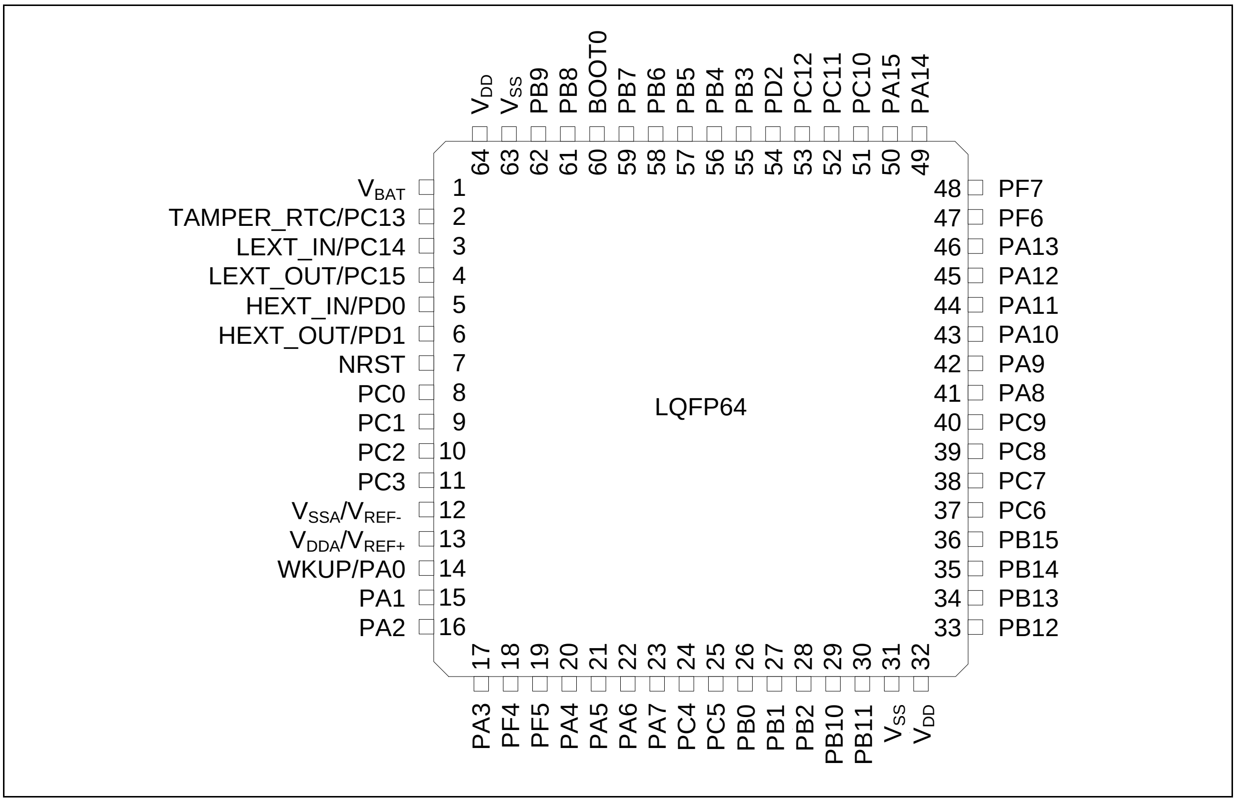


Figure 3. AT32F413 LQFP48 pinout

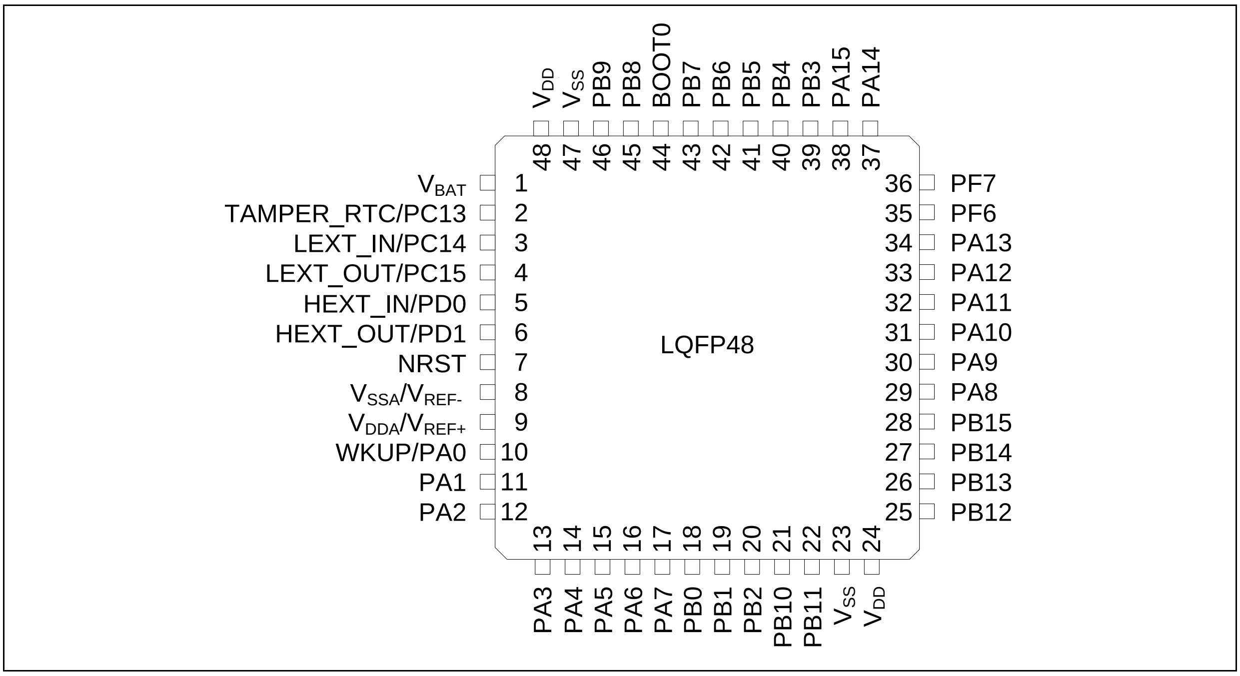


Figure 4. AT32F413 QFN48 pinout

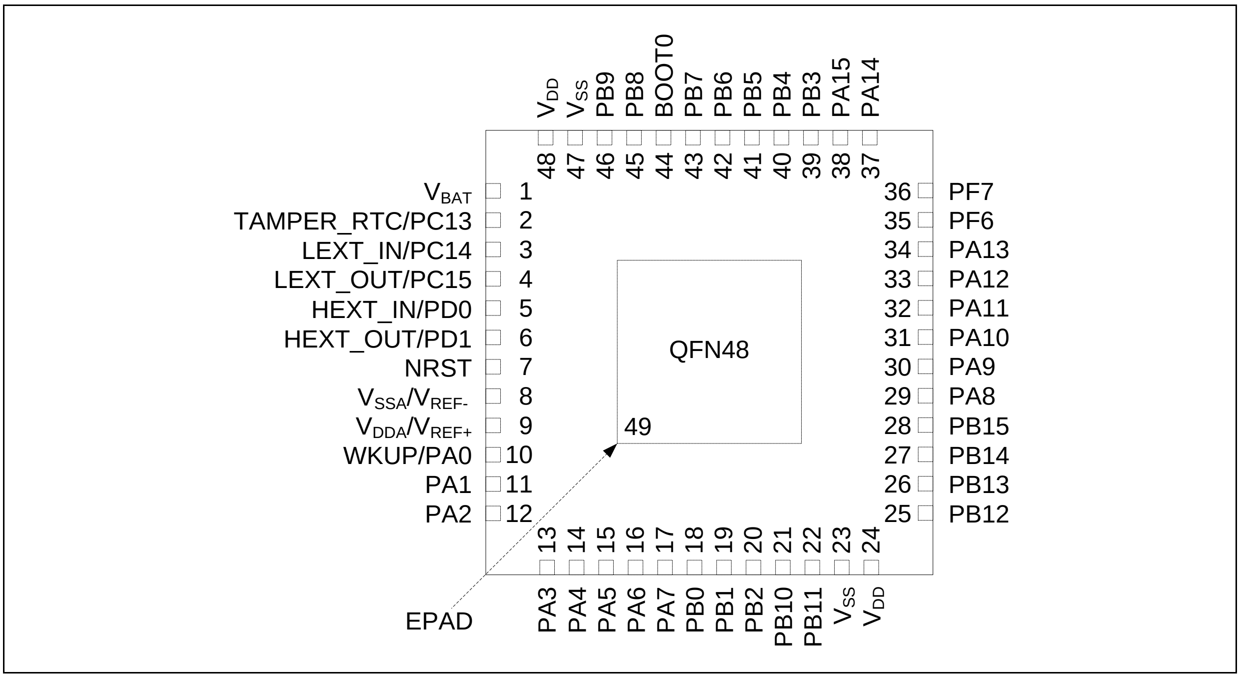
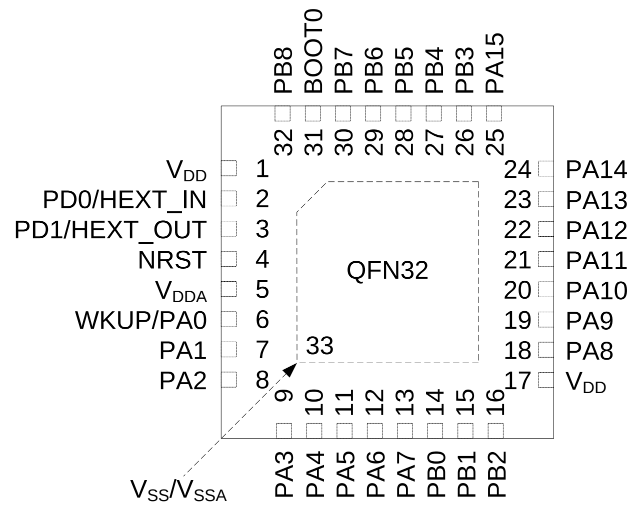


Figure 5. AT32F413 QFN32 pinout



The table below is the pin definition of the AT32F413. "-" presents there is no such pinout on the related package. The multi-functions list follows priority from high to low. In principle, the analog signals have \priority over the digital signals, and the digital output signals have priority over the digital input signals.

Table 5. AT32F413 series pin definitions

Pin number			Pin name	Type[1]	GPIO level[2]	Main functions	Alternate functions [3] [4]	
QFN32	LQFP48 QFN48	LQFP64					Default	Remap
-	1	1	V_{BAT}	S	-	V_{BAT}	-	-
-	2	2	TAMPER-RTC / PC13[5]	I/O	-	PC13[6]	TAMPER-RTC	-
-	3	3	LEXT_IN / PC14[5]	I/O	-	PC14[6]	LEXT_IN	-
-	4	4	LEXT_OUT / PC15[5]	I/O	-	PC15[6]	LEXT_OUT	-
2	5	5	HEXT_IN / PD0[8]	I/O	-	HEXT_IN	-	PD0[8]
3	6	6	HEXT_OUT / PD1[8]	I/O	-	HEXT_OUT	-	PD1[8]
4	7	7	NRST	I/O	-	NRST	-	-
-	-	8	PC0	I/O	-	PC0	ADC12_IN10	SDIO1_D0
-	-	9	PC1	I/O	-	PC1	ADC12_IN11	SDIO1_D1
-	-	10	PC2	I/O	-	PC2	ADC12_IN12	SDIO1_D2
-	-	11	PC3	I/O	-	PC3	ADC12_IN13	SDIO1_D3
-	8	12	V_{SSA} / V_{REF-}	S	-	V_{SSA} / V_{REF-}	-	-
5	9	13	V_{DDA} / V_{REF+}	S	-	V_{DDA} / V_{REF+}	-	-
6	10	14	PA0 / WKUP	I/O	-	PA0	ADC12_IN0 / WKUP / USART2_CTS / TMR2_CH1[7] / TMR2_EXT[7] / TMR5_CH1[7] / TMR8_EXT	-
7	11	15	PA1	I/O	-	PA1	ADC12_IN1 / USART2_RTS / TMR2_CH2[7] / TMR5_CH2[7]	-
8	12	16	PA2	I/O	-	PA2	ADC12_IN2 / USART2_TX / TMR2_CH3[7] / TMR5_CH3 / TMR9_CH1[7] /	SDIO1_CK
9	13	17	PA3	I/O	-	PA3	ADC12_IN3 / USART2_RX / TMR2_CH4[7] / TMR5_CH4 / TMR9_CH2[7]	SDIO1_CMD
-	-	18	PF4	I/O	FT	PF4	-	UART4_TX / TMR5_CH1
-	-	19	PF5	I/O	FT	PF5	-	UART4_RX / TMR5_CH2
10	14	20	PA4	I/O	-	PA4	ADC12_IN4 / USART2_CK / SPI1_CS[7] / I2S1_WS[7]	SDIO1_D4 / SDIO1_D0
11	15	21	PA5	I/O	-	PA5	ADC12_IN5 / SPI1_SCK[7] / I2S1_CK[7]	SDIO1_D5 / SDIO1_D1
12	16	22	PA6	I/O	-	PA6	ADC12_IN6 / SPI1_MISO[7] / TMR3_CH1[7] / TMR8_BRK	SDIO1_D6 / SDIO1_D2 / TMR1_BRK / TMR10_CH1
13	17	23	PA7	I/O	-	PA7	ADC12_IN7 /	SDIO1_D7 / SDIO1_D3 /

Pin number			Pin name	Type(1)	GPIO level(2)	Main functions	Alternate functions (3) (4)	
QFN32	LQFP48 QFN48	LQFP64					Default	Remap
							SPI1_MOSI(7) / I2S1_SD(7) / TMR3_CH2(7) / TMR8_CH1C	TMR1_CH1C / TMR11_CH1
-	-	24	PC4	I/O	-	PC4	ADC12_IN14	SDIO1_CK
-	-	25	PC5	I/O	-	PC5	ADC12_IN15	SDIO1_CMD
14	18	26	PB0	I/O	-	PB0	ADC12_IN8 / I2S1_MCK(7) / TMR3_CH3(7) / TMR8_CH2C	TMR1_CH2C
15	19	27	PB1	I/O	-	PB1	ADC12_IN9 / SPIM_SCK / TMR3_CH4(7) / TMR8_CH3C	TMR1_CH3C
16	20	28	PB2	I/O	FT	PB2 / BOOT1(9)	-	-
-	21	29	PB10	I/O	FT	PB10	I2C2_SCL(7) / USART3_TX(7)	SPIM_IO0 / TMR2_CH3
-	22	30	PB11	I/O	FT	PB11	I2C2_SDA(7) / USART3_RX(7)	SPIM_IO1 / TMR2_CH4
-	23	31	V_{SS}	S	-	V_{SS}	-	-
17	24	32	V_{DD}	S	-	V_{DD}	-	-
-	25	33	PB12	I/O	FT	PB12	USART3_CK(7) / I2C2_SMBA(7) / SPI2_CS(7) / I2S2_WS(7) / CAN2_RX(7) / TMR1_BRK(7)	-
-	26	34	PB13	I/O	FT	PB13	SPI2_SCK(7) / I2S2_CK(7) / USART3_CTS / CAN2_TX(7) / TMR1_CH1C(7) /	-
-	27	35	PB14	I/O	FT	PB14	USART3_RTS / SPI2_MISO(7) / TMR1_CH2C(7)	TMR9_CH1
-	28	36	PB15	I/O	FT	PB15	SPI2_MOSI(7) / I2S2_SD(7) / TMR1_CH3C(7) /	TMR9_CH2
-	-	37	PC6	I/O	FT	PC6	I2S2_MCK(7) / SDIO1_D6 / TMR8_CH1	TMR3_CH1
-	-	38	PC7	I/O	FT	PC7	SDIO1_D7 / TMR8_CH2	I2S2_MCK / TMR3_CH2
-	-	39	PC8	I/O	FT	PC8	SDIO1_D0 / TMR8_CH3	TMR3_CH3
-	-	40	PC9	I/O	FT	PC9	SDIO1_D1 / TMR8_CH4	I2C2_SDA / TMR3_CH4
18	29	41	PA8	I/O	FT	PA8	CLKOUT / USART1_CK / SPIM_CS / USBFS1_SOF / TMR1_CH1	I2C2_SCL
19	30	42	PA9	I/O	FT	PA9	USART1_TX(7) / TMR1_CH2	I2C2_SMBA
20	31	43	PA10	I/O	FT	PA10	USART1_RX(7) / TMR1_CH3	-
21	32	44	PA11	I/O	-	PA11	USBFS1_D- / SPIM_IO0(7) / USART1_CTS / CAN1_RX(7) / TMR1_CH4	-
22	33	45	PA12	I/O	-	PA12	USBFS1_D+ / SPIM_IO1(7) / USART1_RTS / CAN1_TX(7) / TMR1_EXT	-
23	34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	35	47	PF6	I/O	FT	PF6	-	I2C1_SCL / I2C2_SCL

Pin number			Pin name	Type(1)	GPIO level(2)	Main functions	Alternate functions (3) (4)	
QFN32	LQFP48 QFN48	LQFP64					Default	Remap
-	36	48	PF7	I/O	FT	PF7	-	I2C1_SDA / I2C2_SDA
24	37	49	PA14	I/O	FT	JTCK-SWCLK	-	PA14
25	38	50	PA15	I/O	FT	JTDI	-	PA15 / SPI1_CS / I2S1_WS / SPI2_CS / I2S2_WS TMR2_CH1 / TMR2_EXT /
-	-	51	PC10	I/O	FT	PC10	UART4_TX(7) / SDIO1_D2	USART3_TX
-	-	52	PC11	I/O	FT	PC11	UART4_RX(7) / SDIO1_D3	USART3_RX
-	-	53	PC12	I/O	FT	PC12	UART5_TX / SDIO1_CK	USART3_CK
-	-	54	PD2	I/O	FT	PD2	UART5_RX / SDIO1_CMD / TMR3_EXT	-
26	39	55	PB3	I/O	FT	JTDO	-	PB3 / SWO / SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / TMR2_CH2
27	40	56	PB4	I/O	FT	NJTRST	-	PB4 / SPI1_MISO / SPI2_MISO / I2C2_SDA / TMR3_CH1
28	41	57	PB5	I/O	FT	PB5	I2C1_SMBA	SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / CAN2_RX / TMR3_CH2
29	42	58	PB6	I/O	FT	PB6	I2C1_SCL(7) / SPIM_IO3 / TMR4_CH1	USART1_TX / CAN2_TX / I2S1_MCK
30	43	59	PB7	I/O	FT	PB7	I2C1_SDA(7) / SPIM_IO2 / TMR4_CH2	USART1_RX
31	44	60	BOOT0	I	-	BOOT0	-	-
32	45	61	PB8	I/O	FT	PB8	TMR10_CH1(7) / SDIO1_D4 / TMR4_CH3	I2C1_SCL / CAN1_RX
-	46	62	PB9	I/O	FT	PB9	TMR11_CH1(7) / SDIO1_D5 / TMR4_CH4	I2C1_SDA / CAN1_TX
-	47	63	V_{SS}	S	-	V_{SS}	-	-
1	48	64	V_{DD}	S	-	V_{DD}	-	-
-	-/49	-	EPAD	S	-	V_{SS}	-	-
33	-	-	V_{SS}/V_{SSA}	S	-	V_{SS}/V_{SSA}	-	-

(1) I = input, O = output, S = supply.

(2) FT = 5 V-tolerant I/O.

(3) Function availability depends on the chosen device. For example, if a certain part number has only one advanced timer, it is TMR1, see *Table 2*.

(4) If several peripherals are mapped onto the same GPIO port, only one of these peripherals can be enabled at the same time through the enable control bit (in the corresponding CRM peripheral clock enable register) in order to avoid conflicts.

(5) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: these IOs must not be used as a current source (e.g. to drive an LED).

(6) Main function after the first battery powered domain power-up. Later on, it depends on the contents of the battery powered registers even after reset (because these registers are not reset by the main reset). For details on how to manage these GPIOs, refer to the battery powered domain and register description sections in the AT32F413 reference manual.

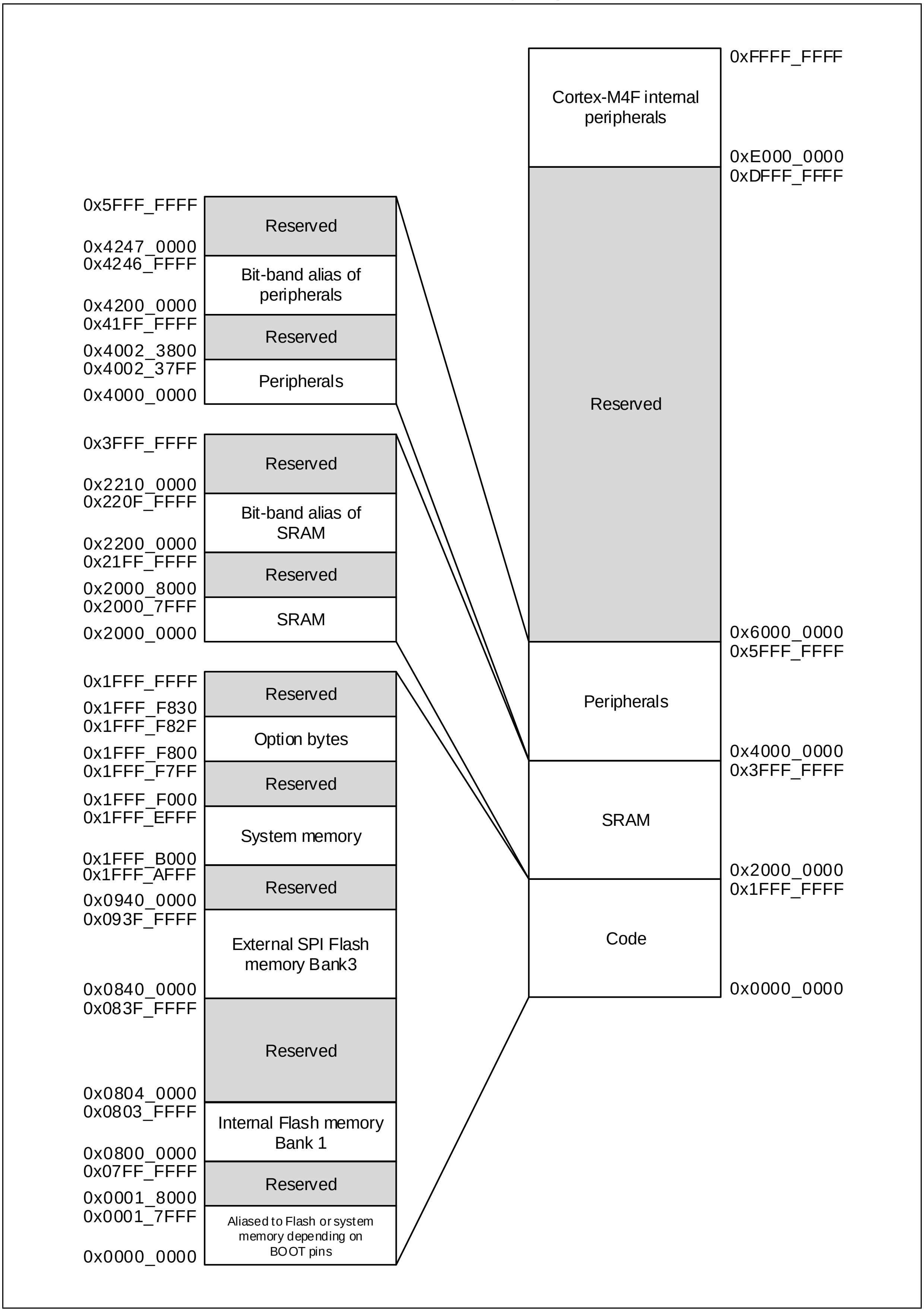
(7) This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the AT32F413 reference manual.

(8) The pins number 5 and 6 (LQFP64, LQFP48, and QFN48), and the pins number 2 and 3 (QFN32) are configured as HEXT_IN/HEXT_OUT after reset, the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to Alternate function I/O and debug configuration section in the AT32F413 reference manual.

(9) If boot from internal Flash memory and PB2 is not used, it is recommended to pull down to ground.

4 Memory mapping

Figure 6. Memory map



5 Electrical characteristics

5.1 Parameter conditions

5.1.1 Minimum and maximum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

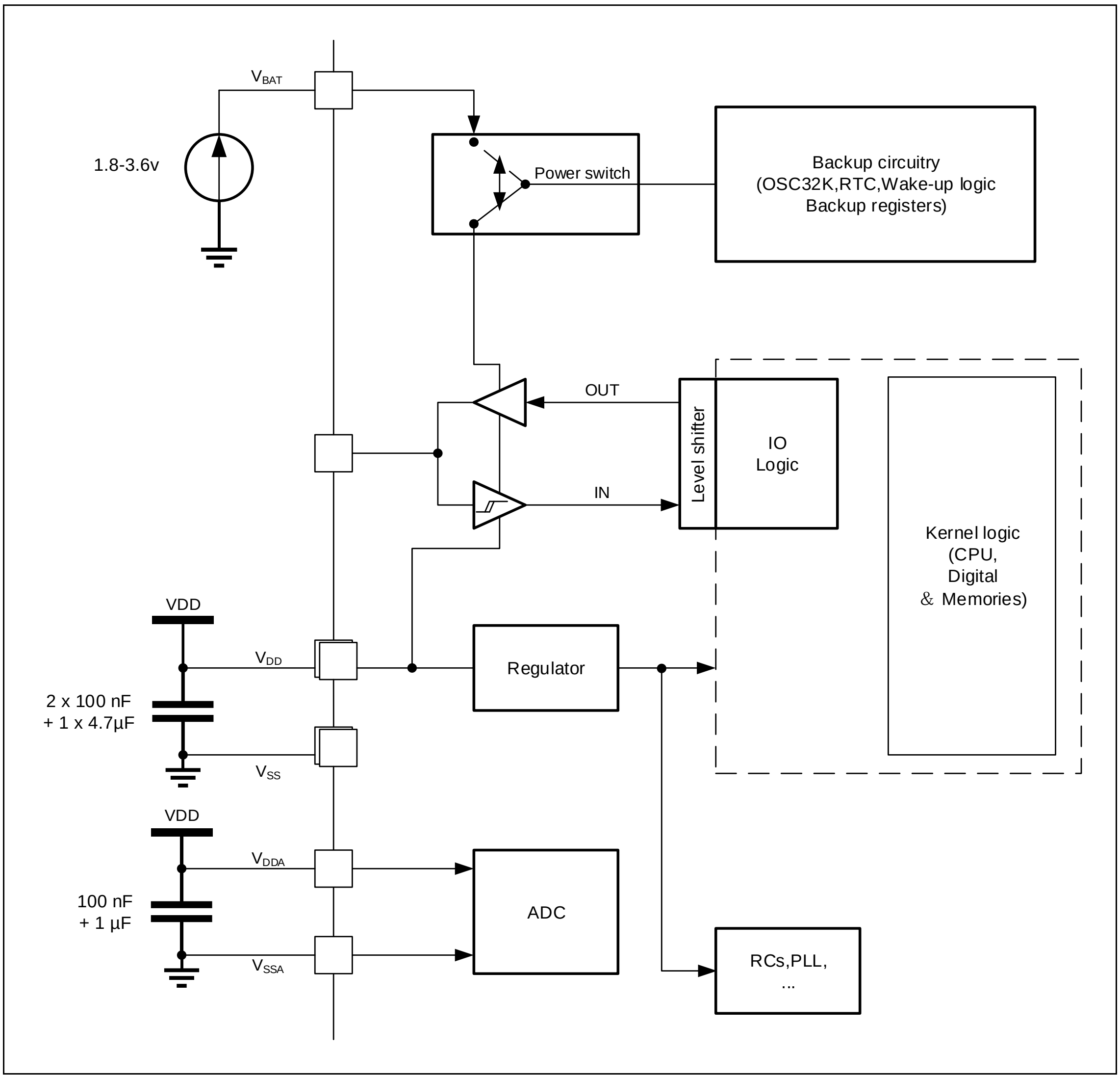
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

5.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

5.1.4 Power supply scheme

Figure 7. Power supply scheme



5.2 Absolute maximum values

5.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 6*, *Table 7*, and *Table 8*, it may cause permanent damage to the device. These are the maximum stress ratings only that the device could bear, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	4.0	V
V_{IN}	Input voltage on FT	V_{SS}-0.3	6.0	
	Input voltage on other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 7. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIOs and control pin	-25	

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

5.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test conforms to the JS-001-2017/JS-002-2014 standard.

Table 9. ESD values

Symbol	Parameter	Conditions	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2018	III	1000	

Static latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 10. Latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (200 mA)

5.3 Specifications

5.3.1 General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Bank 3 (SPIM) not used	0	200	MHz
		Bank 3 (SPIM) used	0	120	
f_{PCLK1}	Internal APB1 clock frequency	-	0	100	
f_{PCLK2}	Internal APB2 clock frequency	-	0	100	
V_{DD}	Digital operating voltage	-	2.6	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}	2.6	3.6	V
V_{BAT}	Battery power operating voltage	-	1.8	3.6	V
P_D	Power dissipation: T_A = 105 °C	LQFP64	-	289	mW
		LQFP48	-	313	
		QFN48	-	394	
		QFN32	-	334	
T_A	Ambient temperature	-	-40	105	°C

5.3.2 Operating conditions at power-up / power-down

Table 12. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞(1)	ms/V
	V_{DD} fall time rate		20	∞	µs/V

(1) If V_{DD} rising time rate is slower than 80 ms/V, the code could access the battery powered registers only after V_{DD} is higher than V_{POR} + 0.1V.

5.3.3 Embedded reset and power control block characteristics

Table 13. Embedded reset and power management block characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	1.95	2.16	2.45	V
V_{LVR}	Low voltage reset threshold	1.8(2)	2.0	2.25	V
$V_{LVRhyst}$	LVR hysteresis	-	160	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	8	-	ms

(1) Guaranteed by design, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 8. Power on reset and low voltage reset waveform

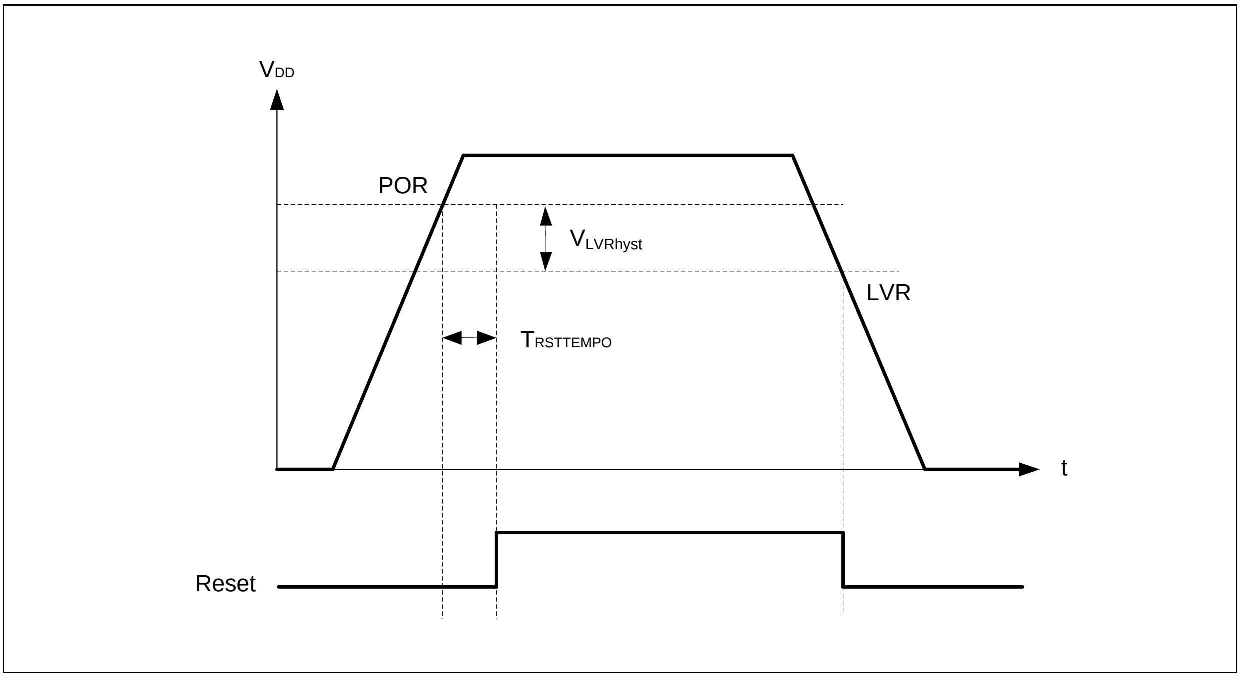


Table 14. Programmable voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold 1(PVMSEL[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge(1)	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge (2)	2.28	2.38	2.48	V
		Falling edge (2)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge (2)	2.38	2.48	2.58	V
		Falling edge (2)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge (2)	2.47	2.58	2.69	V
		Falling edge (2)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge (2)	2.57	2.68	2.79	V
		Falling edge (2)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge (2)	2.66	2.78	2.9	V
		Falling edge (2)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(2)	PVM hysteresis	-	-	100	-	mV

(1) PVMSEL[2:0] = 001 may be not available for its voltage detector level may be lower than V_{POR}.
(2) Guaranteed by characterization results, not tested in production.

5.3.4 Memory characteristics

Table 15. Internal Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
T_{PROG}	Programming time	-	50	200	μs
t_{SE}	Sector erase time (2 KB)	AT32F413xC	50	500	ms
	Sector erase time (1 KB)	AT32F413xB AT32F413x8	40	400	
t_{BKE}	Block erase time	-	0.8	10	s

(1) Guaranteed by design, not tested in production.

Table 16. Internal Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code. The current consumption is obtained by characterization results, not tested in production.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Prefetch is ON. (Reminder: This bit must be set before clock setting and bus prescaling.)
- When the peripherals are enabled:
  - If f_{HCLK} > 100 MHz: $f_{PCLK1} = f_{HCLK}/2$， $f_{PCLK2} = f_{HCLK}/2$， $f_{ADCCLK} = f_{PCLK2}/4$;
  - If $f_{HCLK} \leq$ 100 MHz， $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$
- Code executes in ZW area.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

Table 17. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Type: All peripherals enabled	Type: All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1)(2)	200 MHz	60.5	28.1	mA
			144 MHz	44.2	20.6	
			100 MHz	38.2	15.0	
			72 MHz	28.4	11.5	
			48 MHz	19.4	8.07	
			36 MHz	14.9	6.34	
			24 MHz	10.3	4.62	
			16 MHz	7.25	3.48	
			8 MHz	3.97	2.10	
			4 MHz	2.51	1.58	
			2 MHz	1.79	1.33	
			1 MHz	1.43	1.20	
			500 kHz	1.25	1.41	
			125 kHz	1.11	1.09	
		High speed internal clock (HICK)(2)	200 MHz	60.4	28.0	mA
			144 MHz	44.0	20.5	
			100 MHz	38.1	14.9	
			72 MHz	28.3	11.4	
			48 MHz	19.3	7.95	
			36 MHz	14.7	6.23	
			24 MHz	10.2	4.51	
			16 MHz	7.14	3.36	
			8 MHz	3.67	1.76	
			4 MHz	2.20	1.52	
			2 MHz	1.48	1.01	
			1 MHz	1.11	0.88	
			500 kHz	0.93	1.09	
			125 kHz	0.80	0.77	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Type		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1)(2)	200 MHz	48.3	6.51	mA
			144 MHz	35.3	5.02	
			100 MHz	32.1	4.16	
			72 MHz	23.9	3.73	
			48 MHz	16.4	2.89	
			36 MHz	12.6	2.46	
			24 MHz	8.79	2.04	
			16 MHz	6.26	1.77	
			8 MHz	3.29	1.07	
			4 MHz	2.08	0.98	
			2 MHz	1.48	0.93	
			1 MHz	1.18	0.91	
			500 kHz	1.03	0.90	
			125 kHz	0.92	0.89	
		High speed internal clock (HICK)(2)	200 MHz	48.2	6.40	mA
			144 MHz	35.2	4.90	
			100 MHz	31.9	4.05	
			72 MHz	23.8	3.61	
			48 MHz	16.3	2.76	
			36 MHz	12.5	2.34	
			24 MHz	8.67	1.92	
			16 MHz	6.14	1.64	
			8 MHz	3.17	0.95	
			4 MHz	1.96	0.85	
			2 MHz	1.35	0.80	
			1 MHz	1.05	0.78	
			500 kHz	0.90	0.77	
			125 kHz	0.79	0.76	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 19. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max T_A = 105 °C	Unit
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1), all peripherals enabled	200 MHz	69.1	mA
			144 MHz	52.0	
			100 MHz	46.0	
			72 MHz	35.6	
			48 MHz	26.2	
			36 MHz	21.4	
			24 MHz	16.7	
			16 MHz	13.5	
			8 MHz	10.1	
		High speed external crystal (HEXT)(1), all peripherals disabled	200 MHz	34.5	mA
			144 MHz	26.8	
			100 MHz	21.1	
			72 MHz	17.5	
			48 MHz	14.0	
			36 MHz	12.3	
			24 MHz	10.6	
			16 MHz	9.40	
			8 MHz	8.02	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 20. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max T_A = 105 °C	Unit
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled	200 MHz	56.5	mA
			144 MHz	42.8	
			100 MHz	39.6	
			72 MHz	31.0	
			48 MHz	23.1	
			36 MHz	19.1	
			24 MHz	15.1	
			16 MHz	12.4	
			8 MHz	9.32	
		High speed external crystal (HEXT)(1), all peripherals disabled	200 MHz	12.4	mA
			144 MHz	10.9	
			100 MHz	10.0	
			72 MHz	9.53	
			48 MHz	8.70	
			36 MHz	8.27	
			24 MHz	7.85	
			16 MHz	7.57	
			8 MHz	6.86	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 21. Typical and maximum current consumptions in Deepsleep and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max(2)			Unit
			V_{DD} = 2.6 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode	HICK and HEXT OFF (no WDT)	480	490	Refer to note (3)	3800	6670	μA
	Supply current in Standby mode	LEXT and RTC OFF	7.1	9.9	12.1	13.9	17.1	μA
		LEXT and RTC ON	7.7	11.6	12.9	14.9	18.3	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) The value may be several times the typical values due to process variation.

Figure 9. Typical current consumption in Deepsleep mode vs. temperature at different V_{DD}

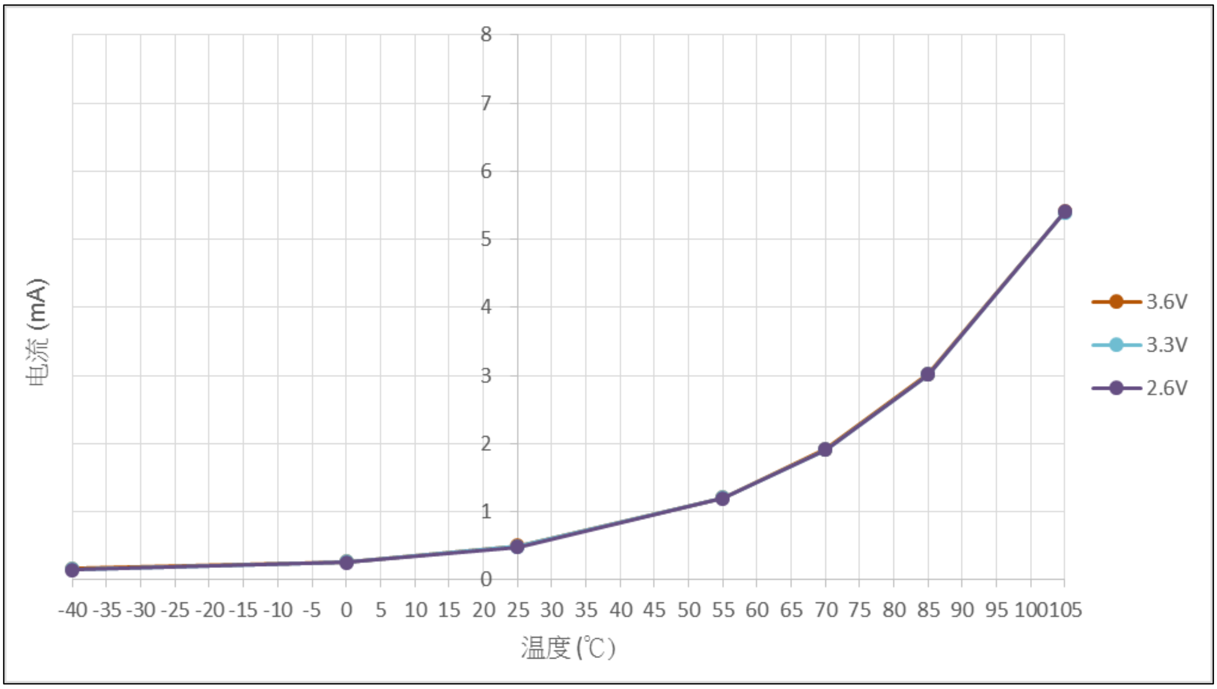


Figure 10. Typical current consumption in Standby mode vs. temperature at different V_{DD}

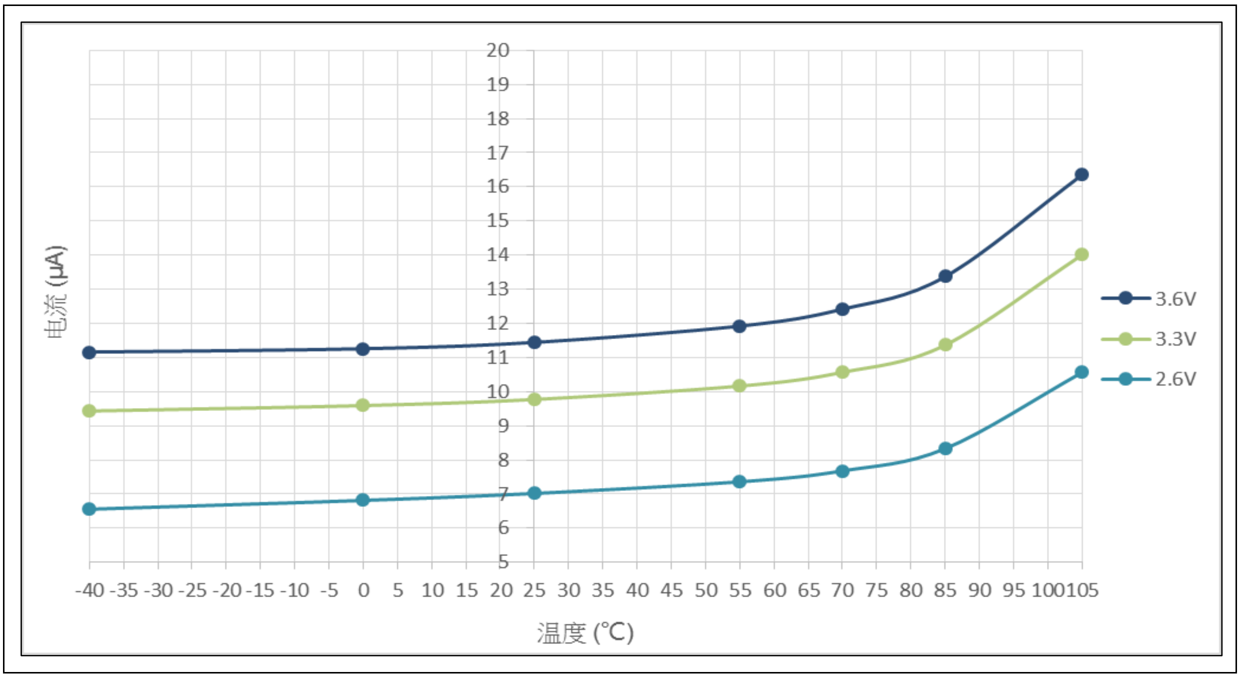
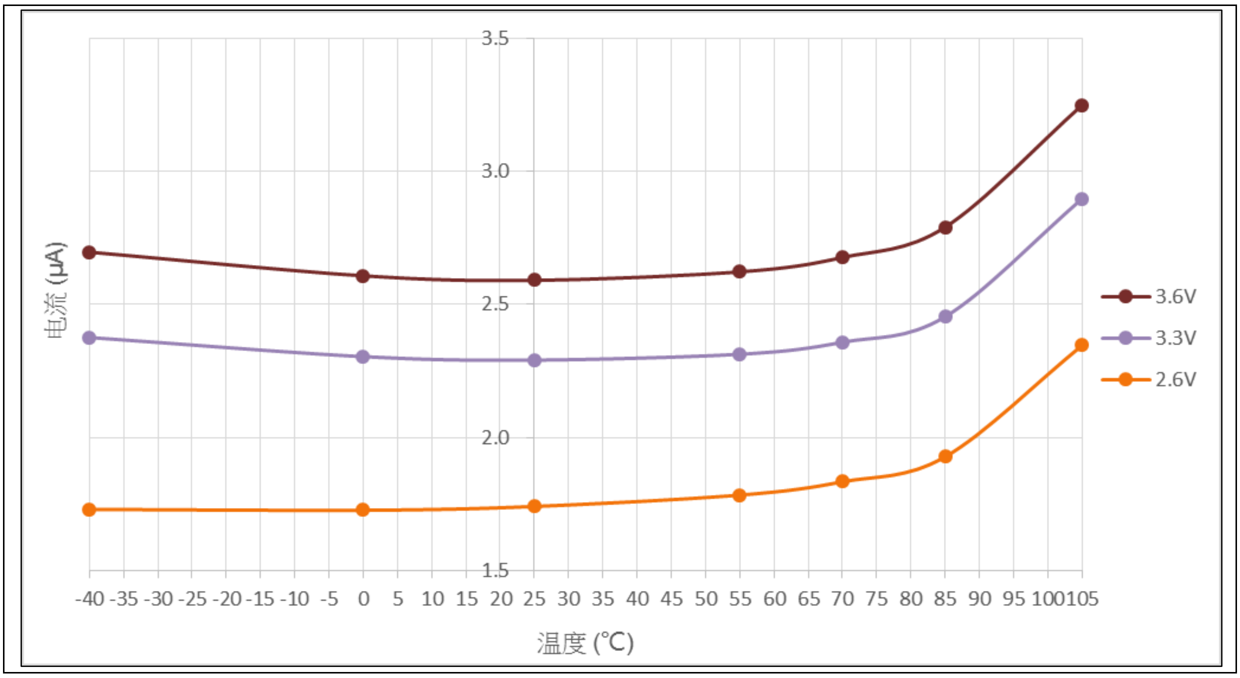


Table 22. Typical and maximum current consumptions on V_{BAT}

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			V_{BAT} = 2.0 V	V_{BAT} = 2.6 V	V_{BAT} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Supply current of V_{BAT}	LEXT and RTC ON, $V_{DD} < V_{LVR}$	1.5	1.7	2.3	2.8	3.0	3.5	µA

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 11. Typical current consumption on V_{BAT} with LEXT and RTC ON vs. temperature at different V_{BAT}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 23. Peripheral current consumption

Peripheral		Typ	Unit
AHB	DMA1	9.45	μA/MHz
	DMA2	9.58	
	GPIOA	1.22	
	GPIOB	1.20	
	GPIOC	1.29	
	GPIOD	1.23	
	GPIOF	1.19	
	CRC	1.57	
	SDIO1	18.5	
APB1	TMR2	8.65	
	TMR3	6.50	
	TMR4	6.57	
	TMR5	8.76	
	SPI2/I²S2	2.80	
	USART2	2.50	
	USART3	2.49	
	UART4	2.54	
	UART5	2.54	
	I²C1	2.47	
	I²C2	2.50	
	USBFS1	6.76	
	CAN1	3.92	
	CAN2	3.91	
	WWDT	0.44	
	PWC	0.41	
	BPR	73.6	
APB2	IOMUX	2.13	μA/MHz
	SPI1/I²S1	2.64	
	USART1	2.48	
	TMR1	9.23	
	TMR8	9.18	
	TMR9	3.80	
	TMR10	2.66	
	TMR11	2.62	
	ADC1	6.54	
	ADC2	6.35	
	ACC	0.97	

5.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

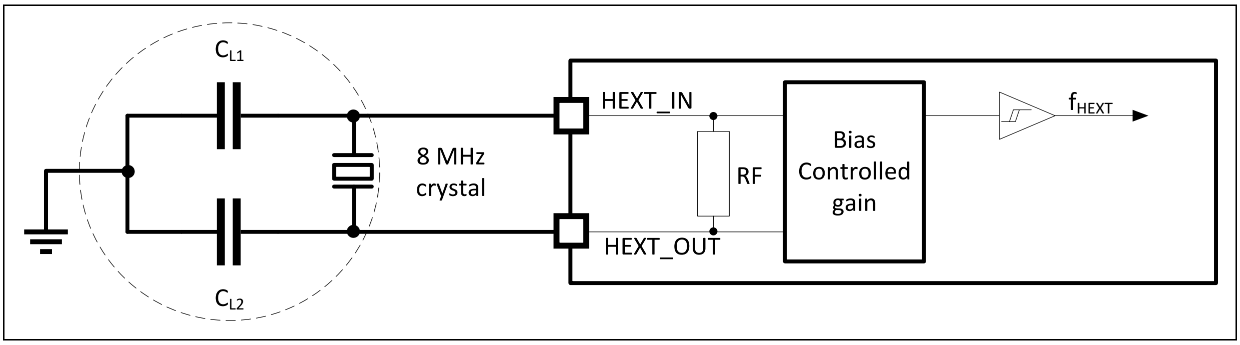
Table 24. HEXT 4-25 MHz crystal characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	V_{DD} is stabilized	-	1.2	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and select to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 12. HEXT typical application with an 8 MHz crystal



High-speed external clock generated from an external source

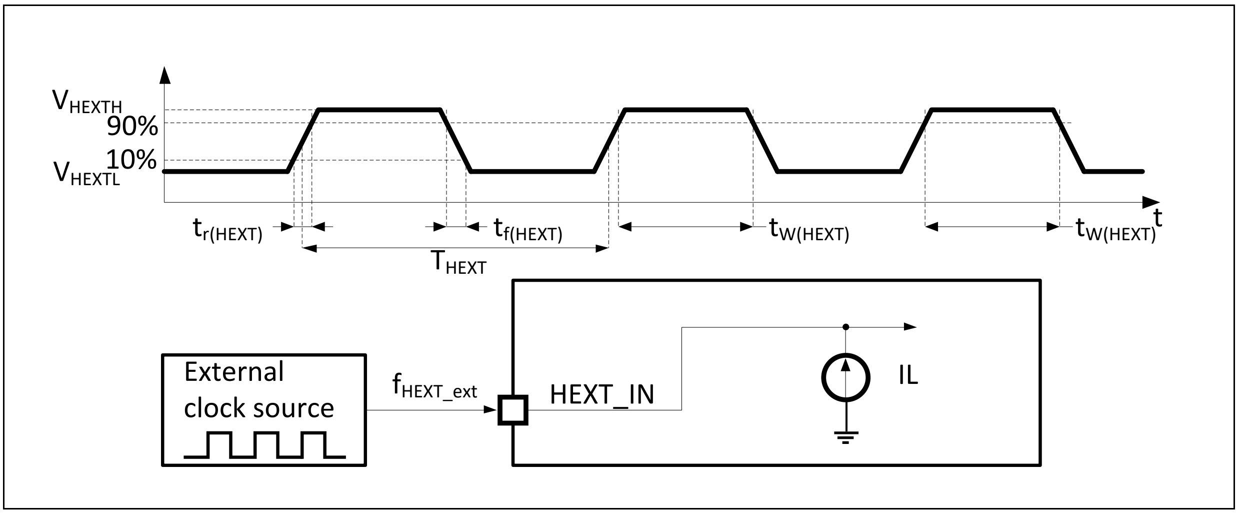
The characteristics given in the table below result from tests performed using a high-speed external clock source.

Table 25. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 13. HEXT external source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 26. LEXT 32.768 kHz crystal characteristics(1)(2)

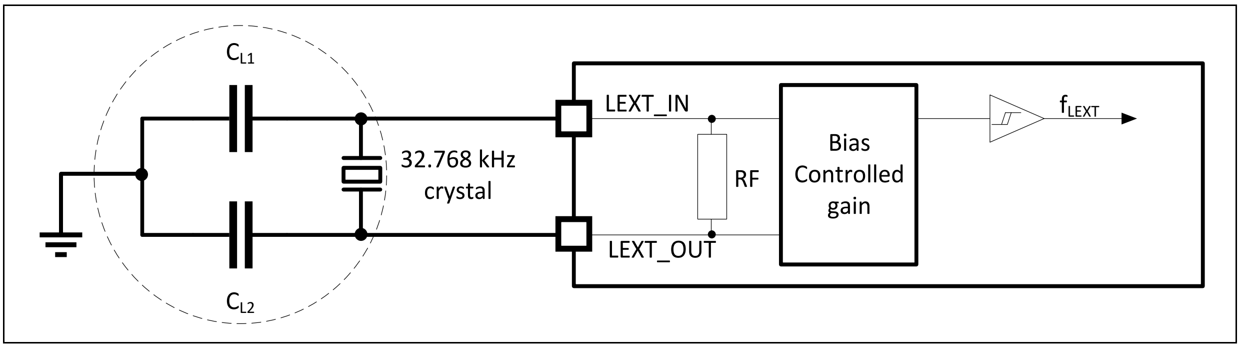
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	150	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 14. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

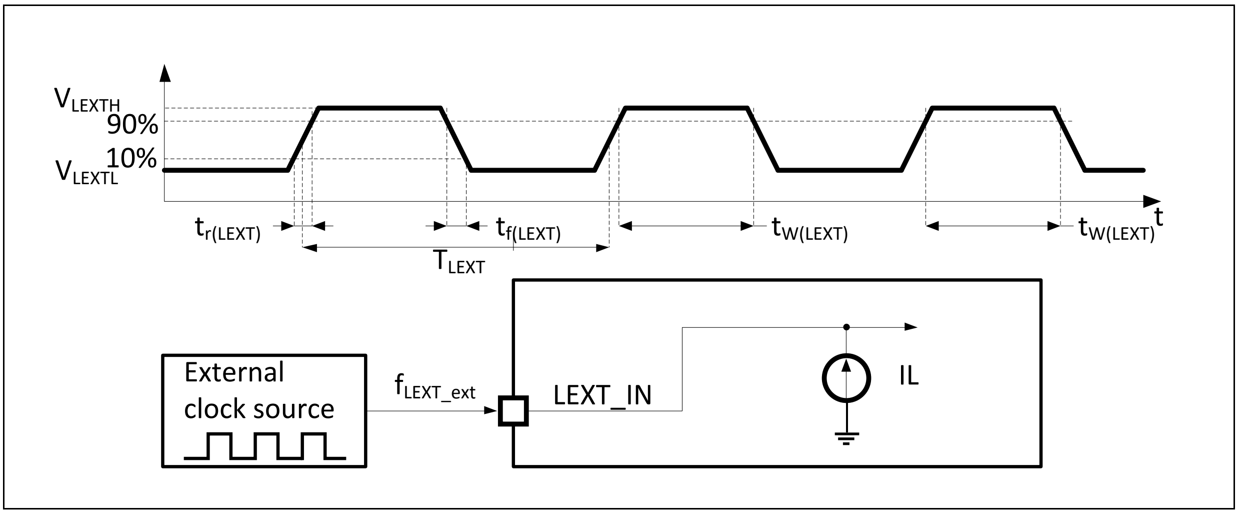
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 27. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 15. LEXT external source AC timing diagram



5.3.7 Internal clock source characteristics

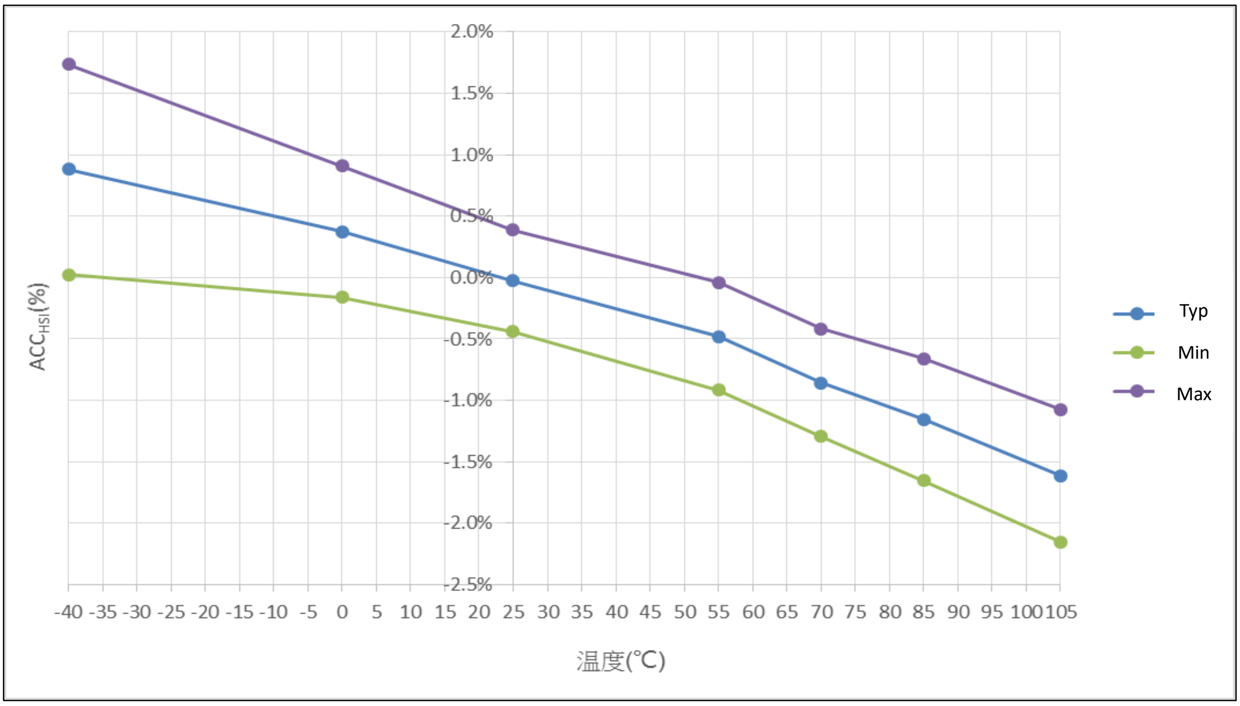
High-speed internal clock (HICK)

Table 28. HICK clock characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CRM_CTRL register		-	-	1	%
		ACC-trimmed		-	-	0.25	
		Factory-calibrated(2)	T_A = -40 ~ 105 °C	-2.5		2.5	%
			T_A = -40 ~ 85 °C	-2	-	2	
			T_A = 0 ~ 70 °C	-1.5	-	1.5	
			T_A = 25 °C	-1	-	1	
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-		-	-	10	µs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-		-	190	200	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 16. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 29. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	30	40	60	kHz

(1) Guaranteed by characterization results, not tested in production.

5.3.8 PLL characteristics

Table 30. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	200	MHz
t_{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Take care of using the appropriate multiplier factors to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

5.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: the clock source is the HICK.

Table 31. Low-power mode wakeup time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	3.3	μs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode	280	μs
$t_{WUSTDBY}$	Wakeup from Standby mode	3.6	ms

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 32. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforms to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional disturbance, V_{DD} and V_{SS} input has one 47 µF capacitor and each V_{DD} and V_{SS} pair 0.1 µF	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, HEXT, f_{HCLK} = 200 MHz, conforms to IEC 61000-4-4	4A（4kV）
		V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, HEXT, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	
		V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, HICK, f_{HCLK} = 200 MHz, conforms to IEC 61000-4-4	
		V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, HICK, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

5.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 33. GPIO static characteristics

Symb	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	–0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	Standard GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT GPIO input high level voltage	-		-	5.5	
V_{hys}	Standard GPIO Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
	FT GPIO Schmitt trigger voltage hysteresis(1)		5% V_{DD}	-	-	-
I_{lkg}	Input leakage current(2)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard GPIOs	-	-	±1	μA
		$V_{SS} \leq V_{IN} \leq$ 5.5V FT GPIOs	-	-	±10	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	60	70	100	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)(4) (5)	$V_{IN} = V_{DD}$	70	80	120	kΩ
C_{IO}	GPIO pin capacitance	-	-	5	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT, and FTa pins.
(4) Each of PA11 and PA12 has a weak pull-down resistor 330 kΩ which is permanently enabled.
(5) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in *Section 5.2.1*:

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Maximum sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 20 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Normal sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 35. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$	Pulse width of external signals detected by EXINT controller	10	-	ns

5.3.12 NRST pin characteristics

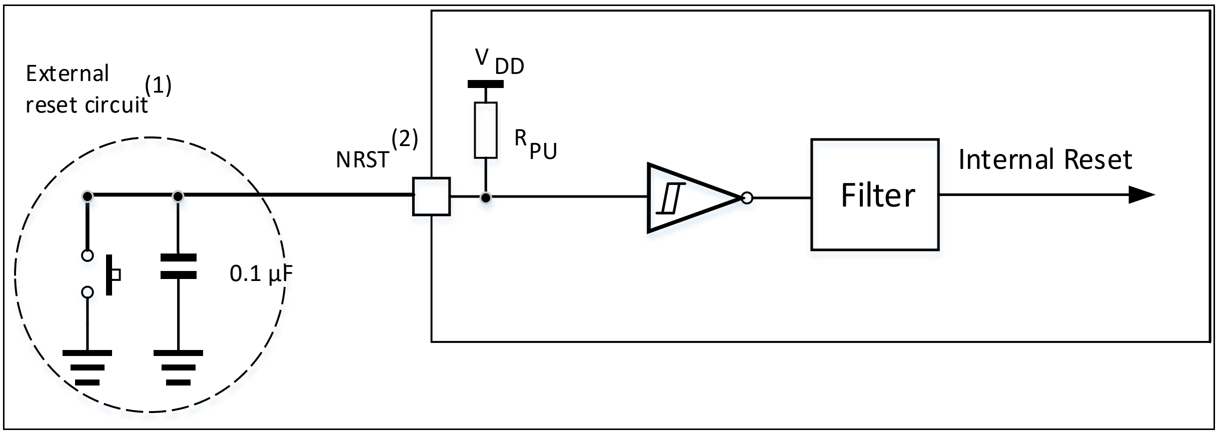
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$ (1)	NRST Schmitt trigger voltage hysteresis	-	-	500	-	mV
R_{PU}(2)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level inactive	-	-	-	33.3	µs
$t_{ILNV(NRST)}$(1)	NRST input low level active	-	66.7	-	-	µs

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 17. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the V_{IL} (NRST) max level specified in *Table 36*. Otherwise the reset will not be performed by the device.

5.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Table 37. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 200 MHz	5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}/2$	MHz
				50	MHz

5.3.14 SPI / SPIM characteristics

Table 38. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency[2][3]	SPI master mode	-	36	MHz
		SPI slave mode	-	32	
		SPIM	-	60	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(CS)}$[1]	CS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(CS)}$[1]	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$[1] $t_{w(SCKL)}$[1]	SCK high and low time	Master mode, prescaler = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}$[1]	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}$[1]		Slave mode	5	-	
$t_{h(MI)}$[1]	Data input setup time	Master mode	4	-	ns
$t_{h(SI)}$[1]		Slave mode	5	-	
$t_{a(SO)}$[1][4]	Data output access time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{dis(SO)}$[1][5]	Data output disable time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{v(SO)}$[1]	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$[1]	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{h(SO)}$[1]	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}$[1]		Master mode (after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 18. SPI timing diagram - slave mode and CPHA = 0

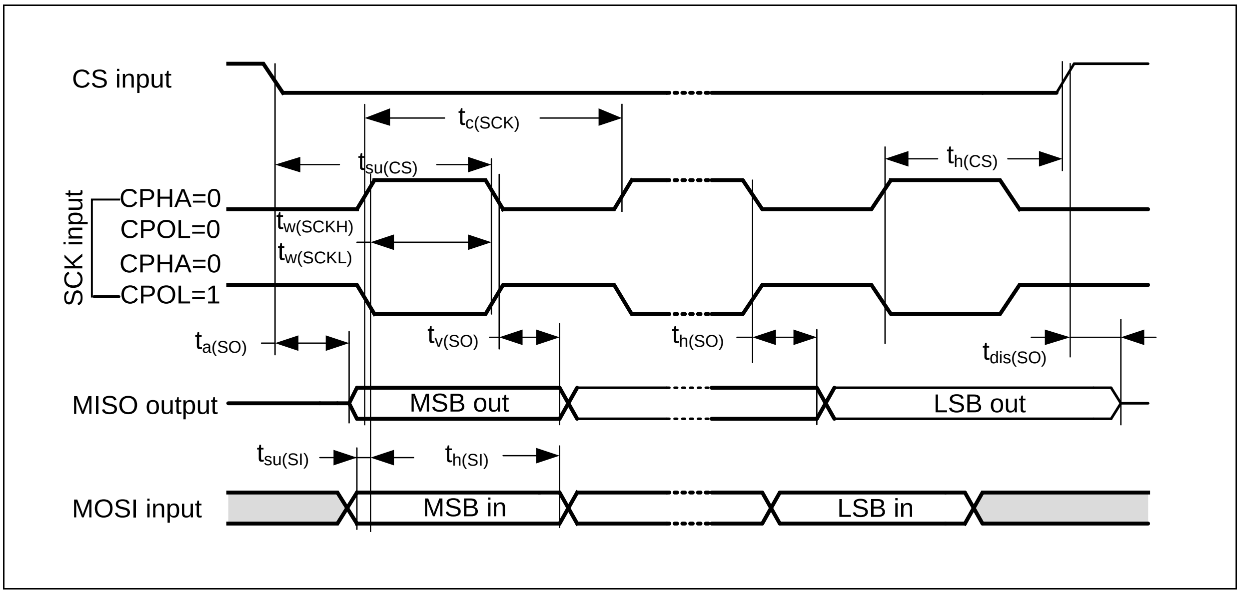


Figure 19. SPI timing diagram - slave mode and CPHA = 1

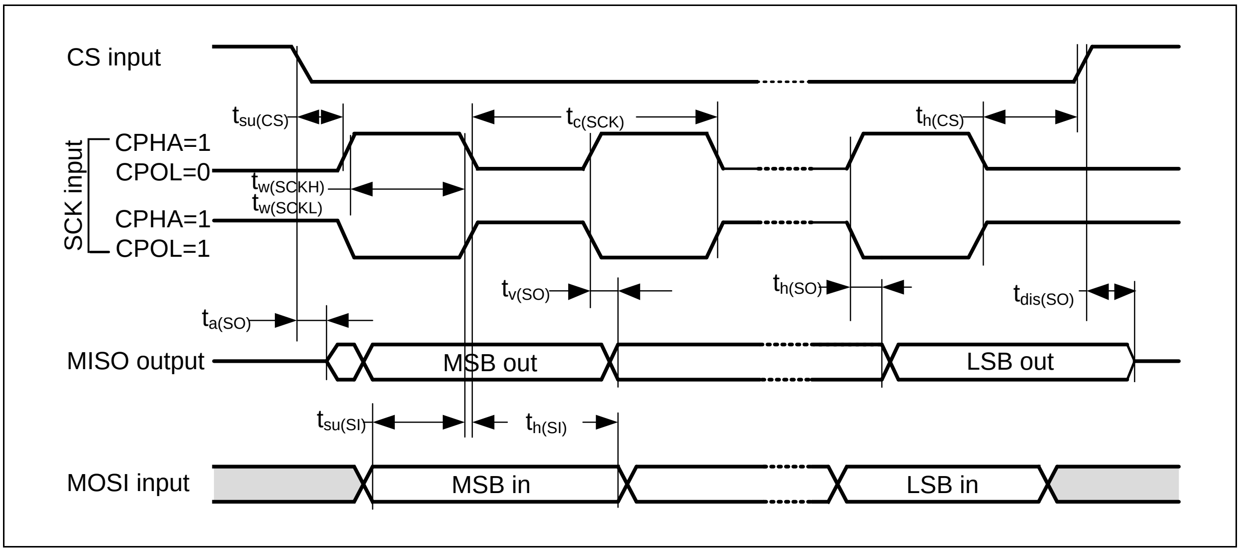
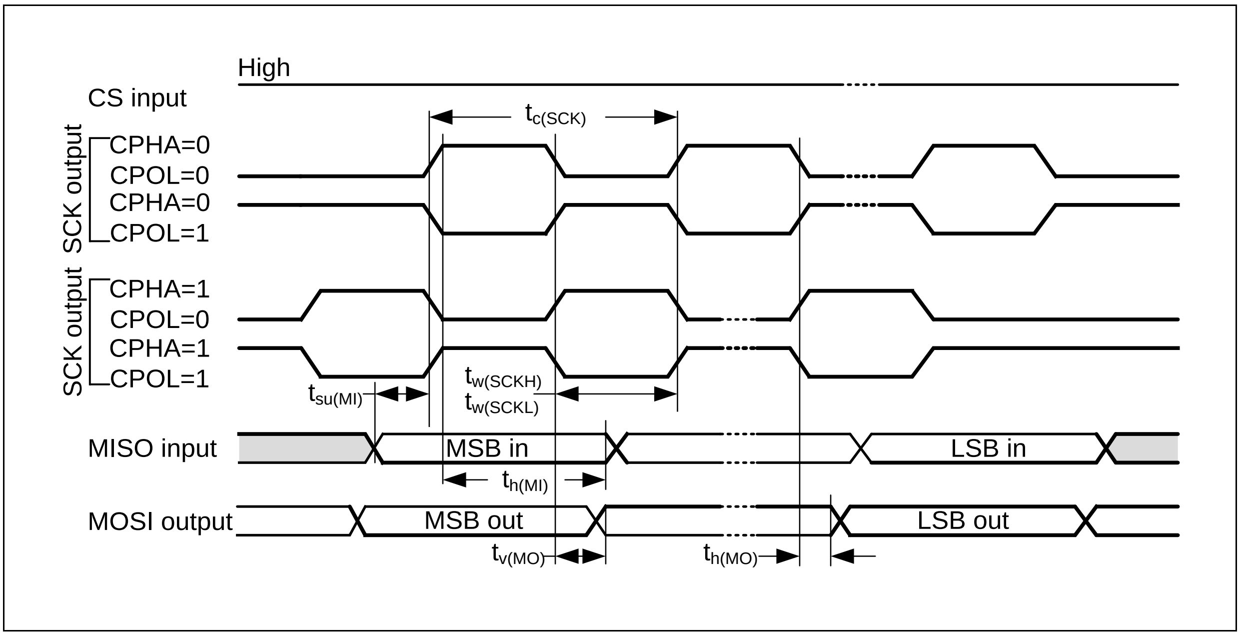


Figure 20. SPI timing diagram - master mode



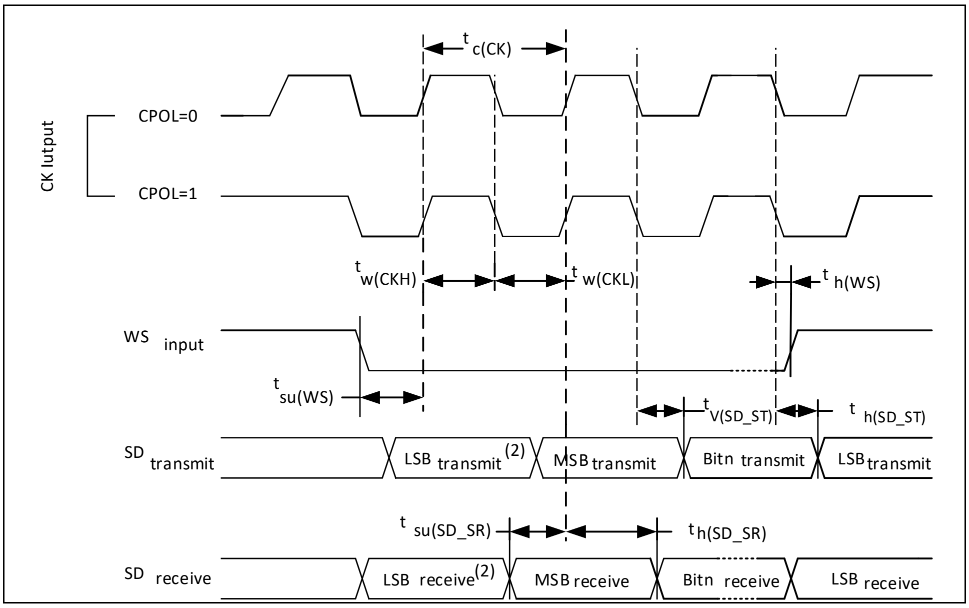
5.3.15 I²S characteristics

Table 39. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	0	4	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	4	
$t_{su(WS)}$(1)	WS setup time	Slave mode	9	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

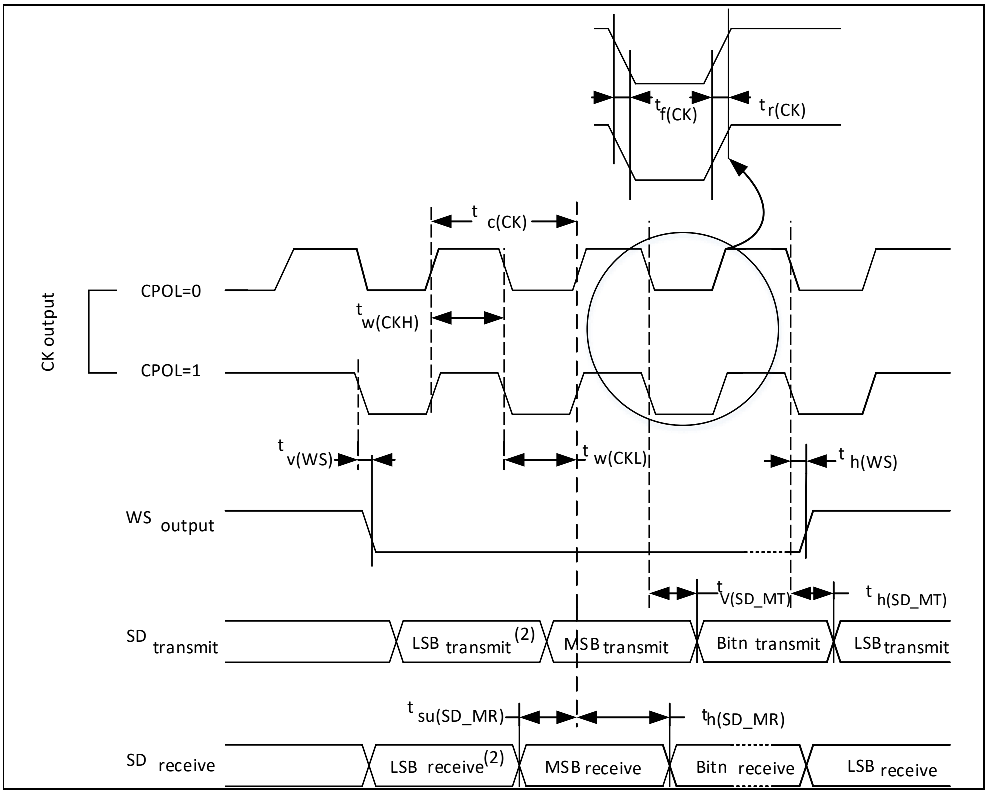
(1) Guaranteed by design, not tested in production.
(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 21. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 22. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

5.3.16 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not "true" open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz). Fore more information, please contact your local or nearest ARTERY sales team.

5.3.17 SDIO characteristics

Figure 23. SDIO high-speed mode

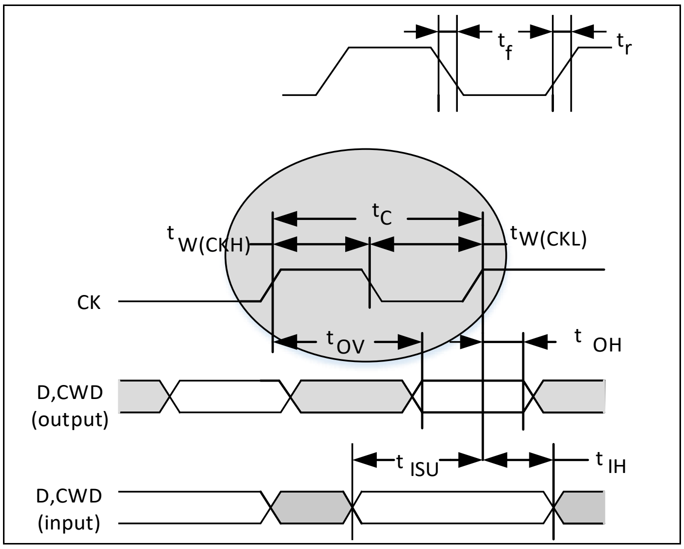


Figure 24. SD default mode

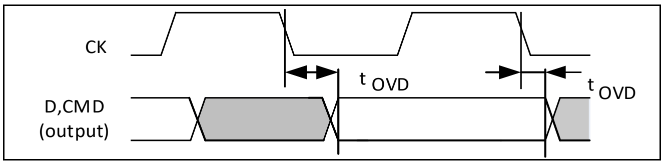


Table 40. SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	48	MHz
$t_{W(CKL)}$	Clock low time	-	32	-	ns
$t_{W(CKH)}$	Clock high time	-	30	-	
t_r	Clock rise time	-	-	4	
t_f	Clock fall time	-	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	-	2	-	ns
t_{IH}	Input hold time	-	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	-	-	6	ns
t_{OH}	Output hold time	-	0	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time	-	-	7	ns
t_{OHD}	Output hold default time	-	0.5	-	

(1) Refer to SDIO_CLKCTRL, the SDIO clock control register to control the CK output.

5.3.18 USBFS characteristics

Table 41. USBFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 42. USBFS DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	OTGFS operating voltage	-	3.0(2)		3.6	V
	V_{DI}(3)	Differential input sensitivity	I (USBFS_D+, USBFS_D-)	0.2		-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8		2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3		2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8		3.6	
R_{PU}		USBFS_D+ internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32F413 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by design, not tested in production.
(4) R_L is the load connected to the USB driver.

Figure 25. USBFS timings: definition of data signal rise and fall time

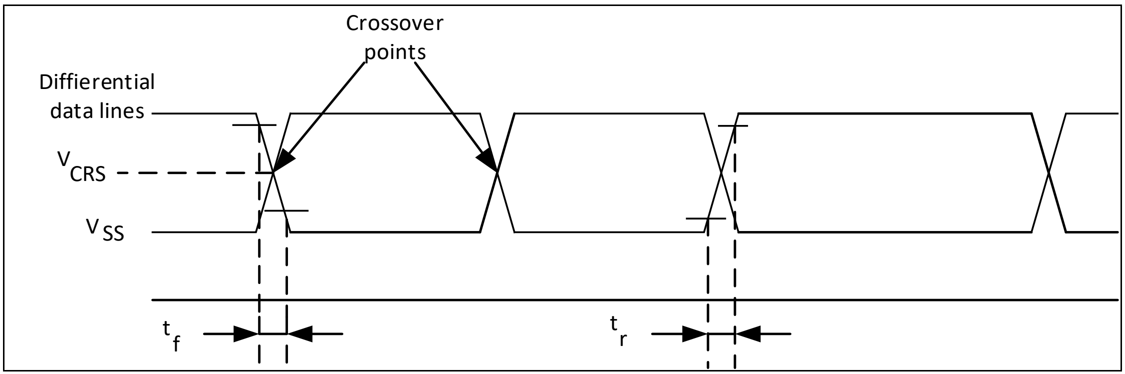


Table 43. USBFS electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time (2)	$C_L \le 50$ pF	4	20	ns
t_f	Fall Time (2)	$C_L \le 50$ pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 11*.

Note: It is recommended to perform a calibration after each power-up.

Table 44. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.6	-	3.6	V
I_{DDA}(1)	Current on the V_{DDA} input pin	-	-	790(2)	900	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(3)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	1/f_{ADC}
V_{AIN}(3)	Conversion voltage range(3)	-	0 (V_{REF-}tied internally to ground))	-	V_{REF+}	V
R_{AIN}(3)	External input impedance	-	See *Table 45* and *Table 46* for details			Ω
C_{ADC}(3)	Internal sample and hold capacitor	-	-	15	-	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 28 MHz	6.14			μs
		-	172			1/f_{ADC}
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(4)	1/f_{ADC}
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	ns
		-	-	-	2(4)	1/f_{ADC}
t_S(3)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	1/f_{ADC}
t_{STAB}(3)	Power-up time	-	42			1/f_{ADC}
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			1/f_{ADC}

(1) V_{REF+} is internally connected to V_{DDA}, and V_{REF-} connected to on the V_{SSA}.
(2) Guaranteed by characterization results, not tested in production.
(3) Guaranteed by design, not tested in production.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 44*.

Table 45 and *Table 46* are used to define the maximum external impedance allowed for an error below 1/4 LSB.

Table 45. R_{AIN} max for f_{ADC} = 14MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.11	0.2
7.5	0.54	1.0
13.5	0.96	2.0
28.5	2.04	4.2
41.5	2.96	6.0
55.5	3.96	8.5
71.5	5.11	11
239.5	17.11	32

(1) Guaranteed by design.

Table 46. R_{AIN} max for f_{ADC} = 28 MHz(1)

T_S (Cycle)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	0.4
13.5	0.48	0.9
28.5	1.02	2.1
41.5	1.48	3.0
55.5	1.98	4.0
71.5	2.55	5.0
239.5	8.55	19

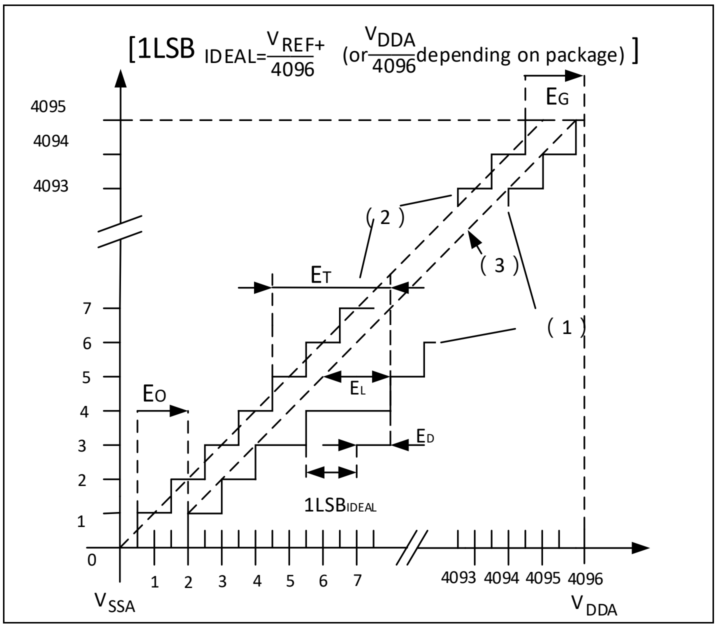
(1) Guaranteed by design.

Table 47. ADC accuracy (1)(2)

Symbol	Parameter	Test Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C V_{REF+} = V_{DDA}	±2	±4	LSB
EO	Offset error		±1	±2	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±0.5	±1	
EL	Integral linearity error		±0.6	±1	
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.6 to 3.6 V T_A = -40 ~ 105 °C	±2	±4	LSB
EO	Offset error		±1	±2.5	
EG	Gain error		±1.5	±3.5	
ED	Differential linearity error		±0.5	±1	
EL	Integral linearity error		±0.6	±1.2	

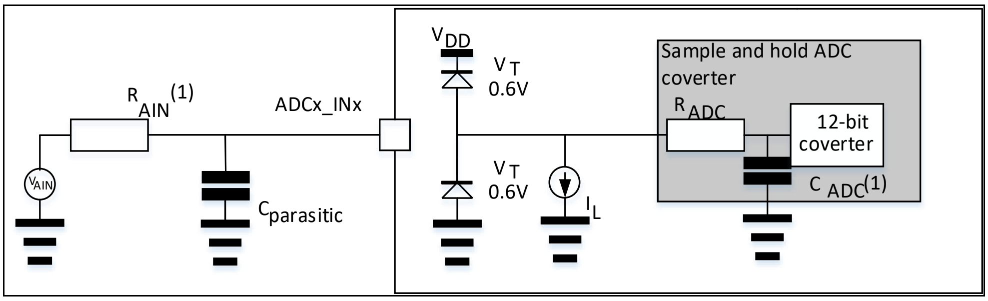
(1) ADC DC accuracy values are measured after internal calibration.
(2) Obtained by characterization results, not tested in production.

Figure 26. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 27. Typical connection diagram using the ADC

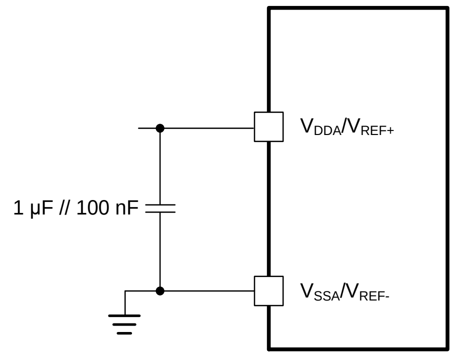


(1) Refer to *Table 44* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 28*. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 28. Power supply and reference decoupling



5.3.20 Internal reference voltage (V_{INTRV}) characteristics

Table 48. Internal reference voltage characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	120	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

5.3.21 Temperature sensor (V_{TS}) characteristics

Table 49. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±2	±5	°C
Avg_Slope(1(2))	Average slope	-4.13	-4.20	-4.35	mV/°C
V_{25}(1)(2)	Voltage at 25 °C	1.18	1.28	1.38	V
t_{START}(3)	Startup time	-	-	100	µs
T_{S_temp}(3)(4)	ADC sampling time when reading the temperature	5.1	-	-	µs

(1) Obtained by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

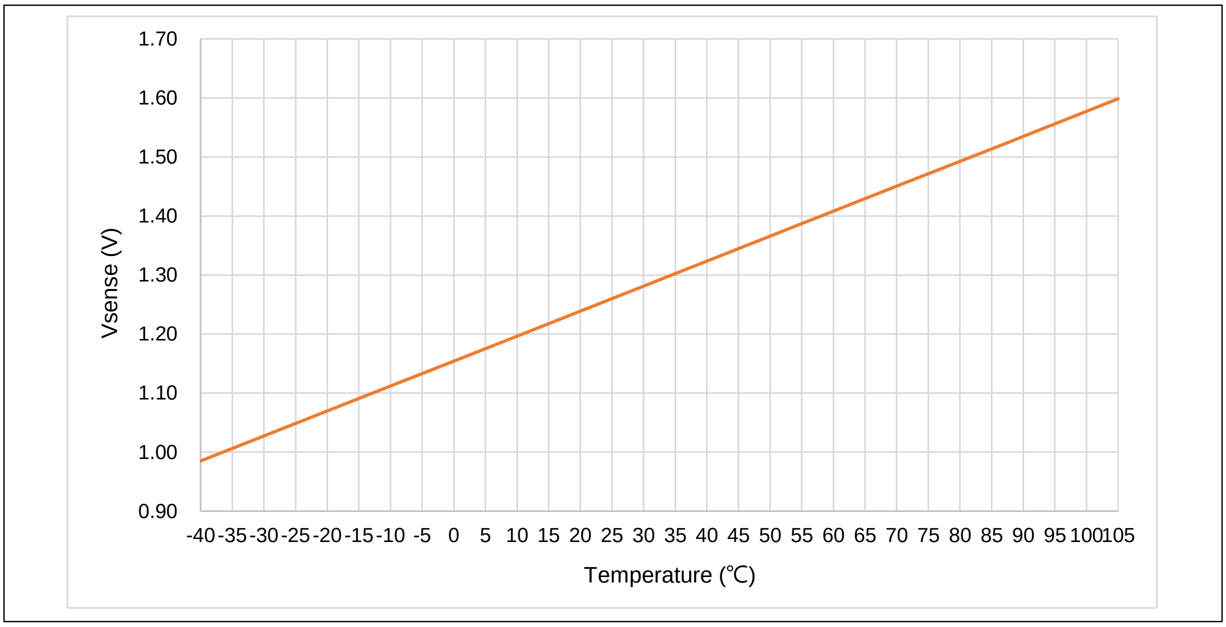
Temperature (in °C) = {(V_{25} - V_{TS}) / Avg_Slope} + 25.

Where,

V_{25} = V_{TS} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{TS} (given in mV/° C).

Figure 29. V_{TS} vs. temperature



6 Package information

6.1 LQFP64 package information

Figure 30. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline

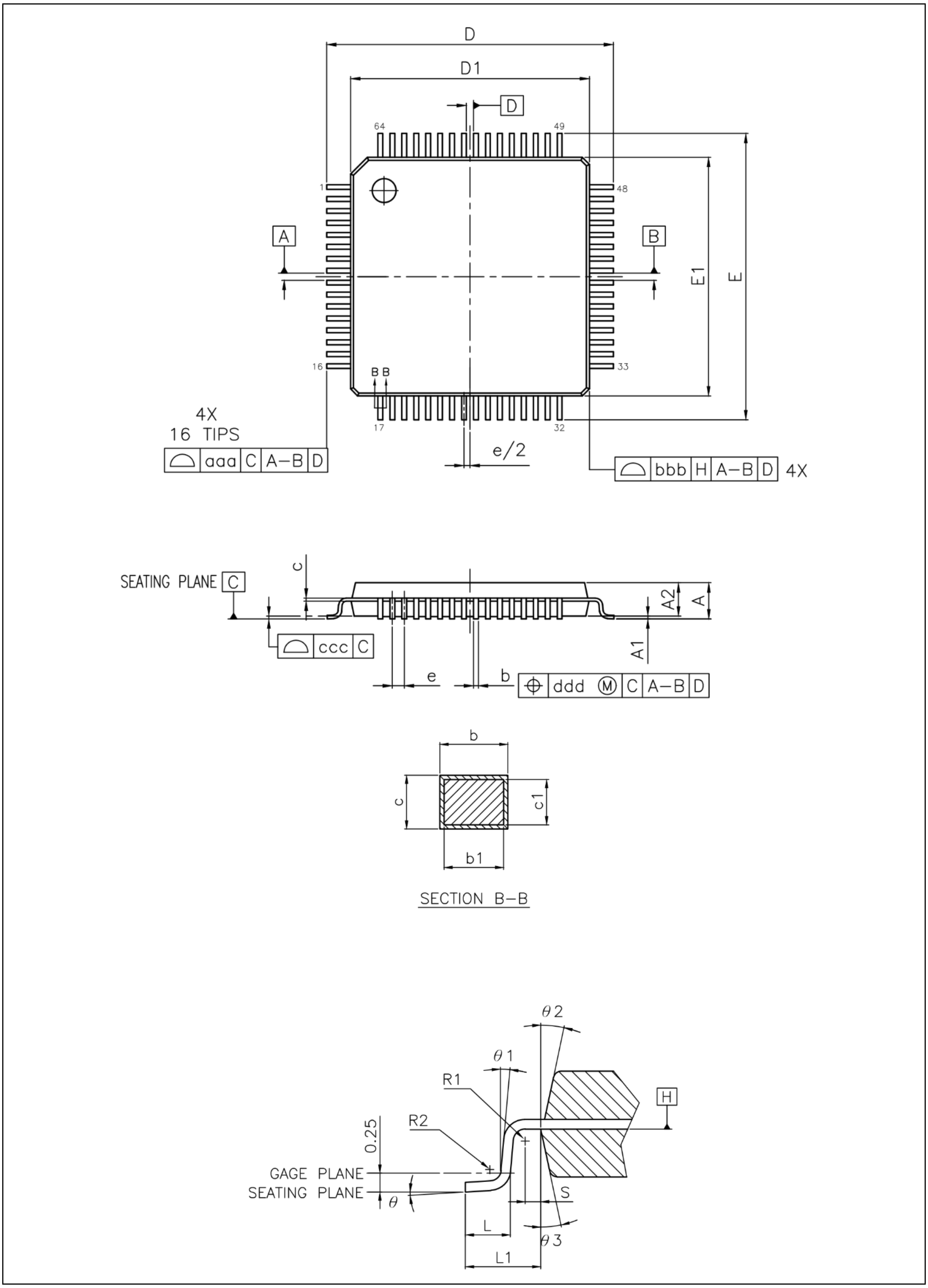


Table 50. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC.		
Θ	3.5° REF.		
L	0.45	0.60	0.75
L1	1.00 REF.		
ccc	0.08		

6.2 LQFP48 package information

Figure 31. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline

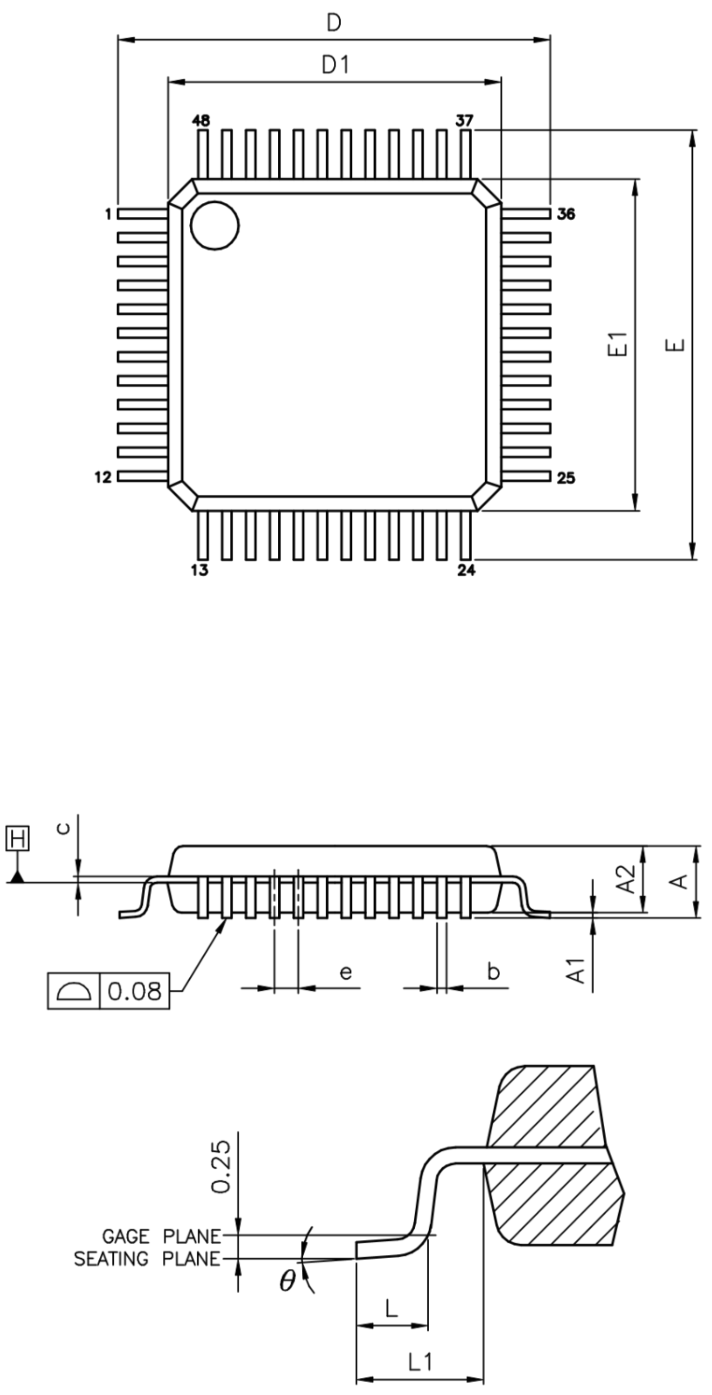


Table 51. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

6.3 QFN48 package information

Figure 32. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline

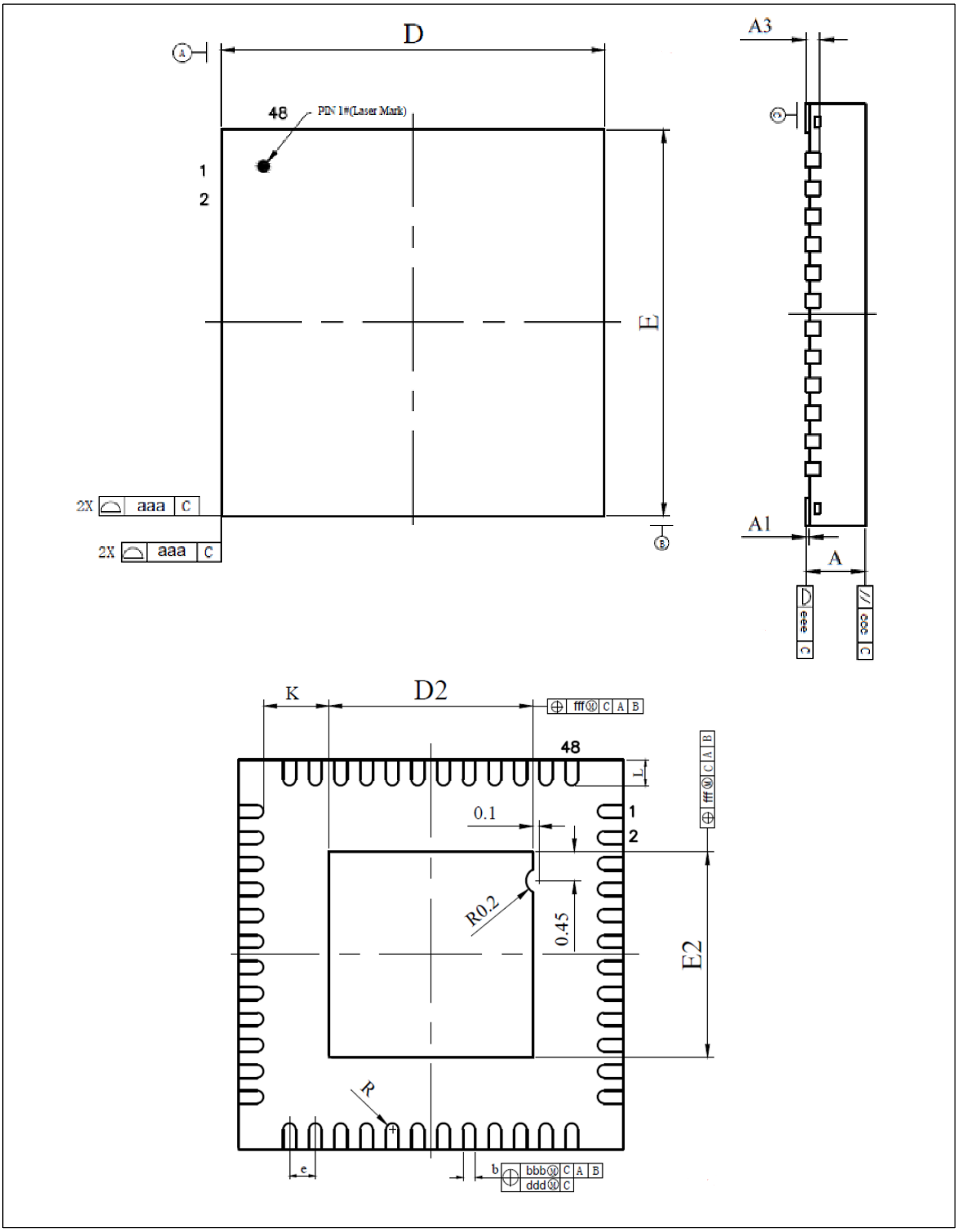


Table 52. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	3.07	3.17	3.27
E	5.90	6.00	6.10
E2	3.07	3.17	3.27
e	0.40 BSC.		
K	0.20	-	-
L	0.35	0.40	0.45

6.4 QFN32 package information

Figure 33. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline

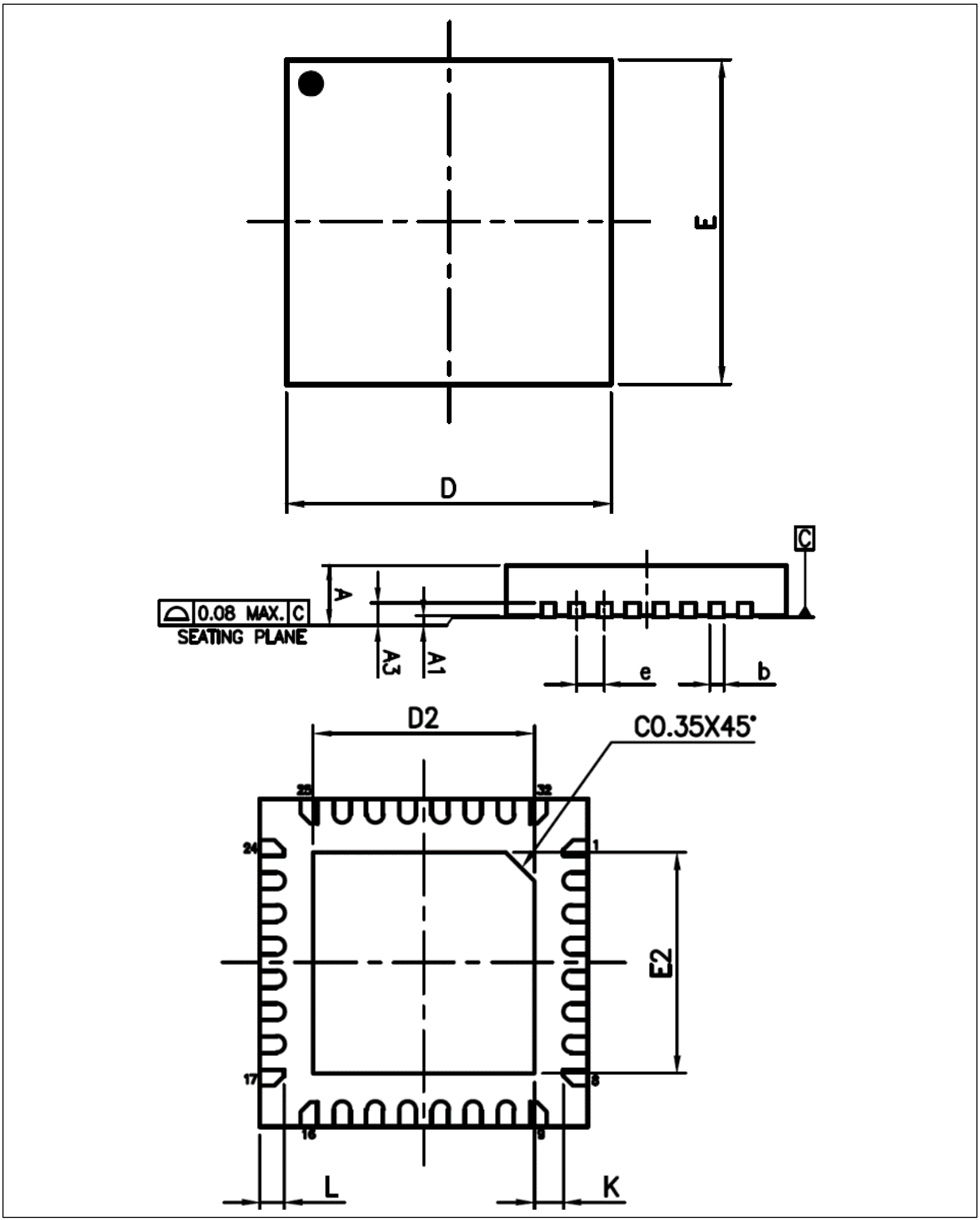


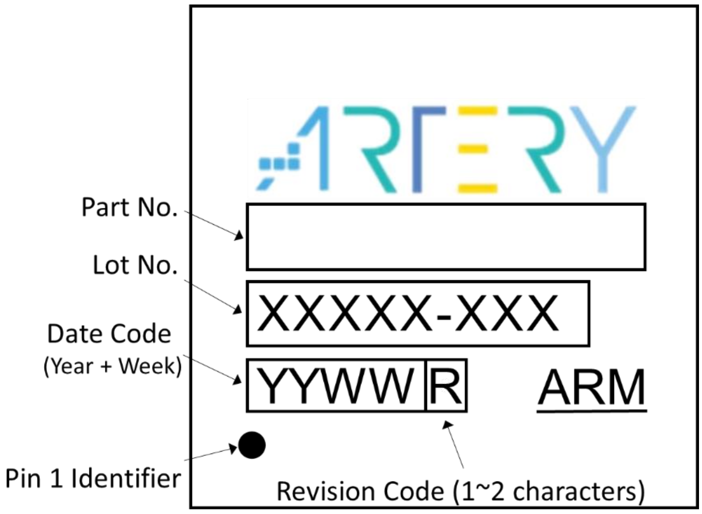
Table 53. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	0.40 BSC.		
K	0.20	-	-
L	0.25	0.30	0.35

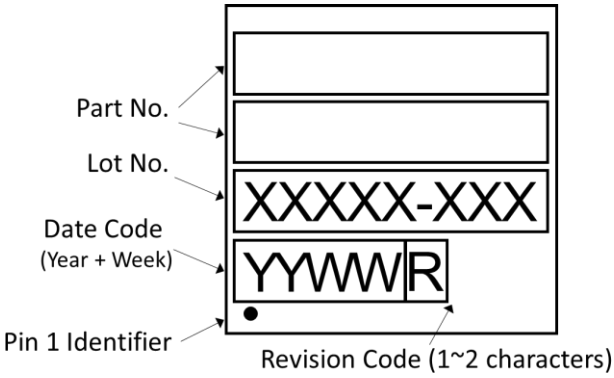
6.5 Device marking

Figure 34. Marking example

LQFP64, LQFP48 and QFN48



QFN32



(1) Not In Scale.

6.6 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material of 1.6mm thickness. They are guaranteed by design, not tested in production.

Table 54. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 – 10 x 10 mm/0.5 mm pitch	69.2	°C/W
	Thermal resistance junction-ambient LQFP48 – 7 x 7 mm/0.5 mm pitch	63.8	
	Thermal resistance junction-ambient QFN48 – 6 x 6 mm/0.4 mm pitch	50.8	
	Thermal resistance junction-ambient QFN32 – 4 x 4 mm/0.4 mm pitch	59.9	

7 Part numbering

Table 55. AT32F413 ordering information scheme

Example: AT32 F 4 1 3 K C U 7 -4

Product family

AT32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4

Product series

1 = Valued line

Product application

3 = CAN + USB series

Pin count

R = 64 pins

C = 48 pins

K = 32 pins

Internal Flash memory size

C = 256 KBytes of the internal Flash memory

B = 128 KBytes of the internal Flash memory

8 = 64 KBytes of the internal Flash memory

Package

T = LQFP

U = QFN

Temperature range

7 = -40 °C to +105 °C

Package details

-4 = QFN32 - 4 x 4 mm

Blank = other packages

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Artery sales office.

8 Document revision history

Table 56. Document revision history

Date	Version	Change
2018.11.23	1.00	Initial release.
2019.2.25	1.01	1. Corrected the maximum PLL input clock as 16 MHz 3. Corrected the number of USART/UART in *Table 2* 4. Modified the maximum HBM value as 5000 V in *Table 9*
2019.3.25	1.02	1. Added AT32F413CBU7
2019.4.16	1.03	1. Modified AT32F413KxU7 as AT32F413KxU7-4
2019.8.6	1.04	1. Added CLKOUT prescaler in *Table 2* 2. Added the maximum rising rate of V_{DD} as note (1) of *Table 12*
2020.3.10	1.05	1. Corrected DMA2 as 7 channels 2. Added USBFS1_SOF function on PA8
2022.2.10	2.00	1. Updated document architecture. 2. Added note (9) in *Table 5* 3. Corrected SPI frequency in *Table 38* 4. Modified LQFP48 package data 5. Modified QFN48 package data and *Figure 32*
2022.6.6	2.01	1. Added max value and notes (T_A = 25 °C) in *Table 21* and *Table 22* 2. Added min and max values in D, D1, E and E1 lines of all package mechanic data tables.
2023.10.17	2.02	1. Updated *Table 15, Table 38 and Table 39* 2. Added footnote(3) to *Table 33* 3. Added a paragraph of description to *section 2.14.6 Controller area network (CAN)* 4. Updated *Figure 28* 5. Updated “IMPORTANT NOTICE” at the end of this file.