Features

- **100% Compatible to AT45D021**
- **Single 4.5V - 5.5V Supply**
- **Serial Interface Architecture**
- **Page Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **1024 Pages (264 Bytes/Page) Main Memory**
- **Optional Page and Block Erase Operations**
- **Two 264-byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory**
- **Continuous Read Capability through Entire Array**
- **Internal Program and Control Timer**
- **Low Power Dissipation**
  - **15 mA Active Read Current Typical**
  - **10 µA CMOS Standby Current Typical**
- **15 MHz Max Clock Frequency**
- **Hardware Data Protection Feature**
- **Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Commercial and Industrial Temperature Ranges**

2-megabit 5-volt Only Serial DataFlash®

AT45D021A

Recommend using AT45DB021B for new designs.

Description

The AT45D021A is a 5-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 2,162,688 bits of memory are organized as 1024 pages of 264 bytes each. In addition to the main memory, the AT45D021A also contains two SRAM data buffers of 264 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash

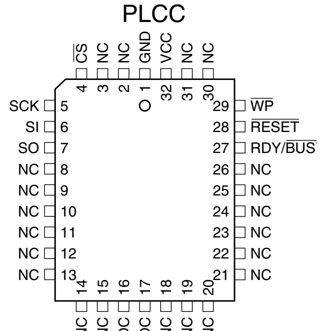
(continued)

Pin Configurations

Pin Name	Function
$\overline{\text{CS}}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{\text{WP}}$	Hardware Page Write Protect Pin
$\overline{\text{RESET}}$	Chip Reset
RDY/$\overline{\text{BUSY}}$	Ready/Busy

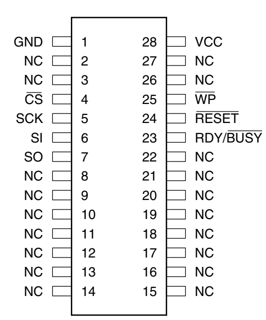
TSOP Top View
Type 1

PLCC



Note: PLCC package pins 16 and 17 are DON'T CONNECT.

SOIC



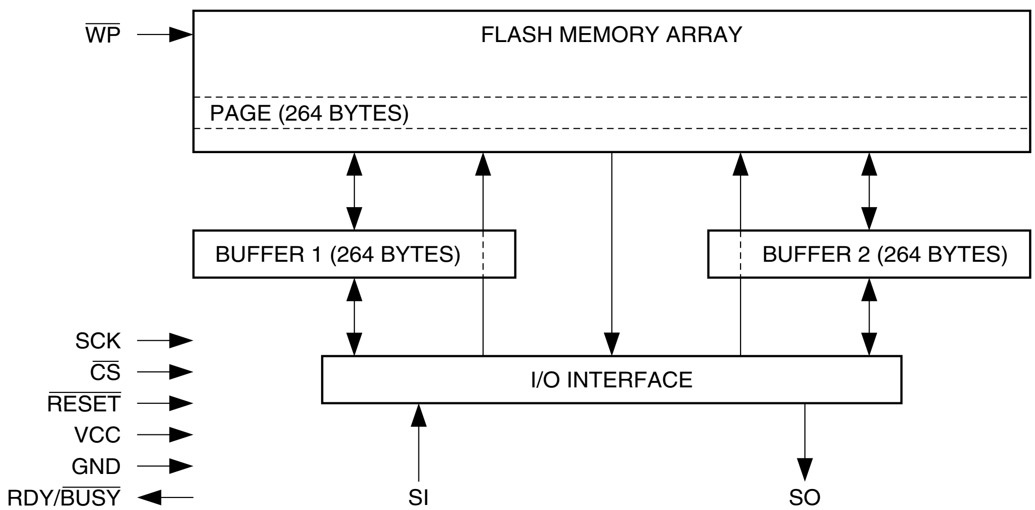
Rev. 1639C–01/01

memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 15 MHz with a typical active read current consumption of 15 mA.

To allow for simple in-system reprogrammability, the AT45D021A does not require high input voltages for programming. The device operates from a single power supply, 4.5V to 5.5V, for both the program and read operations. The AT45D021A is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

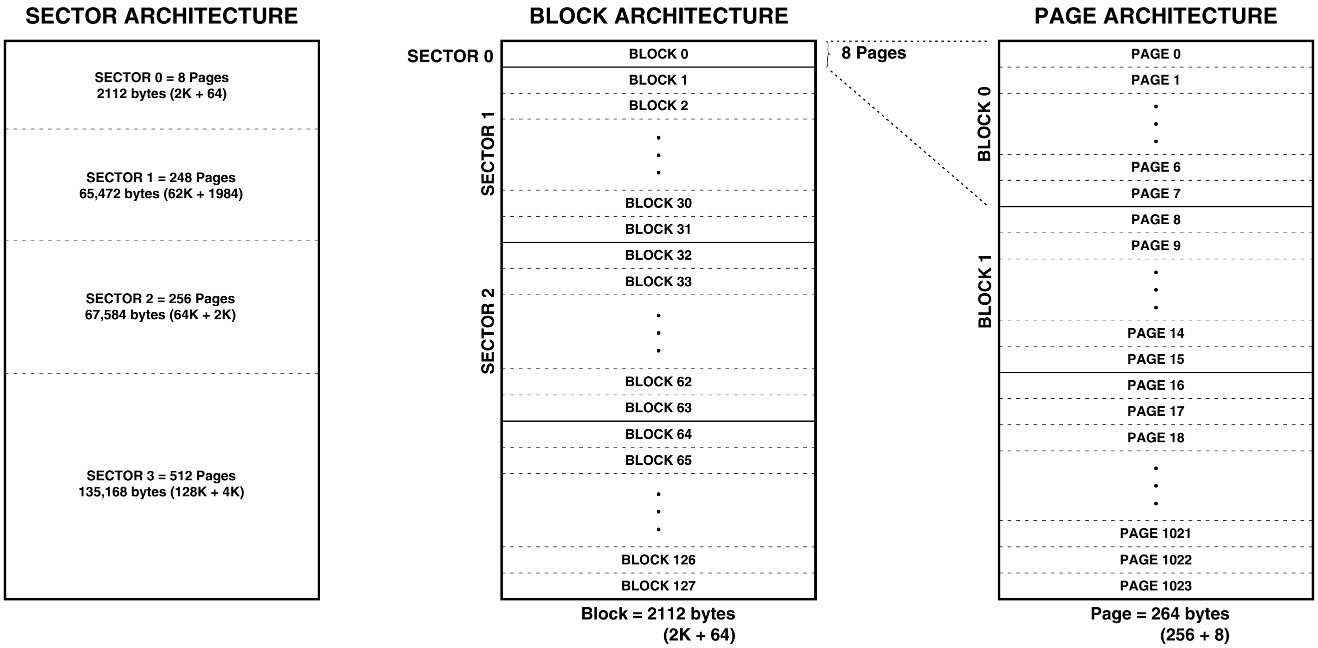
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45D021A is divided into three levels of granularity comprised of sectors, blocks and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page-by-page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 through 4, starting on page 8. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Buffer addressing is referenced in the datasheet using the terminology BFA8-BFA0 to denote the nine address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology PA9-PA0 and BA8-BA0 where PA9-PA0 denotes the 10 address bits required to designate a page address and BA8-BA0 denotes the nine address bits required to designate a byte address within the page.

Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers. The DataFlash supports two categories of read modes in relation to the SCK signal. The differences between the modes are in respect to the inactive state of the SCK signal as well as which clock cycle data will begin to be output. The two categories, which are comprised of four modes total, are defined as Inactive Clock Polarity Low or Inactive Clock Polarity High and SPI Mode 0 or SPI Mode 3. A separate opcode (refer to Table 1 on page 8 for a complete list) is used to select which category will be used for reading. Please refer to the "Detailed Bit-level Read Timing" diagrams in this datasheet for details on the clock cycle sequences for each mode.

CONTINUOUS ARRAY READ: By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read operation without the need of additional address sequences. To perform a continuous read, an opcode of 68H or E8H must be clocked into the device followed by 24 address bits and 32 don't care bits. The first five bits of the 24-bit address sequence are reserved for upward and downward compatibility to larger and smaller density devices (see Notes under "Command Sequence for Read/Write Operations" diagram). The next 10 address bits (PA9-PA0) specify which page of the main memory array to read, and the last nine bits (BA8-BA0) of the 24-bit address sequence specify the starting byte address within the page. The 32 don't care bits that follow the 24 address bits are needed to initialize the read operation. Following the 32 don't care bits, additional clock pulses on the SCK pin will result in serial data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a page in main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin. The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

BURST ARRAY READ: The Burst Array Read operation functions almost identically to the Continuous Array Read operation but allows much higher read throughputs by utilizing faster clock frequencies. The Burst Array Read command allows the device to burst an entire page of data out at the maximum SCK frequency defined by the f_{BAR} parameter. Differences between the Burst Array Read and Continuous Array Read operations are limited to timing only. The opcodes utilized and the opcode and addressing sequence for the Burst Array Read are identical to the Continuous Array Read. The opcode of 68H or E8H must be clocked into the device followed by the 24 address bits and 32 don't care bits. Following the 32 don't care bits, additional clock pulses on the SCK pin will result in serial data being output on the SO (serial output) pin.

As with the Continuous Array Read, the $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. During a Burst Array Read, when the end of a page in main memory is reached (the last bit of the page has been clocked out), the system must delay the next SCK pulse by a minimum time of t_{BRBD}. This delay is necessary to allow the device enough time to cross over the burst read boundary, which is defined as the end of one page in memory to the beginning of the next page. When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. The transition from the last bit of the array back to the beginning of the array is also considered a burst read boundary. Therefore, the system must delay the SCK pulse that will be used to read the first bit of the memory array by a minimum time of t_{BRBD}.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin. The maximum SCK frequency allowable for the Burst Array Read is defined by the f_{BAR} specification. The Burst Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

MAIN MEMORY PAGE READ: A Main Memory Page Read allows the user to read data directly from any one of the 1024 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, an opcode of 52H or D2H must be clocked into the device followed by 24 address bits and 32 don't care bits. The first five bits of the 24-bit address sequence are reserved bits, the next 10 address bits (PA9-PA0) specify the page address, and the next nine address bits (BA8-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a page in main memory is reached during a Main Memory Page Read, the device will continue reading at the beginning of the same page. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H or D4H is used to read data from buffer 1, and an opcode of 56H or D6H is used to read data from buffer 2. To perform a Buffer Read, the eight bits of the opcode must be followed by 15 don't care bits, nine address bits, and eight don't care bits. Since the buffer size is 264-bytes, nine address bits (BFA8-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

STATUS REGISTER READ: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H or D7H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{\text{BUSY}}$	COMP	0	1	0	X	X	X

Ready/Busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-in Erase, Buffer to Main Memory Page Program without Built-in Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45D021A, the three bits are 0, 1, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Program and Erase Commands

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, must be followed by 15 don't care bits and nine address bits (BFA8-BFA0). The nine address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{\text{CS}}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. To start the operation, an 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, must be followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. To start the operation, an 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, must be followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in the main memory to be written, and nine additional don't care bits. When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-in Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by five reserved bits, 10 address bits (PA9-PA0), and nine don't care bits. The nine address bits are used to specify which page of the memory array is to be erased. When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-in Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by five reserved bits, seven address bits (PA9-PA3), and 12 don't care bits. The seven address bits are used to specify which block of eight pages is to be erased. When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	0	0	X	X	X	124
1	1	1	1	1	0	1	X	X	X	125
1	1	1	1	1	1	0	X	X	X	126
1	1	1	1	1	1	1	X	X	X	127

MAIN MEMORY PAGE PROGRAM THROUGH BUFFER: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-in Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. To initiate the operation, an 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, must be followed by the five reserved bits and 20 address bits. The 10 most significant address bits (PA9-PA0) select the page in the main memory where data is to be written, and the next nine address bits (BFA8-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self-timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

Additional Commands

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. To start the operation, an 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, must be followed by the five reserved bits, 10 address bits (PA9-PA0) which specify the page in main memory that is to be transferred, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. To initiate the operation, an 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, must be followed by 24 address bits consisting of the five reserved bits, 10 address bits (PA9-PA0) which specify the page in the main memory that is to be compared to the buffer, and nine don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low-to-high transition of the $\overline{CS}$ pin, the 264 bytes in the selected main memory page will be compared with the 264 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

AUTO PAGE REWRITE: This mode is needed only if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-in Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. To start the rewrite operation, an 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, must be followed by the five reserved bits, 10 address bits (PA9-PA0) that specify the page in main memory to be rewritten, and nine additional don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page-by-page, then the programming algorithm shown in Figure 1 on page 24 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 on page 25 is recommended.

Operation Mode Summary

The modes described can be separated into two groups – modes which make use of the Flash memory array (Group A) and modes which do not make use of the Flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Main Memory Page to Buffer 1 (or 2) Transfer
3. Main Memory Page to Buffer 1 (or 2) Compare
4. Buffer 1 (or 2) to Main Memory Page Program with Built-in Erase
5. Buffer 1 (or 2) to Main Memory Page Program without Built-in Erase
6. Page Erase
7. Block Erase
8. Main Memory Page Program through Buffer
9. Auto Page Rewrite

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Pin Descriptions

SERIAL INPUT (SI): The SI pin is an input only pin and is used to shift data into the device. The SI pin is used for all data input including opcodes and address sequences.

SERIAL OUTPUT (SO): The SO pin is an output only pin and is used to shift data out from the device.

SERIAL CLOCK (SCK): The SCK pin is an input only pin and is used to control the flow of data to and from the DataFlash. Data is always clocked into the device on the rising edge of SCK and clocked out of the device on the falling edge of SCK.

CHIP SELECT ($\overline{CS}$): The DataFlash is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted on the SI pin, and the SO pin will remain in a high impedance state. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition on the $\overline{CS}$ pin is required to end an operation.

WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through a 1kΩ external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI Mode 3. In addition, the SO pin will be in a high impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Table 1. Read Commands

Command	SCK Mode	Opcode
Continuous Array Read	Inactive Clock Polarity Low or High	68H
	SPI Mode 0 or 3	E8H
Burst Array Read	Inactive Clock Polarity Low or High	68H
	SPI Mode 0 or 3	E8H
Main Memory Page Read	Inactive Clock Polarity Low or High	52H
	SPI Mode 0 or 3	D2H
Buffer 1 Read	Inactive Clock Polarity Low or High	54H
	SPI Mode 0 or 3	D4H
Buffer 2 Read	Inactive Clock Polarity Low or High	56H
	SPI Mode 0 or 3	D6H
Status Register Read	Inactive Clock Polarity Low or High	57H
	SPI Mode 0 or 3	D7H

Table 2. Program and Erase Commands

Command	SCK Mode	Opcode
Buffer 1 Write	Any	84H
Buffer 2 Write	Any	87H
Buffer 1 to Main Memory Page Program with Built-in Erase	Any	83H
Buffer 2 to Main Memory Page Program with Built-in Erase	Any	86H
Buffer 1 to Main Memory Page Program without Built-in Erase	Any	88H
Buffer 2 to Main Memory Page Program without Built-in Erase	Any	89H
Page Erase	Any	81H
Block Erase	Any	50H
Main Memory Page Program through Buffer 1	Any	82H
Main Memory Page Program through Buffer 2	Any	85H

Table 3. Additional Commands

Command	SCK Mode	Opcode
Main Memory Page to Buffer 1 Transfer	Any	53H
Main Memory Page to Buffer 2 Transfer	Any	55H
Main Memory Page to Buffer 1 Compare	Any	60H
Main Memory Page to Buffer 2 Compare	Any	61H
Auto Page Rewrite through Buffer 1	Any	58H
Auto Page Rewrite through Buffer 2	Any	59H

Note: In Tables 2 and 3, an SCK mode designation of “Any” denotes any one of the four modes of operation (Inactive Clock Polarity Low, Inactive Clock Polarity High, SPI Mode 0, or SPI Mode 3).

Table 4. Detailed Bit-level Addressing Sequence

Opcode	Opcode	Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes Required
		Reserved	Reserved	Reserved	Reserved	Reserved	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
50H	0 1 0 1 0 0 0 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	x	x	x	N/A
52H	0 1 0 1 0 0 1 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	4 Bytes
53H	0 1 0 1 0 0 1 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
54H	0 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	1 Byte
55H	0 1 0 1 0 1 0 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
56H	0 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	1 Byte
57H	0 1 0 1 0 1 1 1	N/A								N/A								N/A								N/A
58H	0 1 0 1 1 0 0 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
59H	0 1 0 1 1 0 0 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
60H	0 1 1 0 0 0 0 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
61H	0 1 1 0 0 0 0 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
68H	0 1 1 0 1 0 0 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	4 Bytes
81H	1 0 0 0 0 0 0 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
82H	1 0 0 0 0 0 1 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	N/A
83H	1 0 0 0 0 0 1 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
84H	1 0 0 0 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	N/A
85H	1 0 0 0 0 1 0 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	N/A
86H	1 0 0 0 0 1 1 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
87H	1 0 0 0 0 1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	N/A
88H	1 0 0 0 1 0 0 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
89H	1 0 0 0 1 0 0 1	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	x	x	x	x	x	x	x	x	x	N/A
D2H	1 1 0 1 0 0 1 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	4 Bytes
D4H	1 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	1 Byte
D6H	1 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	1 Byte
D7H	1 1 0 1 0 1 1 1	N/A								N/A								N/A								N/A
E8H	1 1 1 0 1 0 0 0	r	r	r	r	r	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	4 Bytes

Note: r = Reserved Bit
P = Page Address Bit
B = Byte/Buffer Address Bit
x = Don't Care

Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45D021A
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[(1)]		4.5V to 5.5V

Note: 1. After power is applied and V_{CC} is at the minimum specified datasheet value, the system should wait 20 ms before an operational mode is started.

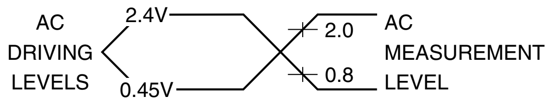
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		10	20	µA
I_{CC1}	Active Current, Read Operation	f = 15 MHz; I_{OUT} = 0 mA; V_{CC} = 5.5V		15	25	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 5.5V		25	50	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2			V

AC Characteristics

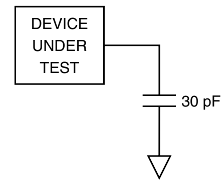
Symbol	Parameter	Min	Max	Units
f_{SCK}	SCK Frequency		15	MHz
f_{CAR}	SCK Frequency for Continuous Array Read		10	MHz
f_{BAR}	SCK Frequency for Burst Array Read		15	MHz
t_{WH}	SCK High Time	30		ns
t_{WL}	SCK Low Time	30		ns
t_{CS}	Minimum $\overline{CS}$ High Time	250		ns
t_{CSS}	$\overline{CS}$ Setup Time	250		ns
t_{CSH}	$\overline{CS}$ Hold Time	250		ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low		200	ns
t_{SU}	Data In Setup Time	10		ns
t_{H}	Data In Hold Time	15		ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		20	ns
t_{V}	Output Valid		25	ns
t_{BRBD}	Burst Read Boundary Delay	1		µs
t_{XFR}	Page to Buffer Transfer/Compare Time		150	µs
t_{EP}	Page Erase and Programming Time		20	ms
t_{P}	Page Programming Time		14	ms
t_{PE}	Page Erase Time		8	ms
t_{BE}	Block Erase Time		12	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10		µs
t_{REC}	$\overline{RESET}$ Recovery Time		1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

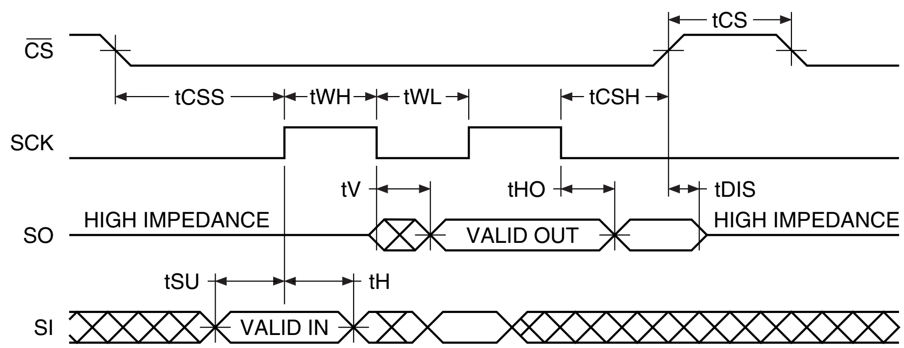


AC Waveforms

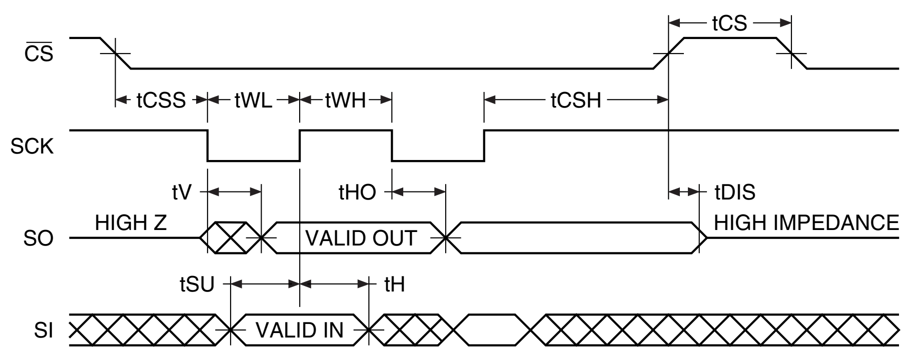
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{\text{CS}}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{\text{CS}}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

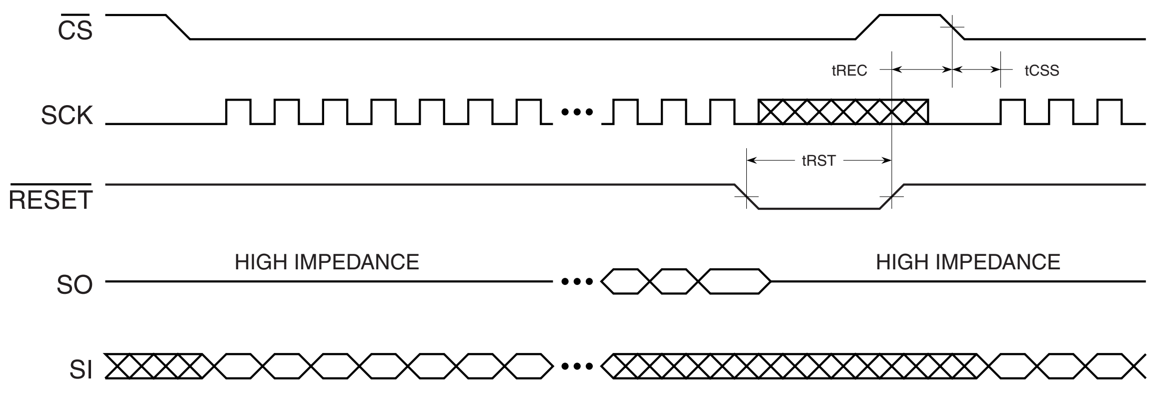
Waveform 1 – Inactive Clock Polarity Low and SPI Mode 0



Waveform 2 – Inactive Clock Polarity High and SPI Mode 3

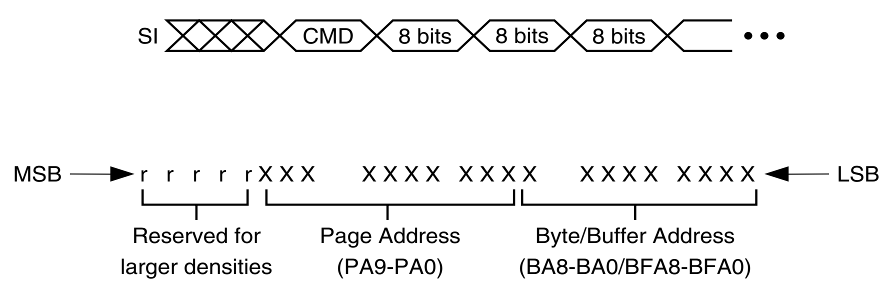


Reset Timing (Inactive Clock Polarity Low Shown)



Note: The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

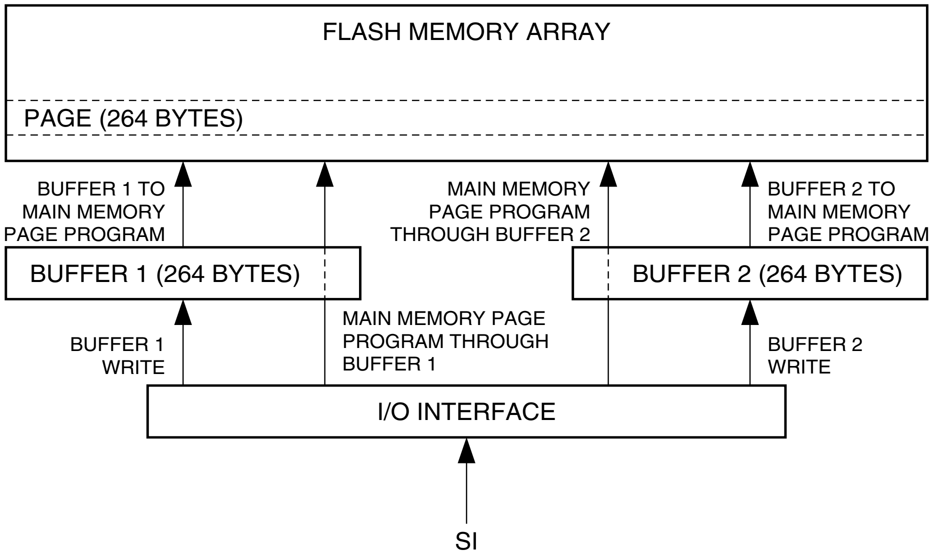
Command Sequence for Read/Write Operations (except Status Register Read)



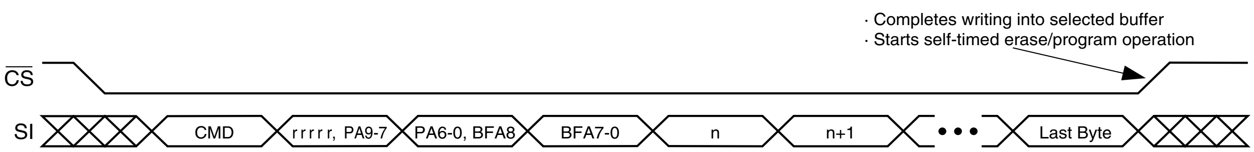
Notes:
1. “r” designates bits reserved for larger densities.
2. It is recommended that “r” be a logical “0” for densities of 2M bits or smaller.
3. For densities larger than 2M bits, the “r” bits become the most significant Page Address bit for the appropriate density.

Write Operations

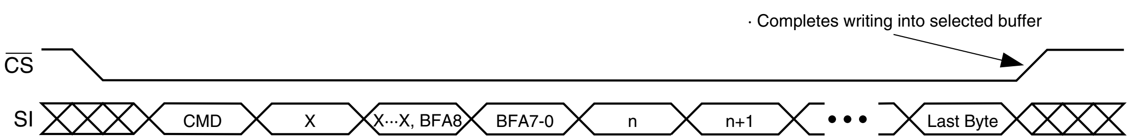
The following block diagram and waveforms illustrate the various write sequences available.



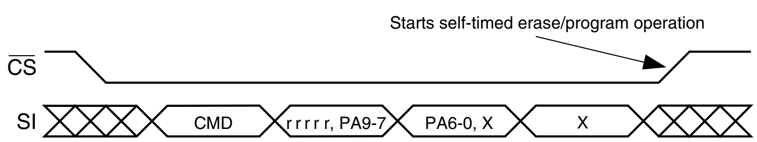
Main Memory Page Program through Buffers

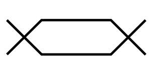


Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)



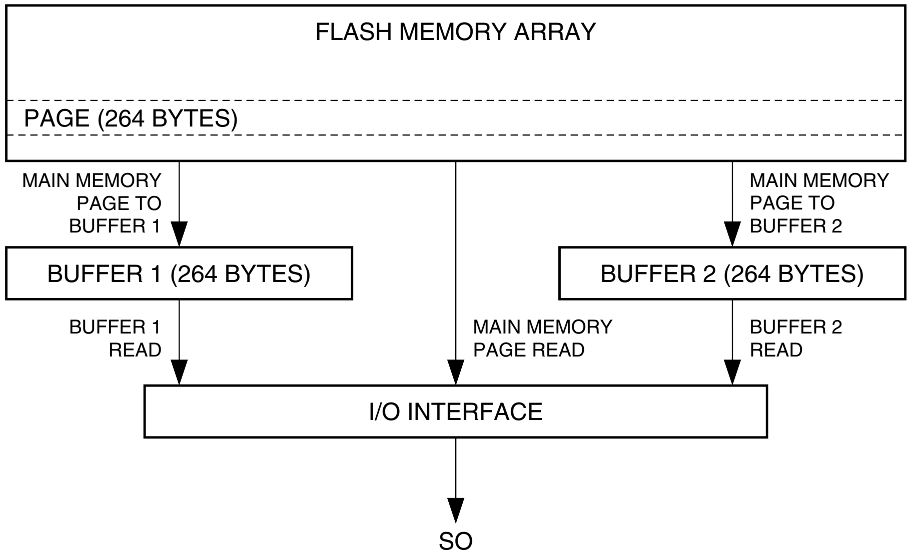
Each transition represents 8 bits and 8 clock cycles 

n = 1st byte read

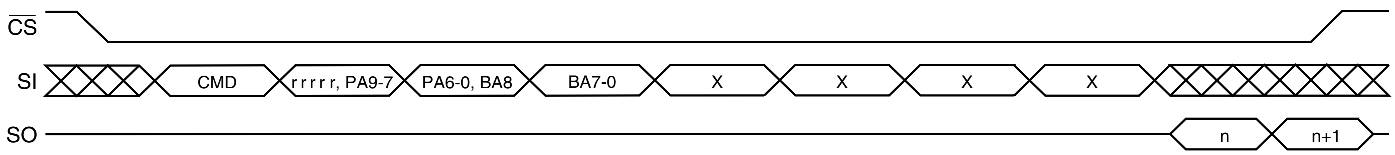
n+1 = 2nd byte read

Read Operations

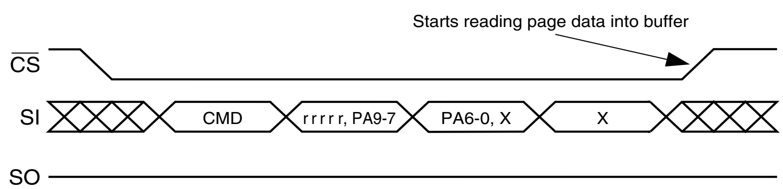
The following block diagram and waveforms illustrate the various read sequences available.



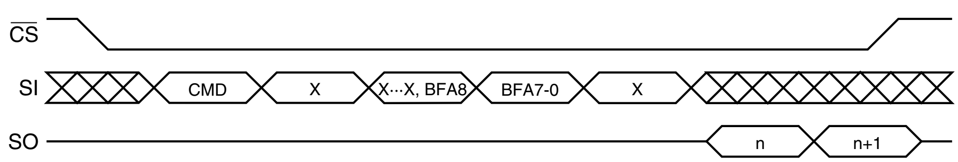
Main Memory Page Read



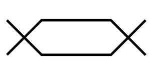
Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read



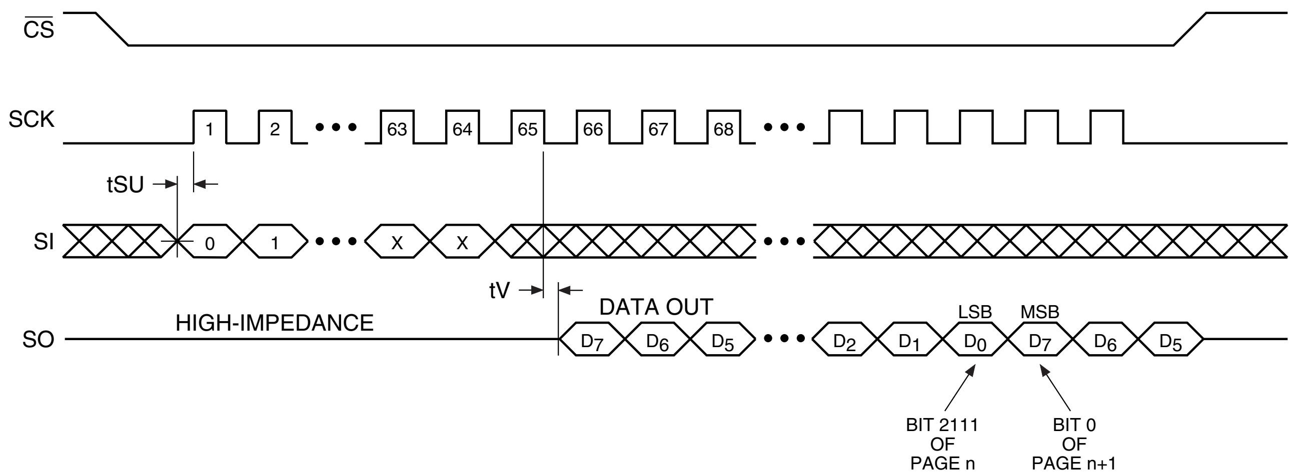
Each transition represents
8 bits and 8 clock cycles



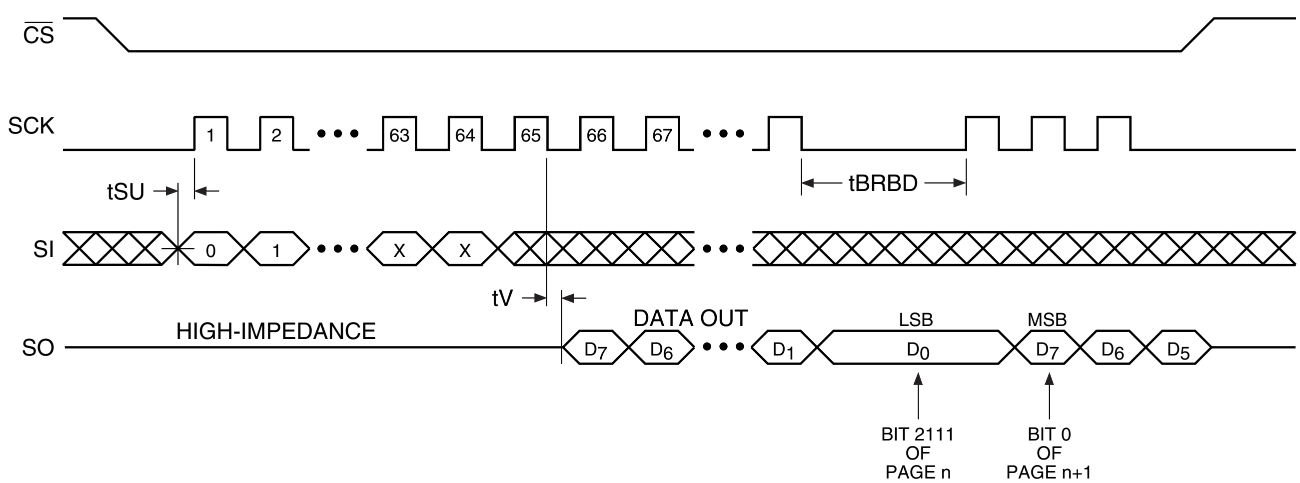
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-level Read Timing – Inactive Clock Polarity Low

Continuous Array Read (Opcode: 68H)

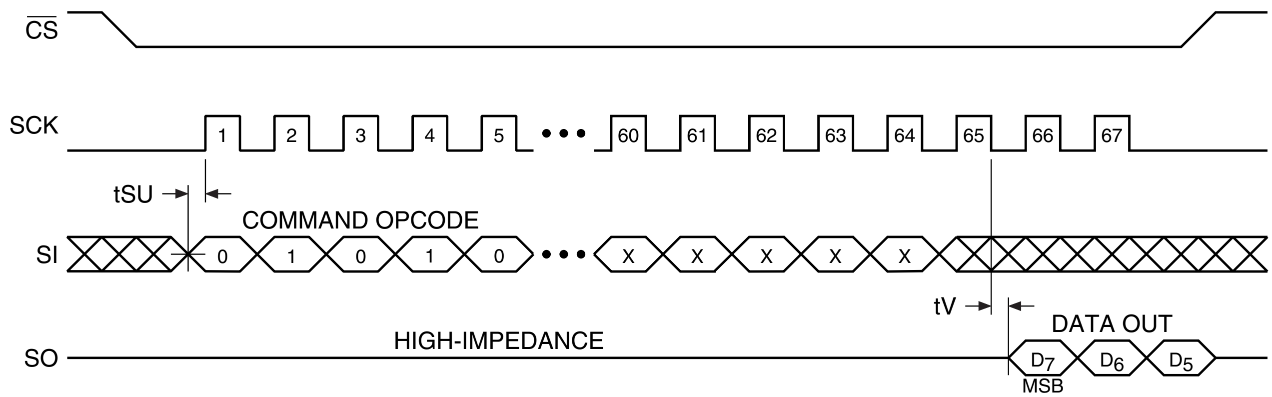


Burst Array Read (Opcode: 68H)

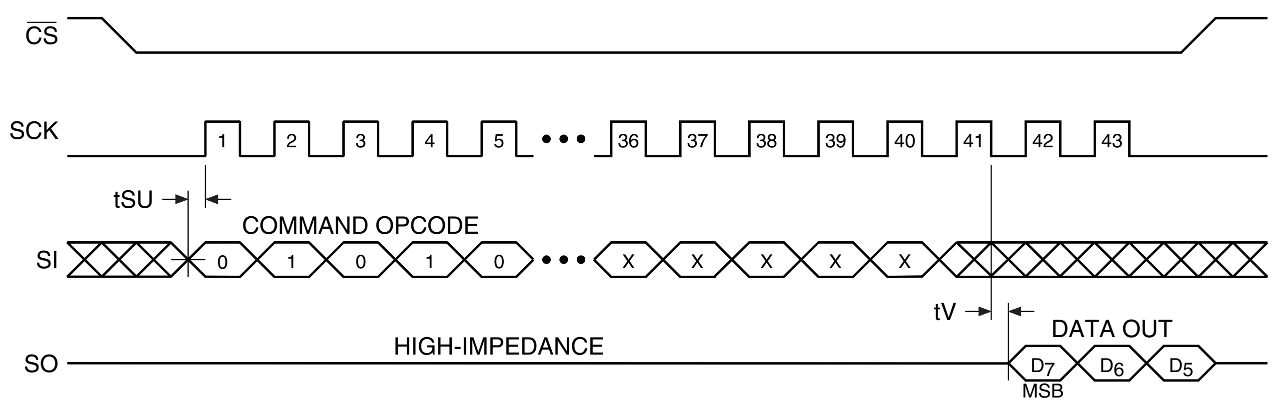


Detailed Bit-level Read Timing – Inactive Clock Polarity Low (Continued)

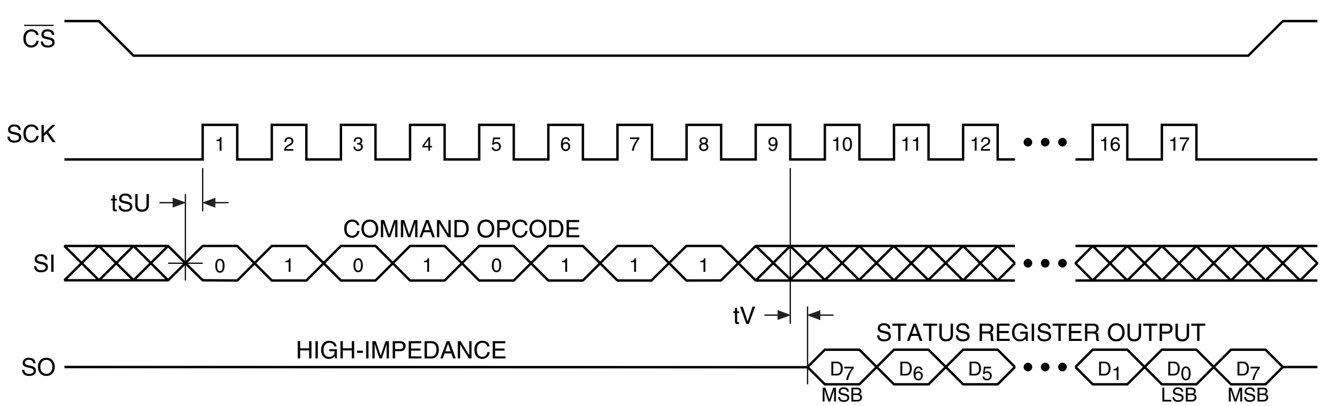
Main Memory Page Read (Opcode: 52H)



Buffer Read (Opcode: 54H or 56H)

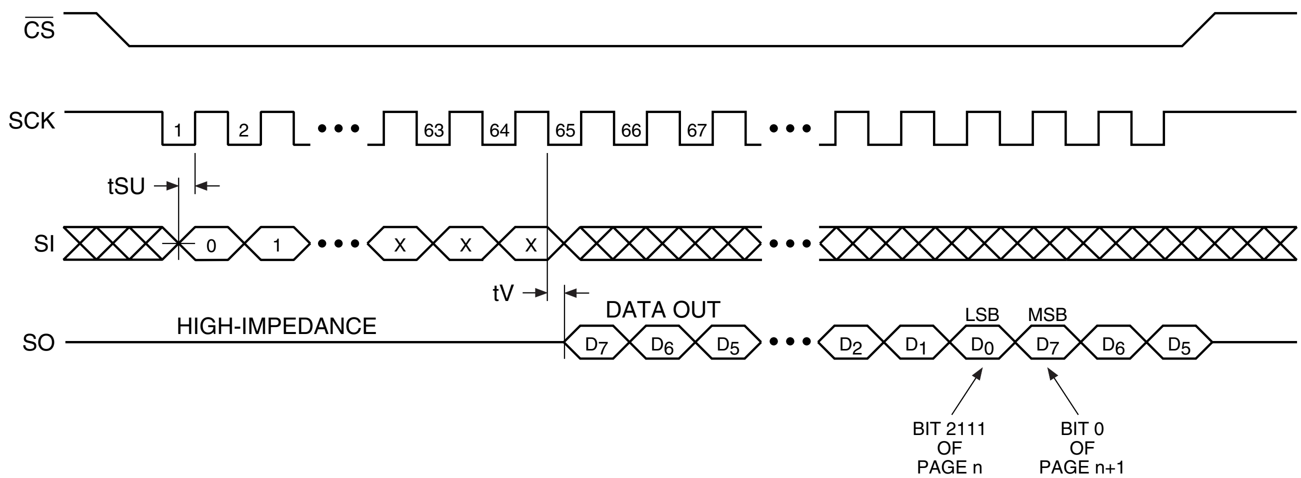


Status Register Read (Opcode: 57H)

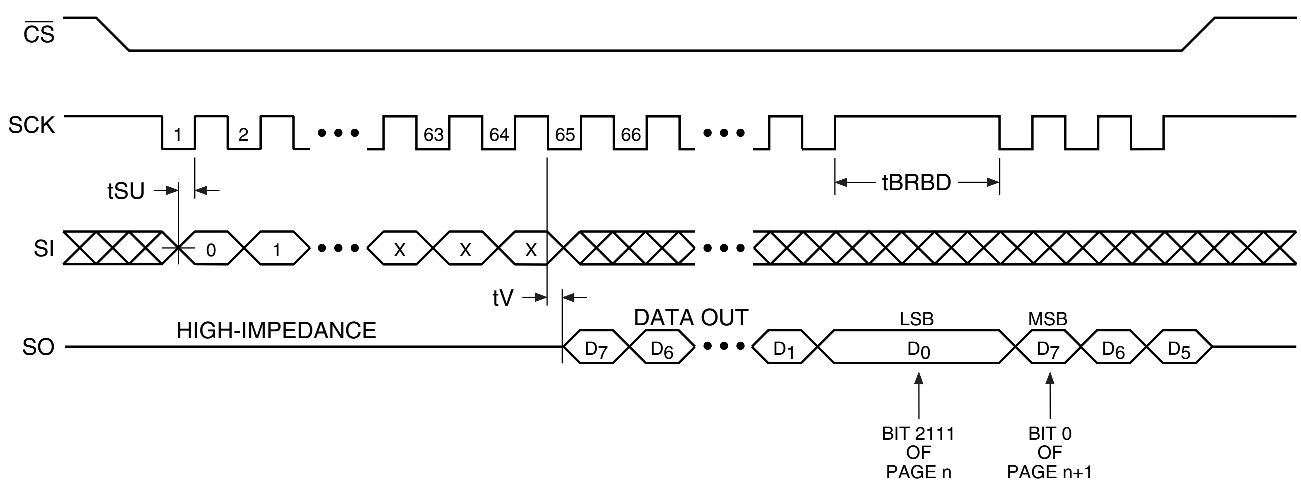


Detailed Bit-level Read Timing – Inactive Clock Polarity High

Continuous Array Read (Opcode: 68H)

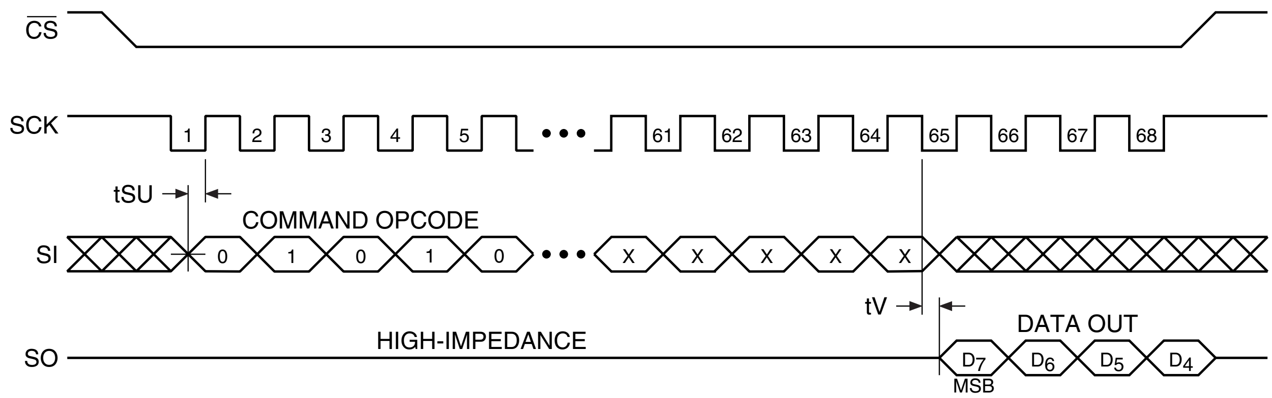


Burst Array Read (Opcode: 68H)

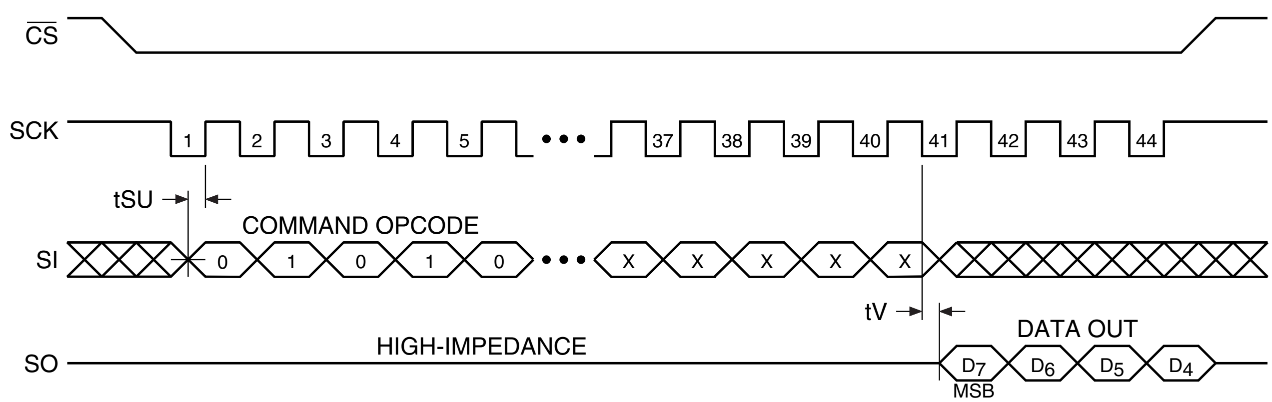


Detailed Bit-level Read Timing – Inactive Clock Polarity High (Continued)

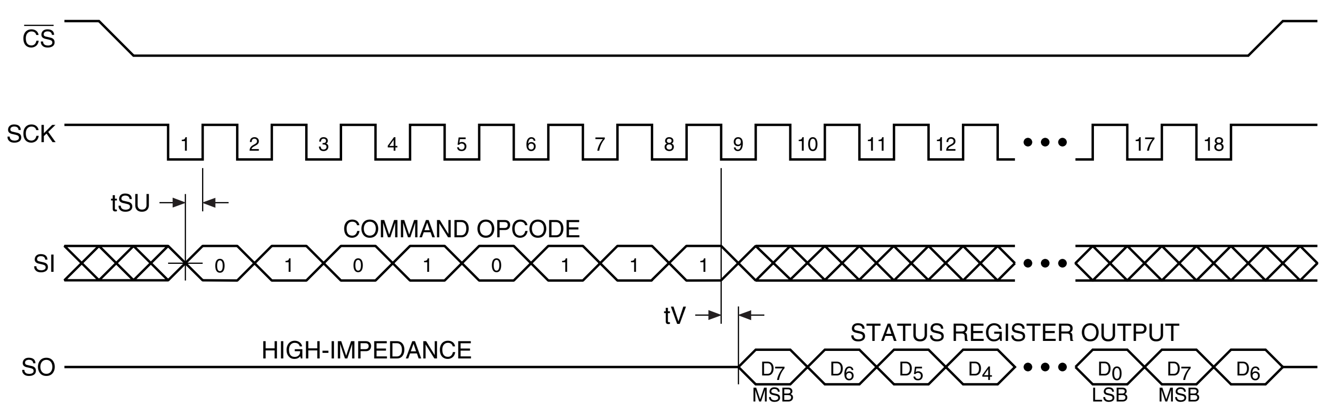
Main Memory Page Read (Opcode: 52H)



Buffer Read (Opcode: 54H or 56H)

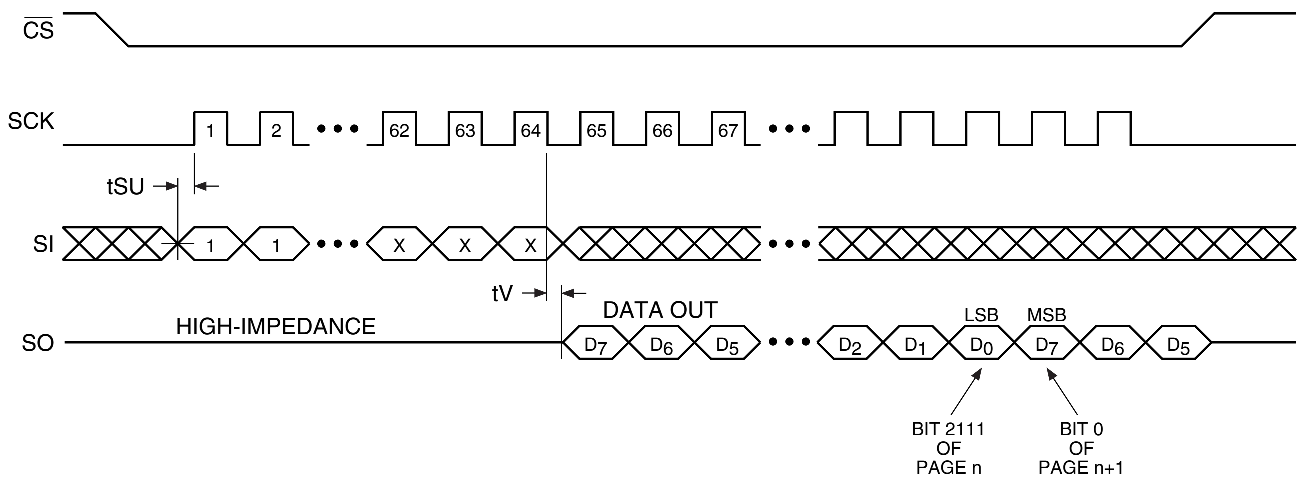


Status Register Read (Opcode: 57H)

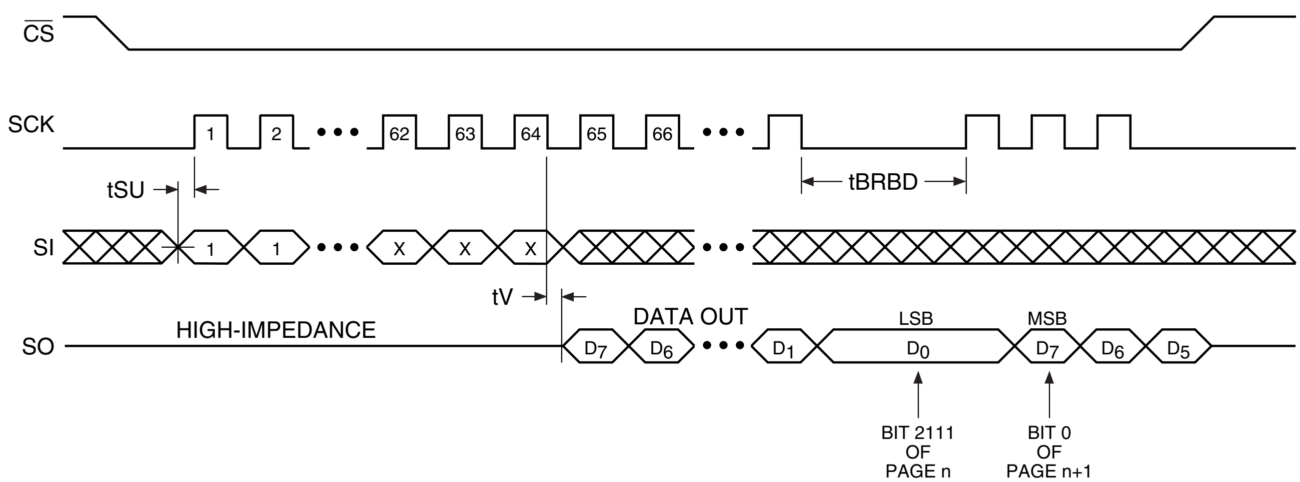


Detailed Bit-level Read Timing – SPI Mode 0

Continuous Array Read (Opcode: E8H)

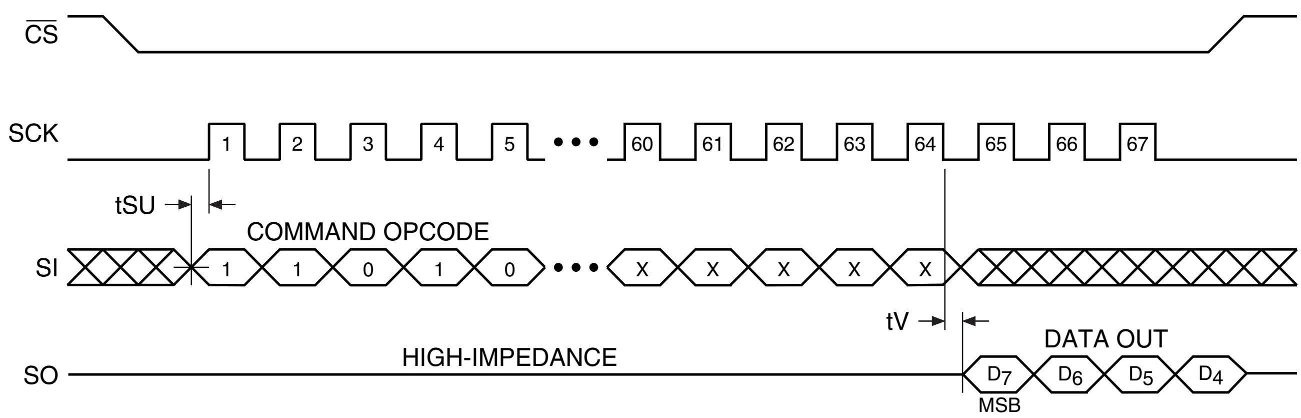


Burst Array Read (Opcode: E8H)

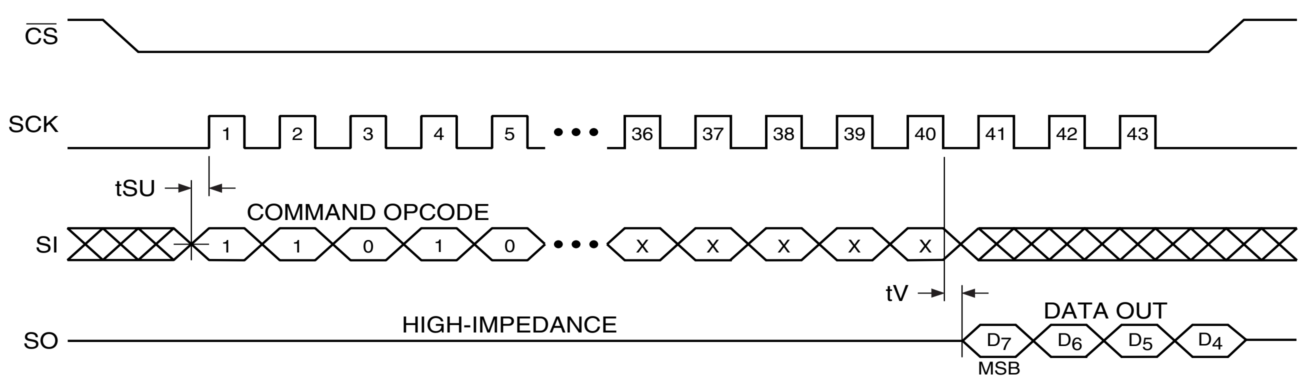


Detailed Bit-level Read Timing – SPI Mode 0 (Continued)

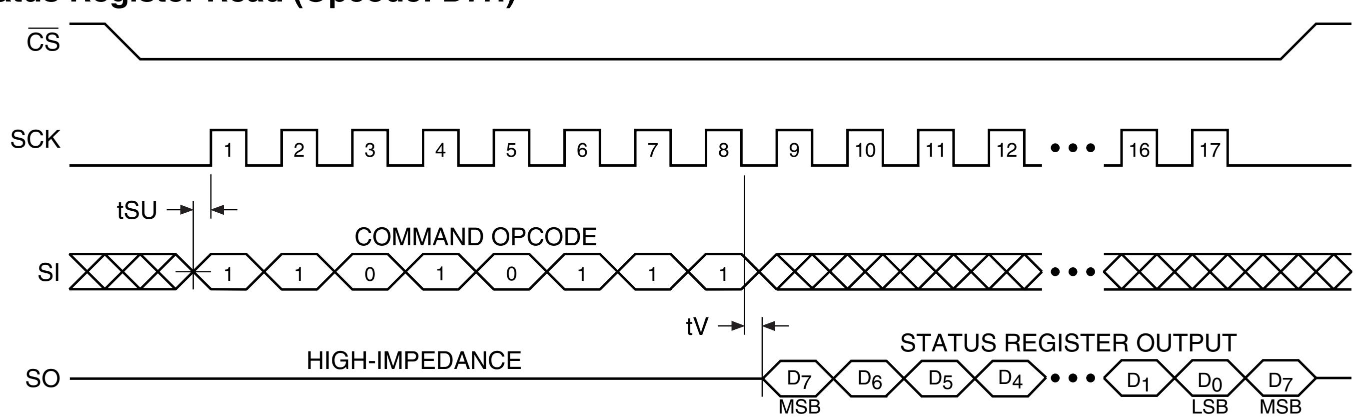
Main Memory Page Read (Opcode: D2H)



Buffer Read (Opcode: D4H or D6H)

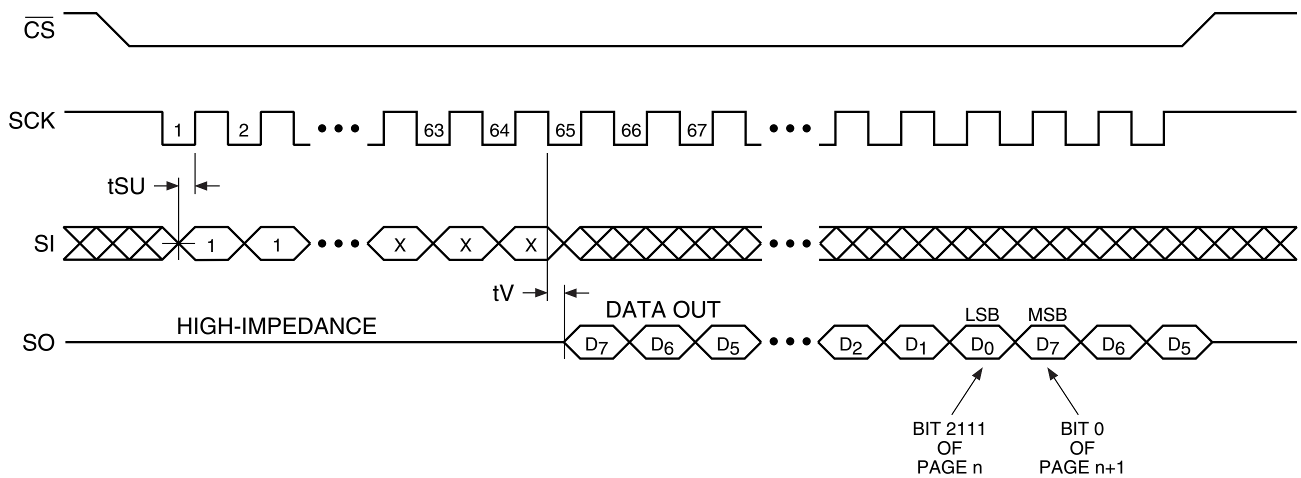


Status Register Read (Opcode: D7H)

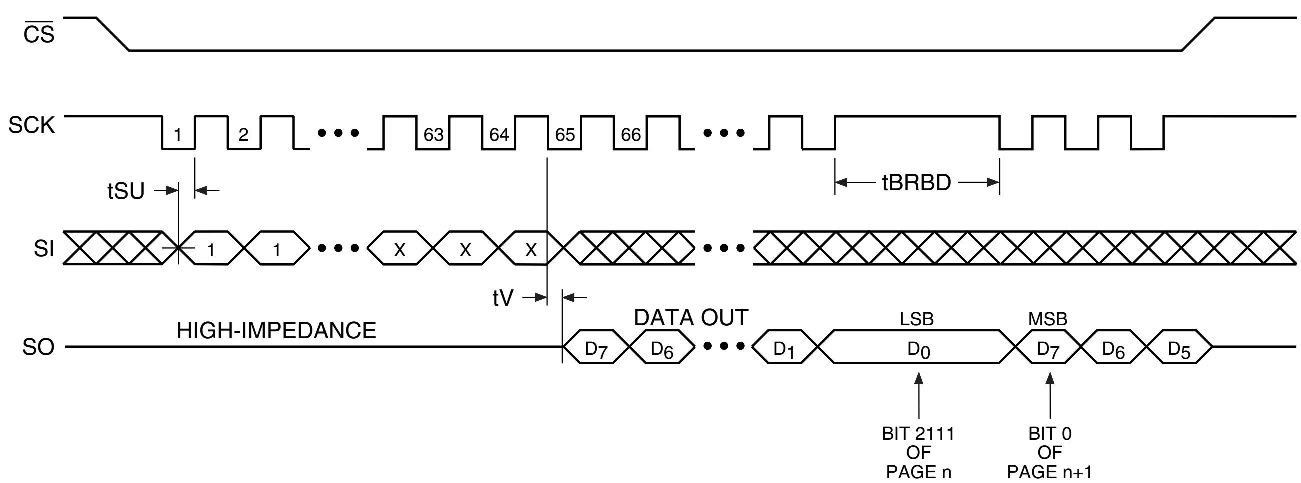


Detailed Bit-level Read Timing – SPI Mode 3

Continuous Array Read (Opcode: E8H)

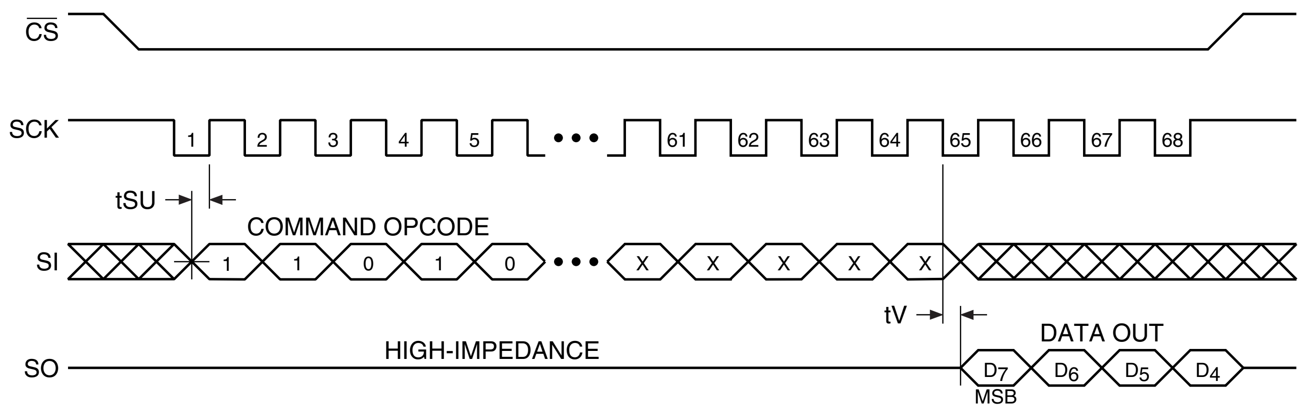


Burst Array Read (Opcode: E8H)

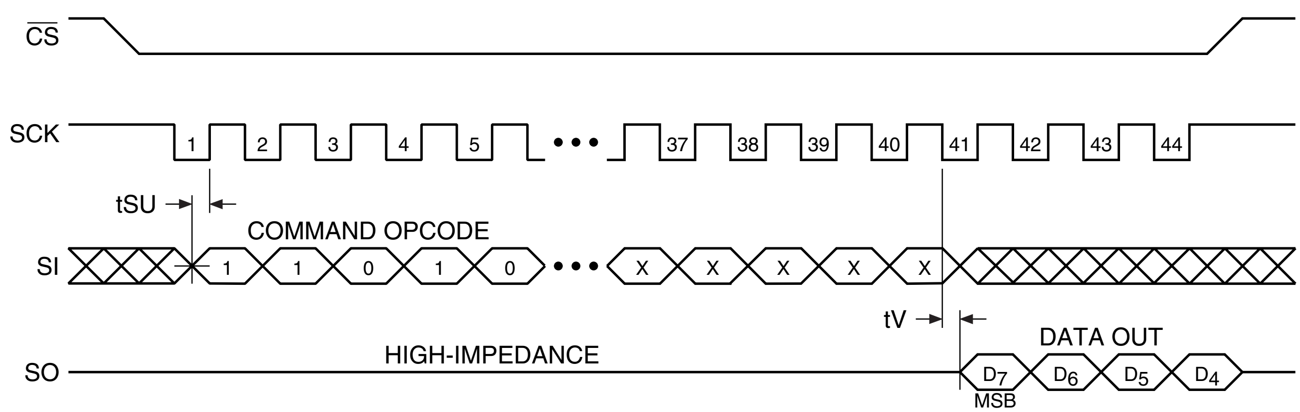


Detailed Bit-level Read Timing – SPI Mode 3 (Continued)

Main Memory Page Read (Opcode: D2H)



Buffer Read (Opcode: D4H or D6H)



Status Register Read (Opcode: D7H)

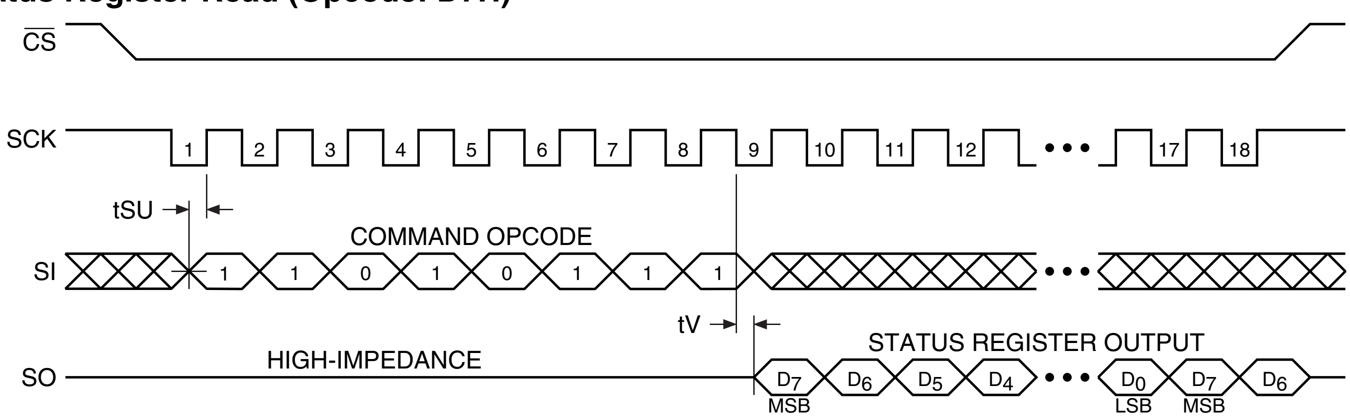
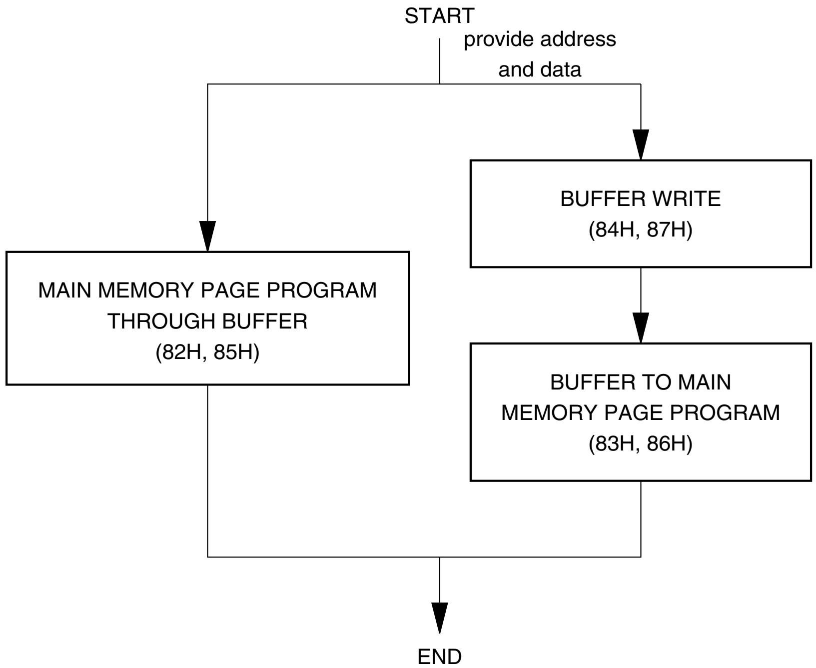
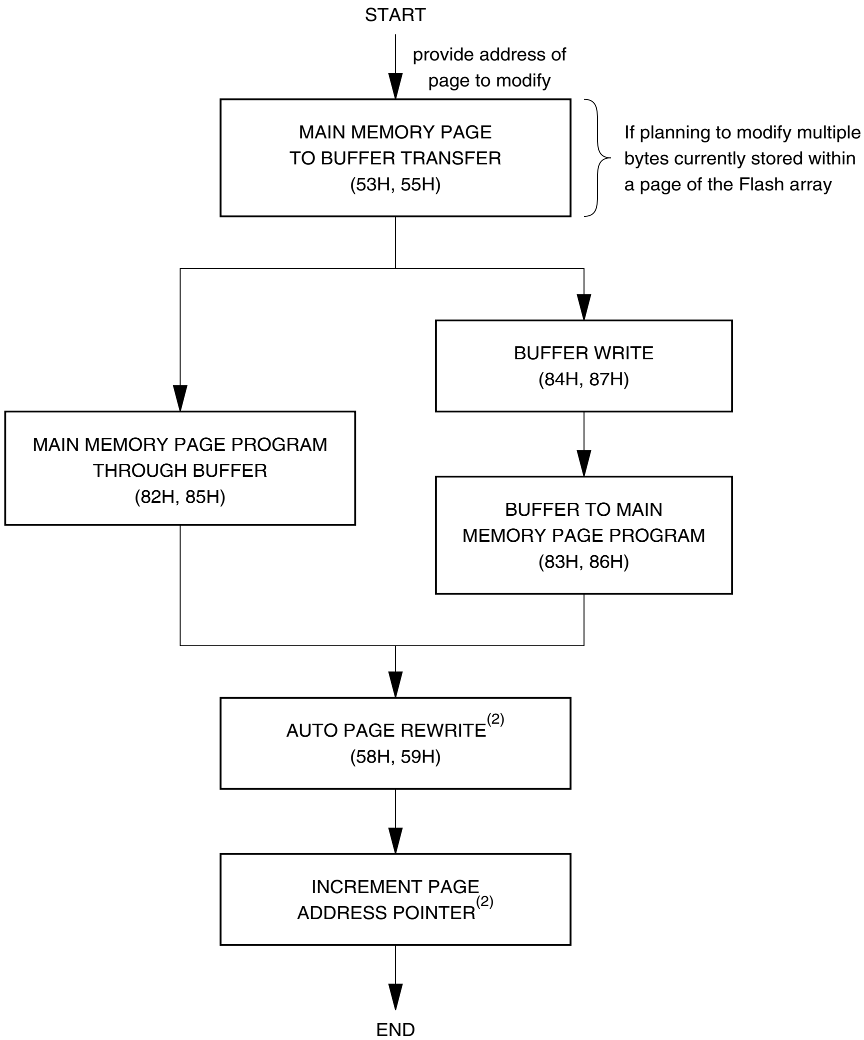


Figure 1. Algorithm for Sequentially Programming or Reprogramming the Entire Array



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

Sector Addressing

PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2-PA0	Sector
0	0	0	0	0	0	0	X	0
0	0	X	X	X	X	X	X	1
0	1	X	X	X	X	X	X	2
1	X	X	X	X	X	X	X	3

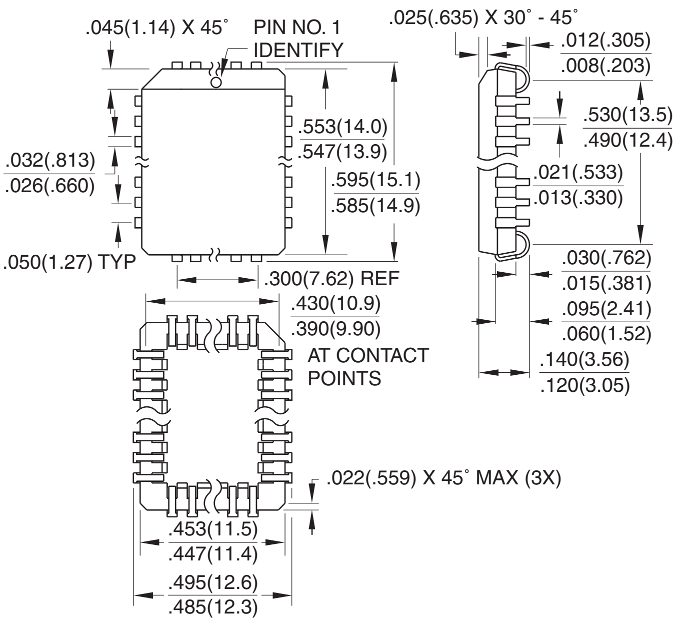
Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
15	25	0.02	AT45D021A-JC AT45D021A-RC AT45D021A-TC	32J 28R 28T	Commercial (0°C to 70°C)
15	25	0.02	AT45D021A-JI AT45D021A-RI AT45D021A-TI	32J 28R 28T	Industrial (-40°C to 85°C)

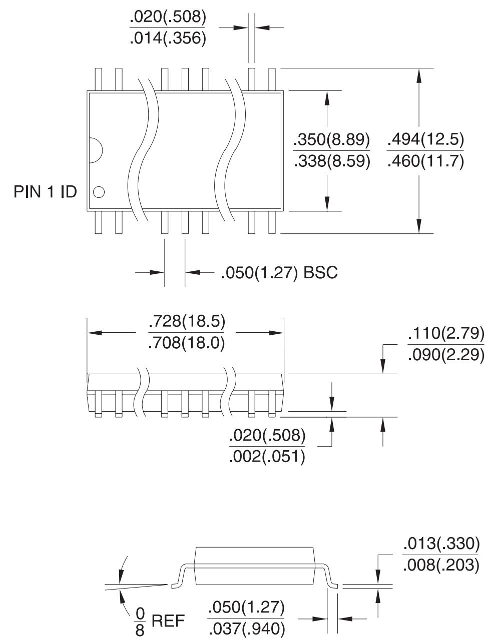
Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier Package (PLCC)
28R	28-lead, 0.330" Wide, Plastic Gull Wing Small Outline Package (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

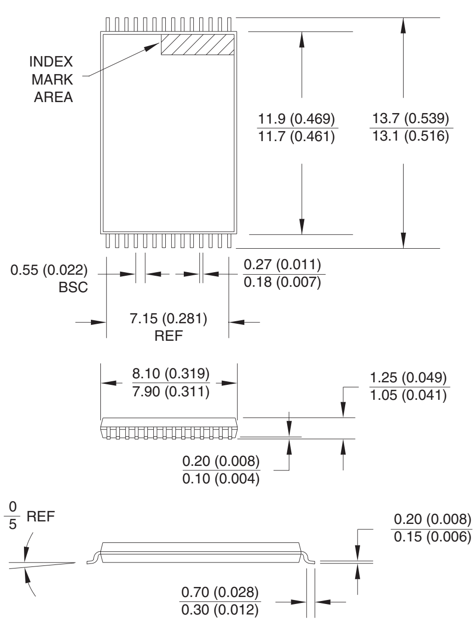
32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



28R, 28-lead, 0.330" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



28T, 28-lead, Plastic Thin Small Outline
Package (TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

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1639C–01/01/xM