Features

- **Single Supply for Read and Write: 2.7V to 3.3V (BV), 3.0V to 3.3V (LV)**
- **Access Time – 90 ns**
- **Sector Erase Architecture**
  - **Fourteen 32K Word (64K Byte) Sectors with Individual Write Lockout**
  - **Two 16K Word (32K Byte) Sectors with Individual Write Lockout**
  - **Two 8K Word (16K Byte) Sectors with Individual Write Lockout**
  - **Four 4K Word (8K Byte) Sectors with Individual Write Lockout**
- **Fast Word Program Time – 20 µs**
- **Fast Sector Erase Time – 200 ms**
- **Dual Plane Organization, Permitting Concurrent Read while Program/Erase**
  - **Memory Plane A: Four 4K Word, Two 8K Word and Two 16K Word Sectors**
  - **Memory Plane B: Fourteen 32K Word Sectors**
- **Erase Suspend Capability**
  - **Supports Reading/Programming Data from Any Sector by Suspending Erase of Any Different Sector**
- **Low-power Operation**
  - **25 mA Active**
  - **10 µA Standby**
- **$\overline{\text{Data}}$ Polling, Toggle Bit, Ready/$\overline{\text{Busy}}$ for End of Program Detection**
- **Optional VPP Pin for Fast Programming**
- **RESET Input for Device Initialization**
- **Sector Program Unlock Command**
- **TSOP and CBGA Package Options**
- **Top or Bottom Boot Block Configuration Available**

Description

The AT49BV/LV8011(T) is a 2.7- to 3.3-volt 8-megabit Flash memory organized as 524,288 words of 16 bits each or 1,048,576 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 22 sectors for erase operations. The device is offered in 48-pin TSOP and 48-ball CBGA packages. The device has $\overline{\text{CE}}$, and $\overline{\text{OE}}$ control signals to avoid any bus

(continued)

Pin Configurations

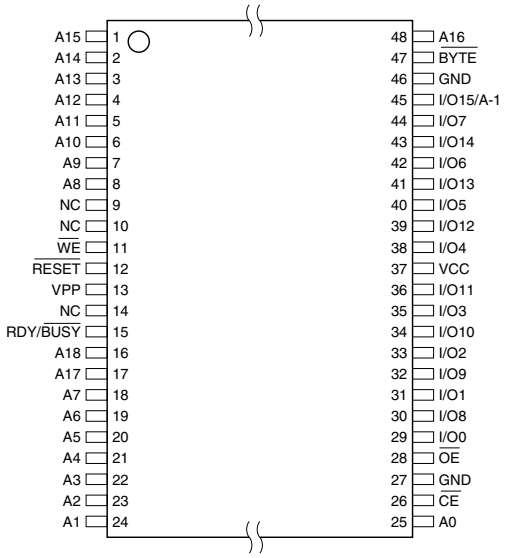
Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Reset
RDY/$\overline{\text{BUSY}}$	READY/$\overline{\text{BUSY}}$ Output
VPP	Optional Power Supply for Faster Program/Erase Operations
I/O0 - I/O14	Data Inputs/Outputs
I/O15 (A-1)	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
$\overline{\text{BYTE}}$	Selects Byte or Word Mode
NC	No Connect
VCCQ	Output Power Supply

8-megabit (512K x 16/1M x 8) 3-volt Only Flash Memory

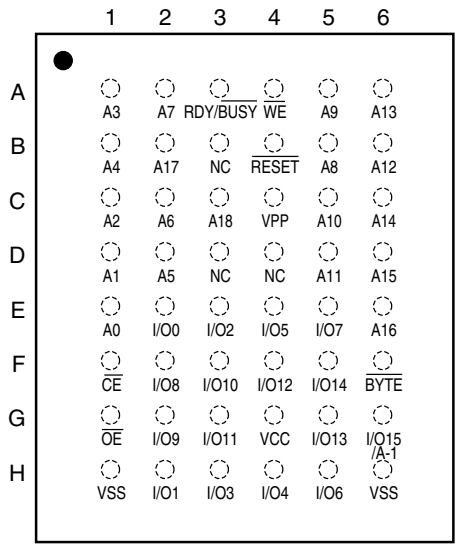
AT49BV8011
AT49BV8011T
AT49LV8011
AT49LV8011T

Rev. 1265E–01/00

TSOP Top View
Type 1



CBGA Top View



contention. This device can be read or reprogrammed using a single 2.7V power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as Program and Erase. The device has the capability to protect the data in any sector. Once the data protection for a given sector is enabled, the data in that sector cannot be changed using input levels between ground and V_{CC}.

The device is segmented into two memory planes. Reads from memory plane B may be performed even while program or erase functions are being executed in memory plane A and vice versa. This operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend feature. This feature will put the Erase on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the same memory plane. There is no reason to suspend the erase operation if the data to be read is in the other memory plane. The end of a program or an Erase cycle is detected by the Ready/$\overline{\text{Busy}}$ pin, $\overline{\text{Data}}$ polling, or by the toggle bit.

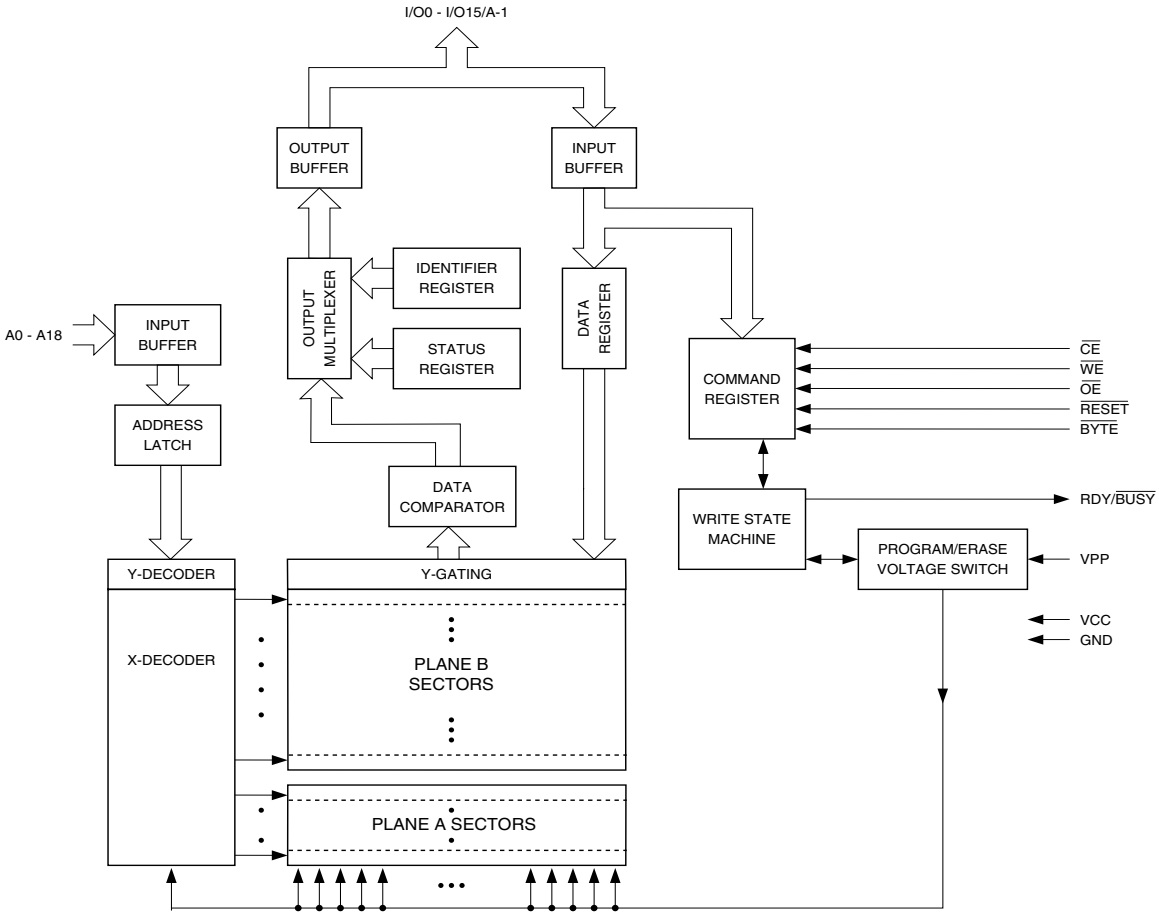
A VPP pin is provided to improve program/erase times. This pin can be tied to V_{CC}. To take advantage of faster programming and erasing, the pin should supply 4.5 to 5.5 volts during program and erase operations.

A 6-byte command (bypass unlock) sequence to remove the requirement of entering the 3-byte program sequence is offered to further improve programming time. After entering the 6-byte code, only single pulses on the write control lines are required for writing into the device. This mode (single-pulse byte/word program) is exited by powering down the device, or by pulsing the $\overline{\text{RESET}}$ pin low for a minimum of 50 ns and then bringing it back to V_{CC}. Erase and Erase Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the 6-byte code reside in the software of the final product but only exist in external programming code.

The $\overline{\text{BYTE}}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{\text{BYTE}}$ pin is set at logic “1”, the device is in word configuration, I/O0 - I/O15 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$.

If the $\overline{\text{BYTE}}$ pin is set at logic “0”, the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The data I/O pins I/O8 - I/O14 are tri-stated, and the I/O15 pin is used as an input for the LSB (A-1) address function.

Block Diagram



Device Operation

READ: The AT49BV/LV8011(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{RESET}$ pin, any sector can be reprogrammed even if the sector lockout feature has been enabled (see "Sector Programming Lockout Override" section).

ERASURE: Before a byte/word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase commands.

CHIP ERASE: The entire device can be erased at one time by using the 6-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the sector lockout has been enabled, the Chip Erase will not erase the data in the sector that has been locked; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into 22 sectors that can be individually erased. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H Data Input command is latched on the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a section is t_{SEC}. When the sector programming lockout feature is not enabled, the sector will erase (from the same Sector Erase command). Once a sector has been protected, data in the protected sectors cannot be changed unless the RESET pin is taken to 12V ± 0.5V. An attempt to erase a sector that has been protected will result in the operation terminating in 2 µs.

BYTE/WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical “0”) on a byte-by-byte or on a word-by-word basis. Programming is accomplished via the internal device command register and is a four bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature or the toggle bit feature may be used to indicate the end of a program cycle.

SECTOR PROGRAMMING LOCKOUT: Each sector has a programming lockout feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector’s usage as a write-protected region is optional to the user.

Once the feature is enabled, the data in the protected sectors can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the remaining sectors can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

SECTOR LOCKOUT DETECTION: A software method is available to determine if programming of a sector is locked out. When the device is in the software product identification mode (see “Software Product Identification Entry/Exit” sections), a read from address location 00002H within a sector will show if programming the sector is locked out. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

SECTOR PROGRAMMING LOCKOUT OVERRIDE: The user can override the sector programming lockout by taking the $\overline{RESET}$ pin to 12V ± 0.5V. By doing this, protected data can be altered through a chip erase, sector erase or byte/word programming. When the $\overline{RESET}$ pin is brought back to TTL levels, the sector programming lockout feature is again active.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the same plane. Since this device has a dual plane architecture, there is no need to use the erase suspend feature while erasing a sector when you want to read data from a sector in the other plane. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the plane that contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one bus cycle command that does require the plane address, which is determined by A18 - A16. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see “Operating Modes” (for hardware operation) or “Software Product Identification”. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49BV/LV8011(T) features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte/word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle. Please see “Status Bit Table” for more details.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling, the AT49BV/LV8011(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the same memory plane will result in I/O6 toggling between “1” and “0”. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

An additional toggle bit is available on I/O2, which can be used in conjunction with the toggle bit that is available on I/O6. While a sector is erase suspended, a read or a program operation from the suspended sector will result in the I/O2 bit toggling. Please see “Status Bit Table” for more details.

RDY/$\overline{\text{BUSY}}$: An open drain READY/$\overline{\text{BUSY}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49BV/LV8011(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.3V power supply, the address inputs and control inputs ($\overline{\text{OE}}$, $\overline{\text{CE}}$, and $\overline{\text{WE}}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

Command Definition in (Hex)[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[3][4]	30
Byte/Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Bypass Unlock	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	A0
Single-pulse Byte/Word Program	1	Addr	D_{IN}										
Sector Lockout	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[3][4]	40
Erase Suspend	1	xxxx	B0										
Erase Resume	1	PA[5]	30										
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit[2]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit[2]	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex).
   The ADDRESS FORMAT in each bus cycle is as follows: A15 - A0 (Hex). Address A18 through A14 are Don't Care in the word mode. Address A18 through A14 and A-1 are Don't Care in the byte mode.
2. Either one of the Product ID Exit commands can be used.
3. SA = sector address. Any byte/word address within a sector can be used to designate the sector address (see next two pages for details).
4. When the sector programming lockout feature is not enabled, the sector will erase (from the same Sector Erase command). Once the sector has been protected, data in the protected sectors cannot be changed unless the $\overline{\text{RESET}}$ pin is taken to 12V ± 0.5V.
5. PA is the plane address (A18 - A16).

Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AT49BV/LV8011 – Sector Address Table

Plane	Sector	Size (Bytes/Words)	x8 Address Range (A18 - A-1)	x16 Address Range (A18 - A0)
A	SA0	16K/8K	000000 - 003FFF	00000 - 01FFF
A	SA1	32K/16K	004000 - 00BFFF	02000 - 05FFF
A	SA2	8K/4K	00C000 - 00DFFF	06000 - 06FFF
A	SA3	8K/4K	00E000 - 00FFFF	07000 - 07FFF
A	SA4	8K/4K	010000 - 011FFF	08000 - 08FFF
A	SA5	8K/4K	012000 - 013FFF	09000 - 09FFF
A	SA6	32K/16K	014000 - 018FFF	0A000 - 0DFFF
A	SA7	16K/8K	01C000 - 01FFFF	0E000 - 0FFFF
B	SA8	64K/32K	020000 - 02FFFF	10000 - 17FFF
B	SA9	64K/32K	030000 - 03FFFF	18000 - 1FFFF
B	SA10	64K/32K	040000 - 04FFFF	20000 - 27FFF
B	SA11	64K/32K	050000 - 05FFFF	28000 - 2FFFF
B	SA12	64K/32K	060000 - 06FFFF	30000 - 37FFF
B	SA13	64K/32K	070000 - 07FFFF	38000 - 3FFFF
B	SA14	64K/32K	080000 - 08FFFF	40000 - 47FFF
B	SA15	64K/32K	090000 - 09FFFF	48000 - 4FFFF
B	SA16	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
B	SA17	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
B	SA18	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
B	SA19	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
B	SA20	64K/32K	0E0000 - 0EFFFF	70000 - 77FFF
B	SA21	64K/32K	0F0000 - 0FFFFF	78000 - 7FFFF

AT49BV/LV8011T – Sector Address Table

Plane	Sector	Size (Bytes/Words)	x8 Address Range (A18 - A-1)	x16 Address Range (A18 - A0)
B	SA0	64K/32K	000000 - 00FFFF	00000 - 07FFF
B	SA1	64K/32K	010000 - 01FFFF	08000 - 0FFFF
B	SA2	64K/32K	020000 - 02FFFF	10000 - 17FFF
B	SA3	64K/32K	030000 - 03FFFF	18000 - 1FFFF
B	SA4	64K/32K	040000 - 04FFFF	20000 - 27FFF
B	SA5	64K/32K	050000 - 05FFFF	28000 - 2FFFF
B	SA6	64K/32K	060000 - 06FFFF	30000 - 37FFF
B	SA7	64K/32K	070000 - 07FFFF	38000 - 3FFFF
B	SA8	64K/32K	080000 - 08FFFF	40000 - 47FFF
B	SA9	64K/32K	090000 - 09FFFF	48000 - 4FFFF
B	SA10	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
B	SA11	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
B	SA12	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
B	SA13	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
A	SA14	16K/8K	0E0000 - 0E3FFF	70000 - 71FFF
A	SA15	32K/16K	0E4000 - 0EBFFF	72000 - 75FFF
A	SA16	8K/4K	0EC000 - 0EDFFF	76000 - 76FFF
A	SA17	8K/4K	0EE000 - 0EFFFF	77000 - 77FFF
A	SA18	8K/4K	0F0000 - 0F1FFF	78000 - 78FFF
A	SA19	8K/4K	0F2000 - 0F3FFF	79000 - 79FFF
A	SA20	32K/16K	0F4000 - 0FBFFF	7A000 - 7DFFF
A	SA21	16K/8K	0FC000 - 0FFFFF	7E000 - 7FFFF

DC and AC Operating Range

		AT49LV8011(T)-90	AT49BV8011(T)-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.3V	2.7V to 3.3V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[6]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{CC}	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High-Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
Program Inhibit	X	V_{IL}	X	V_{IH}	X		
Output Disable	X	V_{IH}	X	V_{IH}	X		High-Z
Reset	X	X	X	V_{IL}	X	X	High-Z
Product Identification							
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}		A1 - A18 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
						A1 - A18 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}		A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code[4]
						A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH (x8); 001FH (x16), Device Code: 00CB-AT49BV8011; 004A-AT49BV8011T.
5. See details under “Software Product Identification Entry/Exit”.
6. For faster program/erase operations, V_{PP} = 5V ± 10%.

DC Characteristics

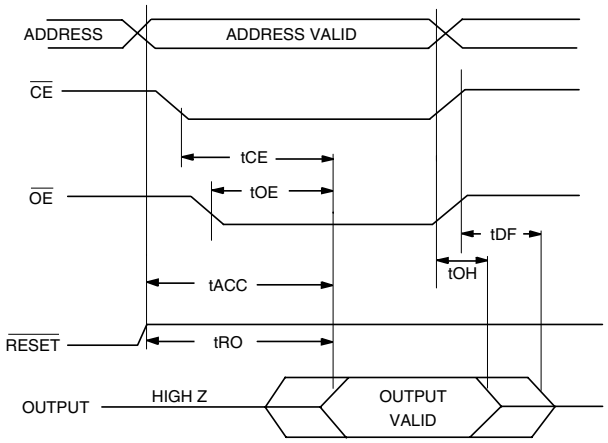
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		10	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC}[1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		30	mA
I_{CCRW}	V_{CC} Read while Write Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

AC Read Characteristics

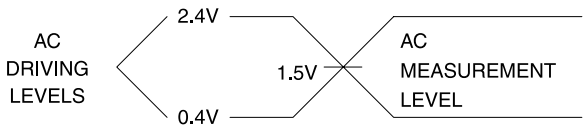
Symbol	Parameter	AT49LV8011(T)-90		AT49BV8011(T)-12		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	40	0	50	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		800		800	ns

AC Read Waveforms[1][2][3][4]



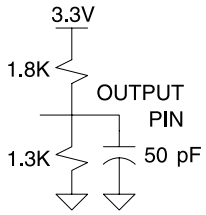
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

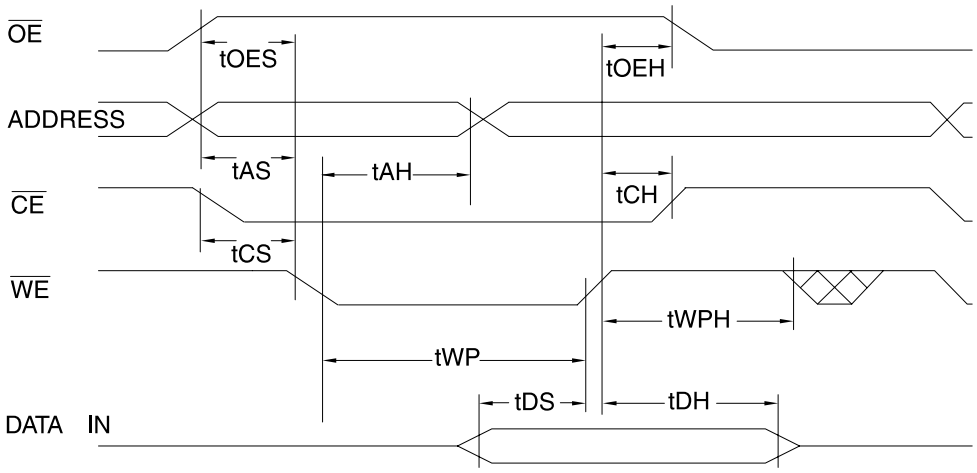
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte/Word Load Characteristics

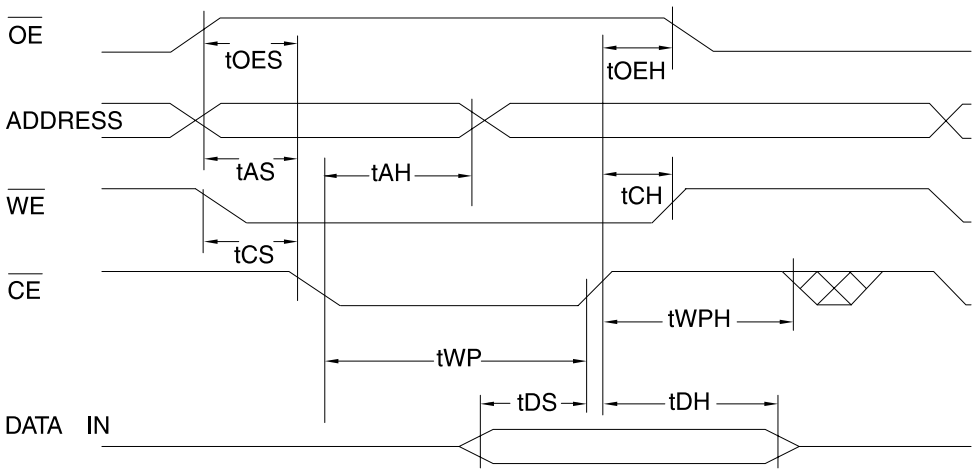
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Setup Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	50		ns

AC Byte/Word Load Waveforms

$\overline{WE}$ Controlled



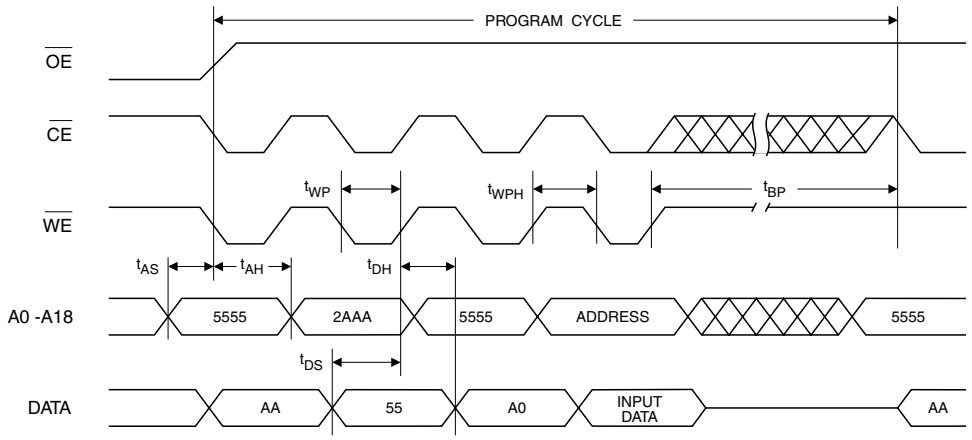
$\overline{CE}$ Controlled



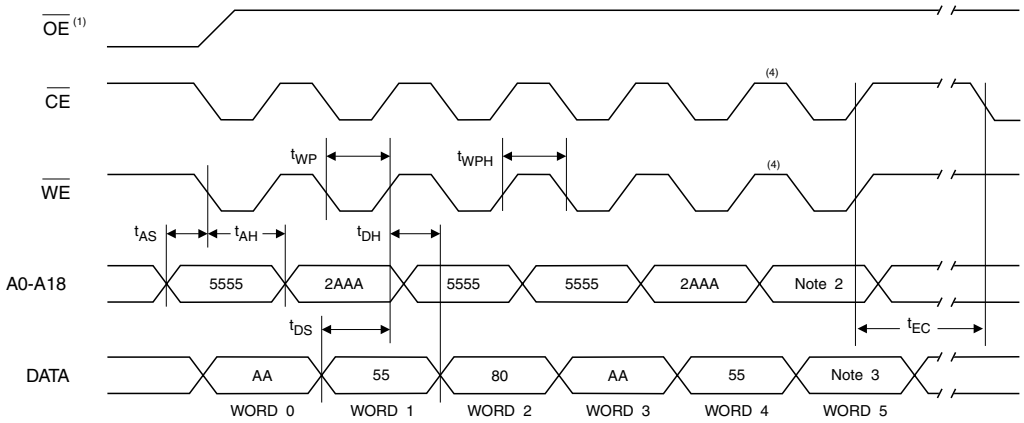
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte/Word Programming Time		20	50	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	100			ns
t_{DS}	Data Setup Time	100			ns
t_{DH}	Data Hold Time	10			ns
t_{WP}	Write Pulse Width	100			ns
t_{WPH}	Write Pulse Width High	50			ns
t_{EC}	Chip Erase Cycle Time			10	seconds
t_{SEC}	Sector Erase Cycle Time		200		ms

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



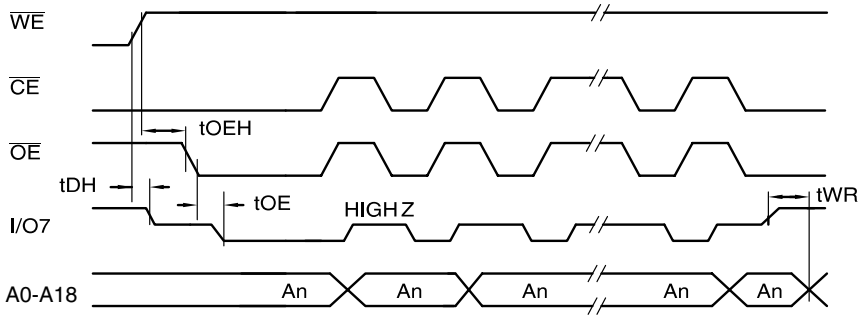
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 3 under command definitions.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.
4. The t_{WPH} time between the 5th and 6th bus cycle should be a minimum of 150 ns.

$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics".

$\overline{\text{Data}}$ Polling Waveforms

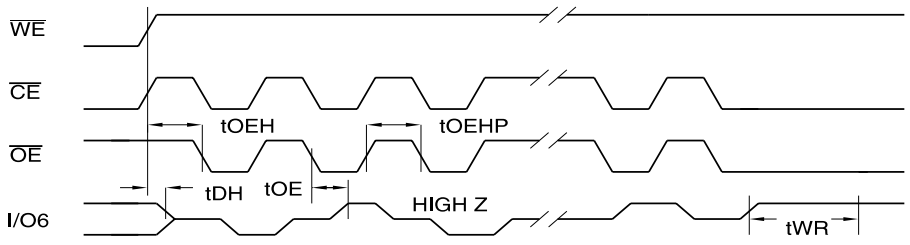


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

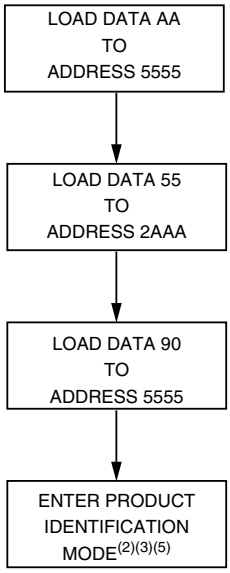
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics".

Toggle Bit Waveforms(1)(2)(3)

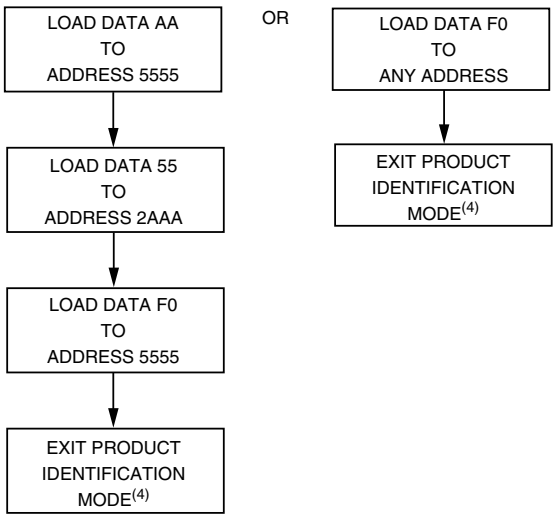


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

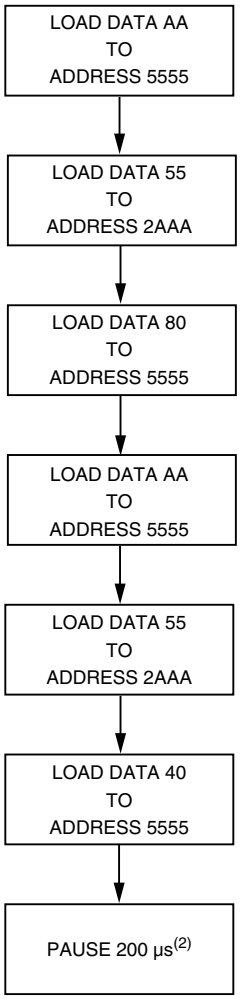


Software Product Identification Exit[1][7]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A15 - A0 (Hex), A-1, and A15 - A18 (Don't Care).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH(x8); 001FH(x16)
6. Device Code: 00CB-AT49BV8011;
   004A-AT49BV8011T.
7. Either one of the Product ID Exit commands can be used.

Sector Lockout Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A15 - A0 (Hex), A-1, and A15 - A18 (Don't Care).
2. Sector lockout feature enabled.

Status Bit Table

	Status Bit					
	I/O7		I/O6		I/O2	
Read Address In	**Plane A**	**Plane B**	**Plane A**	**Plane B**	**Plane A**	**Plane B**
While						
Programming in Plane A	$\overline{I/O7}$	DATA	TOGGLE	DATA	1	DATA
Programming in Plane B	DATA	$\overline{I/O7}$	DATA	TOGGLE	DATA	1
Erasing in Plane A	0	DATA	TOGGLE	DATA	TOGGLE	DATA
Erasing in Plane B	DATA	0	DATA	TOGGLE	DATA	TOGGLE
Erase Suspended & Read Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA
Erase Suspended & Program Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Program Non-erasing Sector in Plane A	$\overline{I/O7}$	DATA	TOGGLE	DATA	TOGGLE	DATA
Erase Suspended & Program Non-erasing Sector in Plane B	DATA	$\overline{I/O7}$	DATA	TOGGLE	DATA	TOGGLE

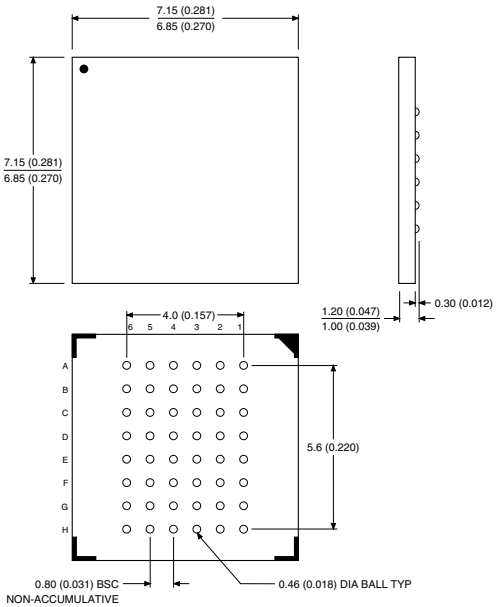
AT49BV/LV8011(T) Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	25	0.01	AT49LV8011-90CC AT49LV8011-90TC	48C3 48T	Commercial (0° to 70°C)
	25	0.01	AT49LV8011-90CI AT49LV8011-90TI	48C3 48T	Industrial (-40° to 85°C)
120	25	0.01	AT49BV8011-12CC AT49BV8011-12TC	48C3 48T	Commercial (0° to 70°C)
	25	0.01	AT49BV8011-12CI AT49BV8011-12TI	48C3 48T	Industrial (-40° to 85°C)
90	25	0.01	AT49LV8011T-90CC AT49LV8011T-90TC	48C3 48T	Commercial (0° to 70°C)
	25	0.01	AT49LV8011T-90CI AT49LV8011T-90TI	48C3 48T	Industrial (-40° to 85°C)
120	25	0.01	AT49BV8011T-12CC AT49BV8011T-12TC	48C3 48T	Commercial (0° to 70°C)
	25	0.01	AT49BV8011T-12CI AT49BV8011T-12TI	48C3 48T	Industrial (-40° to 85°C)

Package Type	
48C3	48-ball, Plastic Chip-size Ball Grid Array Package (CBGA)
48T	48-lead, Thin Small Outline Package (TSOP)

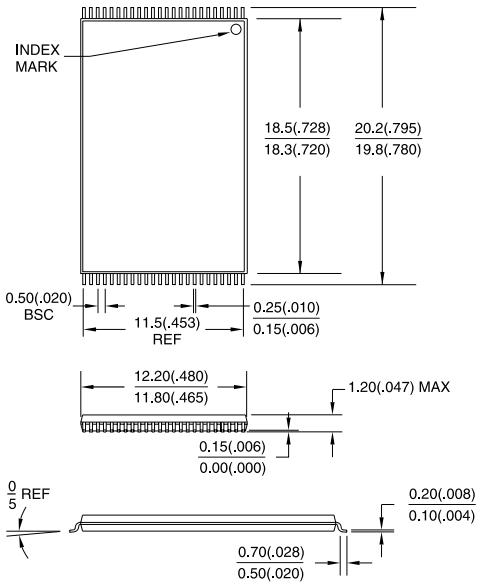
Packaging Information

48C3, 48-ball, Plastic Chip-size Ball Grid Array Package (CBGA)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

48T, 48-lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 DD



*Controlling dimension: millimeters

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