AT5819

2.0A Low Dropout Regulator with Enable

Immense Advance Tech.

FEATURES

- Reference voltage 0.8V
- Input voltage as low as 1.4V and VPP voltage 5V
- 300mV dropout @2A
- Over current, short circuit and over temperature protection
- Enable function
- Low reverse leakage (output to input)
- High output voltage accuracy ±2%
- Power Good signal
- Adjustable output voltage by external resistors
- V_{OUT} pull low resistance when disable

DESCRIPTION

The AT5819 is a 2A low dropout high performance linear voltage regulator, that provides a low voltage, high current output with a minimum of external components, utilizing dual supply configuration.

The AT5819 offers a low input voltage range from 1.4 V to 5.5V and is ideal for applications that need to convert down to 0.8V.

Additionally, the AT5819 is fully protected with current limit, short circuit and thermal shutdown. Also, there is an EN input which enables or shuts down the device.

APPLICATION

- Motherboards application
- Peripheral cards
- Network cards
- Set top boxes
- Notebook PC applications

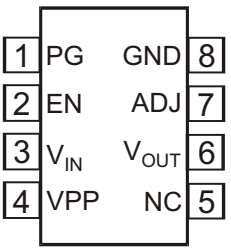
ORDERING INFORMATION

AT 5819- SF8 R

- AT: IAT
- 5819: Circuit Type
- SF8: PSOP-8
- R: Shipping — R: Tape & Reel, T: Tube

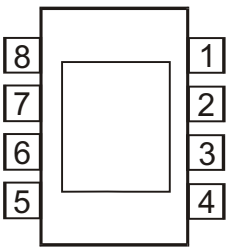
PIN CONFIGURATIONS

TOP VIEW



PSOP-8

BOTTOM VIEW

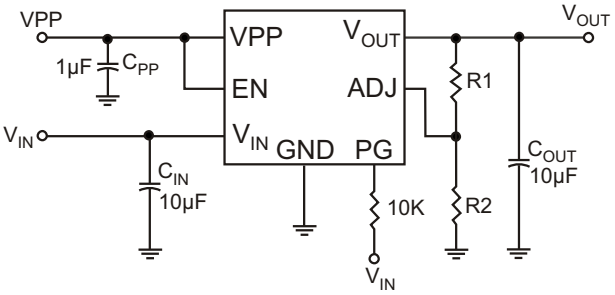


PSOP-8

PIN DESCRIPTIONS

Pin NO.	Pin Name	Pin Description
Pin 1	PG	Assert high once V_{OUT} reaches 92% of its rating voltage. Power Good Open Drain Output.
Pin 2	EN	Chip Enable (Active-High).
Pin 3	V_{IN}	Supply Input Voltage.
Pin 4	VPP	Supply Voltage of Control Circuitry.
Pin 5	NC	No Internal Connection.
Pin 6	V_{OUT}	Output Voltage.
Pin 7	ADJ	Set the output voltage by the internal feedback resistors when ADJ is grounded. If external feedback resistors is used: $V_{OUT} = \frac{0.8\ (R1+R2)}{R2}$ (Figure 1.)
Pin 8	GND	Ground.

TYPICAL APPLICATION CIRCUITS



$$V_{OUT} = \frac{0.8(R1+R2)}{R2}$$

R2< 120KΩ is recommended

Figure 1. Adjustable Voltage Regulator

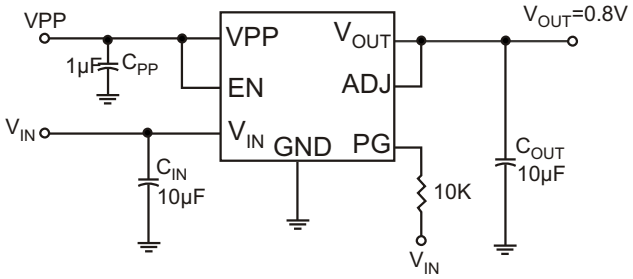


Figure 2. Fixed Voltage Regulator

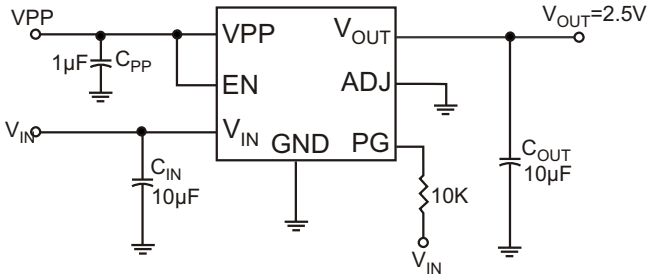
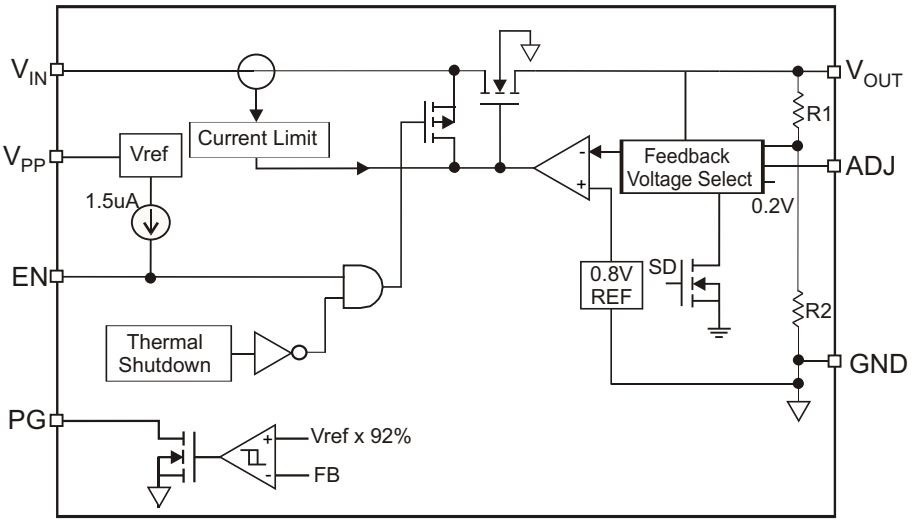


Figure 3. Fixed Voltage Regulator

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Max Value	Unit
Supply Voltage, V_{IN}	V_{IN}	6	V
Control Voltage, VPP, EN	VPP	6	V
Output Voltage, V_{OUT}	V_{OUT}	6	V
Power Dissipation, P_D @ T_A=25°C PSOP-8(Exposed Pad)	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient (Note2) PSOP-8	Θ_{JA}	36	°C/W
Junction Temperature	T_J	125	°C
Lead Temperature(Soldering) 5 Sec.	T_{LEAD}	260	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
ESD Susceptibility (Note 3) HBM (Human Body Mode)	V_{ESD}	2	kV

RECOMMENDED OPERATING CONDITIONS (Note 4)

Parameter	Symbol	Operation Conditions	Unit
Supply Voltage, V_{IN}	V_{IN}	1.4 to 5.5	V
Control Voltage, VPP	VPP	4.5 to 5.5	V
Output Voltage, V_{OUT}	V_{OUT}	0.8 to 5.5	V
Junction Temperature Range	T_J	-40 to 125	°C
Ambient Temperature Range	T_A	-40 to 85	°C

Notes 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Notes 2: 2 square inch of FR-4 , double sided, 1 oz. minimum copper weight.

Notes 3: Devices are ESD sensitive. Handling precaution recommended.

Notes 4: The device is not guaranteed to function outside its operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} =V_{OUT} +500mV, V_{EN}= VPP =5V, C_{IN} =C_{OUT} =10uF, T_A=T_J =25°C, unless otherwise specified.

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
V_{IN}							
Supply Voltage, V_{IN}		V_{IN}		1.4		5.5	V
VPP							
VPP Operation Voltage Range		VPP	VPP Input Range	4.5		5.5	V
VPP Shutdown Current		I_{PPL}	V_{EN} = 0V		10	20	μA
ADJ							
Adjustable Pin Threshold		V_{TH_ADJ}		0.15	0.2	0.25	V
Reference Voltage (ADJ Pin Voltage)		V_{ADJ}	V_{ADJ}=V_{OUT}	0.788	0.8	0.812	V
V_{OUT}							
Fixed Output Voltage Range		V_{OUT}	V_{IN}=V_{OUT}+500mV, V_{ADJ} =GND	2.45	2.5	2.55	V
Line Regulation (V_{IN})		$REG_{(LINE)}$	V_{IN}=V_{OUT}+0.5V to 5V, I_{OUT}=1mA		0.2	1	%
Load Regulation (Note 7)		$REG_{(LOAD)}$	V_{IN}=V_{OUT}+1V, I_{OUT} =10mA to 2A		0.2	1	%
Dropout Voltage (Note 5)		V_D	I_{OUT}=2A		250	300	mV
Quiescent Current (Note 6)		I_Q			0.25	0.5	mA
Short Circuit Protection Current					1.4		A
V_{OUT} Pull Low Resistance			V_{EN}=0V		90		Ω
Enable							
EN Input Bias current		I_{EN}	V_{EN} = 0V		12	20	μA
EN Threshold	Logic-Low Voltage	V_{ENL}	VPP= 5V			0.4	V
	Logic-High Voltage	V_{ENH}	VPP= 5V	1.6			
Power Good							
PG Rising Threshold					92		%
PG Hysteresis					7		%
Thermal Protection							
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		$\triangle T_{SD}$			30		°C

Notes 5: Defined as the input to output differential at which the output voltage drops to 2% below the value measured at a differential of 0.8V and V_{OUT} set to 2.5V.

Notes 6: Quiescent, or ground current, is the difference between input and output currents. It is defined by I_Q=I_{IN}-I_{OUT} under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

Notes 7: Regulation is measured at constant junction temperature by using a pulsed current .

APPLICATION INFORMATION

Adjustable Mode Operation

The output voltage of AT5819 is adjustable from 0.8V to 5.5V by external voltage divider resisters as shown in Typical Application Circuit(Figure 1). The value of resisters R1 and R2 should be more than 10KΩ to reduce the power loss.

Enable

The AT5819 goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 10μA typical. The AT5819 goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, NOTE that the AT5819 internal initial logic level. For AT5819, the EN pin function pulls high level internally. So the regulator will be turn on when EN pin is floating.

Output Capacitor

A minimum bulk capacitance of 10μF ceramic, along with a 0.1μF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response . The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors.

External Voltage Selection Resistors :

The use of 1% resistors, and consider for system stability and power losing , we recommend to design high dividing resistance (R2<120KΩ) to strengthen the benefits which AT819 has inherent .

Input Capacitor

A minimum of 10μF ceramic capacitor is recommended to be placed directly next to the V_{IN} pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance may be added closely to the input supply pin of the AT5819 to ensure that V_{IN} does not sag, improving load transient response.

Power Good

The Power Good function is an open-drain output. Connects 10KΩ Pull up resistor to V_{OUT} to obtain an output voltage. The PG pin will output high immediately after the output voltage arrives 92% of normal output voltage.

Power Dissipation

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D=(V_{IN}-V_{OUT})xI_{OUT}+V_{IN}xI_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)}=(T_{J(MAX)}-T_{A(MAX)})/\Theta_{JA}$$

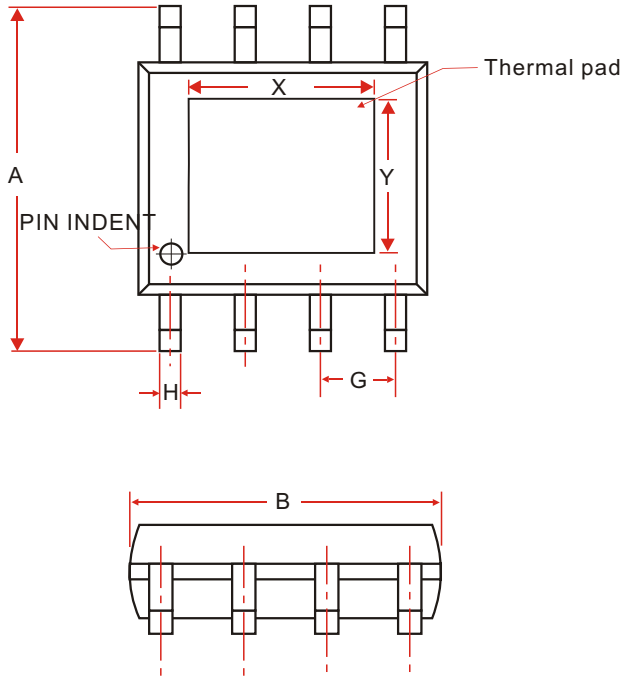
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the Θ_{JA} is the junction to ambient thermal resistance.

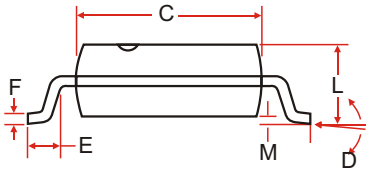
For recommended operation conditions specification of AT5819, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance for PSOP-8 (Exposed Pad) package is 36°C /W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at $T_{A(MAX)}$=85°C can be calculated by following formula:

$$P_{D(MAX)}=(125°C-85°C)/(36°C/W)=1.11W$$

(PSOP-8 Exposed Pad on the minimum layout)

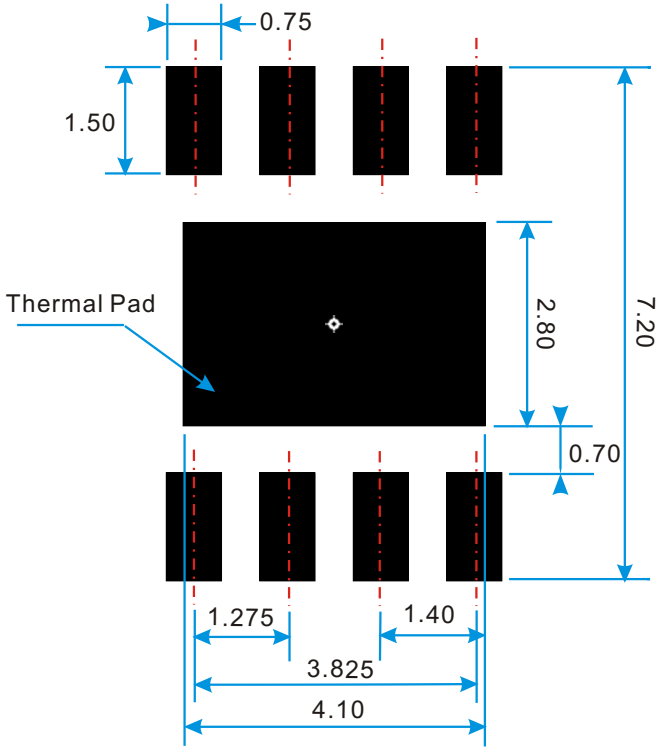
PSOP-8 PACKAGE OUTLINE DIMENSIONS





REF.	DIMENSIONS Millimeters	
	Min.	Max.
A	5.80	6.20
B	4.80	5.00
C	3.80	4.00
D	0°	8°
E	0.40	0.90
F	0.15	0.26
M	0	0.25
H	0.31	0.51
L	1.35	1.75
G	1.27 TYP.	
X	3.30 TYP.	
Y	2.50 TYP.	

PSOP-8 PACKAGE FOOTPRINT (mm)



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