



AT5C1008

Die Manufacturers Available	Device Pin Outs	
<ul style="list-style-type: none"> » Samsung » Cypress » G-Link 	<p>32-Pin DIP (C, CW) 32-Pin CSOJ (SOJ)</p>	<p>32-Pin LCC (ECA)</p>
<p style="text-align: center;">Product Features</p> <ul style="list-style-type: none"> » Operating Temperature range of +125°C to -55°C » Access times of: 12, 15, 20, 25, 30, 35, 45, 55 and 70 ns » Battery Backup: 2V data retention » Fast output enable (tAOE) for cache applications » Low standby power » Fully static operation, no clock or refresh required » TTL Compatible Inputs and Outputs » Easy memory expansion with CE1\, CE2, and OE\ options. » Single +5V power supply 		
<p>32-Pin Flat Pack (F)</p>		

General Description

The AT5C1008 SRAM employs high-speed, low power CMOS designs using a four-transistor memory cell, and are fabricated using double-layer metal, double-layer polysilicon technology. For design flexibility in high-speed memory applications, this device offers dual chip enables (CE1\, CE2) and output enable (OE\). These control pins can place the outputs in High-Z for additional flexibility in system design. All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible. Writing to these devices is accomplished when write enable (WE\) and CE1\ inputs are both LOW and CE2 is HIGH. Reading is accomplished when WE\ and CE2 remain HIGH and CE1\ and OE\ go LOW. The devices offer a reduced power standby mode when disabled, allowing system designs to achieve low standby power requirements. The "L" version offers a 2V data retention mode, reducing current consumption to 1mA maximum. For further electrical specifications please contact Anloy Technologies or reference the original die manufacturers datasheet.