AT7170

1A 1.5MHz Step-Down Converter

Immense Advance Tech.

FEATURES

- Up to 96% Efficiency
- Up to 1A Max Output Current
- 1.5MHz Frequency
- Light Load operation
- Internal Compensation
- SOT-25 Package

APPLICATION

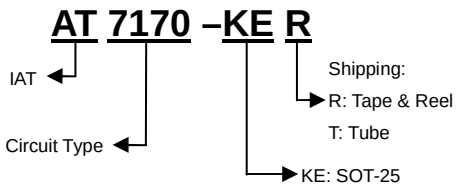
- MIDs, Tablet PC
- Set Top Boxes
- USB ports/Hubs
- Hot Swaps
- Cellphones

DESCRIPTION

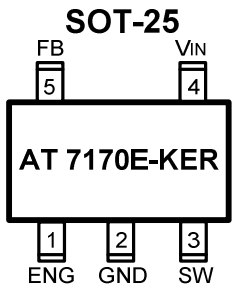
The AT7170 is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 1A of output current. The devices operate from an input voltage range of 2.6V to 5.5V and provide output voltages from 0.6V to VIN, making the AT7170 ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small inductance value and low DCR inductors, thereby achieving higher efficiencies. Other external components, such as ceramic input and output caps, can also be small due to higher switching frequency, while maintaining exceptional low noise output voltages. Built-in EMI reduction circuitry makes this converter ideal power supply for RF applications. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

AT7170 is housed in a tiny SOT25 package.

ORDER INFORMATION



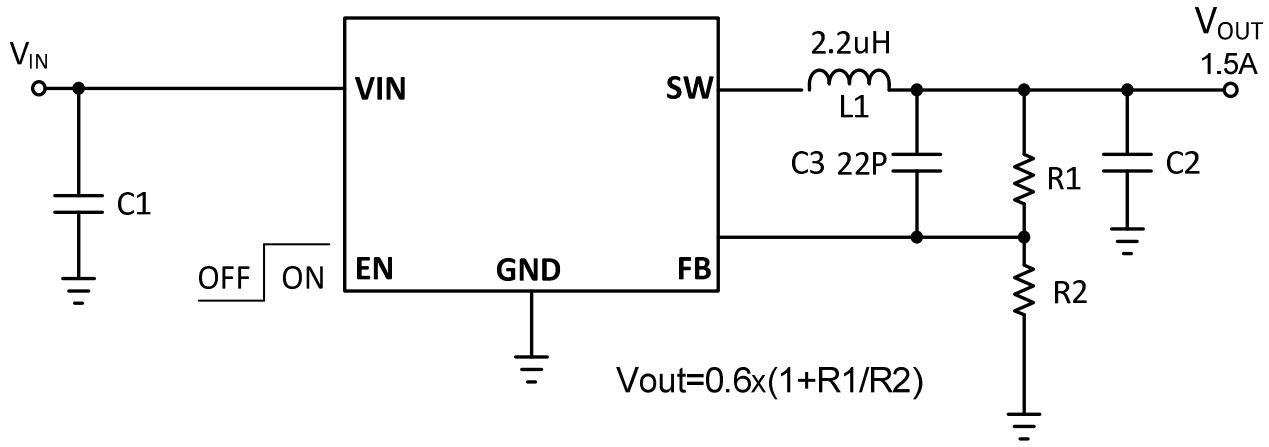
PIN CONFIGURATIONS (TOP VIEW)



PIN DESCRIPTIONS

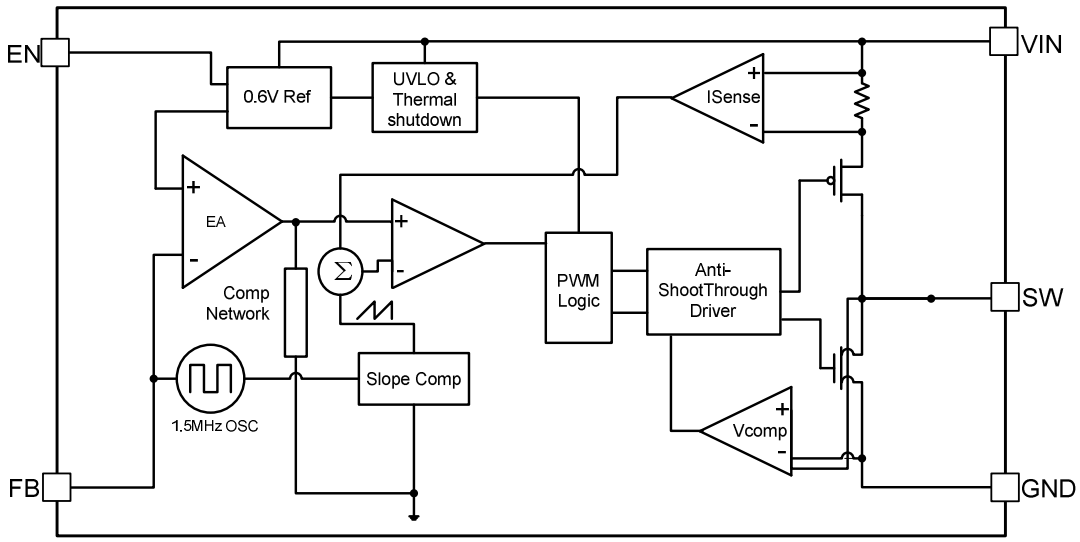
Pin Name	Pin Description
V_{IN}	Supply Voltage. Short to PIN. Bypass with a 10μF ceramic capacitor to GND.
GND	Ground.
EN	Enable pin for the IC. Drive this pin to high to enable the part, low to disable.
FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and VIN.
SW	Inductor Connection. Connect an inductor Between SW and the regulator output.

TYPICAL APPLICATION CIRCUITS



$V_{OUT}=V_{FB}$ x(1+R1/R2),V_{FB}=0.6V,R2 suggest 10k~300kΩ

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Max Value	Unit
VCC pin voltage	V_{IN}	-0.3 to 7	V
SW pin voltage	V_{SW}	-0.7 to VIN+0.3	V
EN, FB pins voltage		-0.3 to VIN+0.3	V
Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃
Lead Temperature(Soldering) 5 Sec.	T_{LEAD}	260	℃
Power Dissipation, P_D @ T_A=25℃ (Note 2)	P_D	450	mW
Thermal Resistance Junction to Ambient	θ_{JA}	220	℃/ W
Thermal Resistance Junction to Case	θ_{JC}	106.6	℃/ W
ESD Rating (Human Body Model) (Note 2)	V_{ESD}	2	kV

ELECTRICAL CHARACTERISTICS

T_A=25℃, unless otherwise specified

Function Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range			2.6	—	6	V
Input UVLO		Rising, Hysteresis=90mV	—	2.31	2.45	V
Input Supply Current		V_{FB} =0.65V	—	40	70	μA
Input Shutdown Current			—	—	1	μA
FB Feedback Voltage		V_{IN} =2.5 to 5V	0.588	0.6	0.612	V
FB Input Current			—	0.01	—	μA
Output Voltage Range			0.6	—	V_{IN}	V
Load Regulation		V_{OUT}=1.8V, I_{OUT}From 0.2A to 0.4A	—	0.1	—	%
Line Regulation		V_{IN} =2.7 to 5.5V	—	0.2	—	%/V
Switching Frequency			—	1.5	—	MHz
NMOS Switch On Resistance		I_{SW} =200mA	—	200	—	mΩ
PMOS Switch On Resistance		I_{SW} =200mA	—	280	—	mΩ
PMOS Switch Current Limit			1.5	—	—	A
SW Leakage Current		V_{IN}=5.5V,V_{SW}=0 or 5.5V,EN= GND	—	—	10	μA
EN Input Current			—	—	1	μA
EN Input Low Voltage			0.4	—	—	V
EN Input High Voltage			—	—	1.5	V

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stressratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: Thermal Resistance is specified with the component mounted on a low effective thermal conductivity test board in free air at T_A=25℃.

Note 3: Devices are ESD sensitive. Handing precaution recommended.

APPLICATION INFORMATION

The AT7170 highefficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 1A of output current. The device operates in pulse-width modulation (PWM) at 1.5MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.6V to VIN, making the AT7170 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Loop Operation

AT7170 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. AT7170 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to I_{PEAK} and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

AT7170 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If IN drops below 2.4V, the UVLO circuit inhibits switching. Once IN rises above 2.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160℃, a thermal sensor forces the device into shutdown, allowing the die to cool.

APPLICATION INFORMATION (CONTINUED)

The thermal sensor turns the device on again after the junction temperature cools by 15℃, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Setting Output Voltages

Output voltages are set by external resistors. The FBthreshold is 0.6V.

$R_{TOP} = R_{BOTTOM} x[(V_{OUT} / 0.6) - 1]$

Input Capacitor and Output Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. Input ripple with a ceramiccapacitor is approximately as follows:

$V_{RIPPLE} = IL_{(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{IN})]$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE(ESR)} = IL_{(PEAK)} \times ESR$

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance.

Inductor Selection

A reasonable inductor value (LIDEAL) can be derived from the following:

$L_{IDEAL} = [2(VIN) \times D(1 - D)] / I_{OUT} \times f_{OSC}$

PCB LAYOUT GUIDE

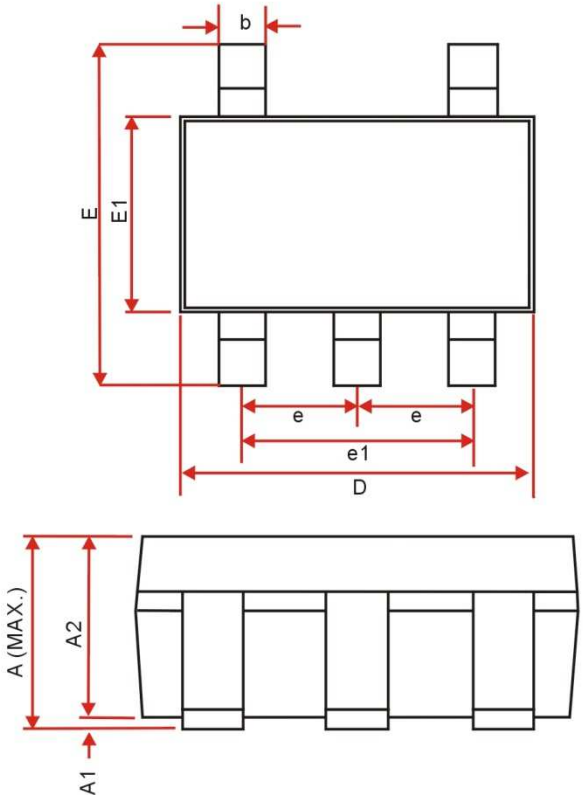
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

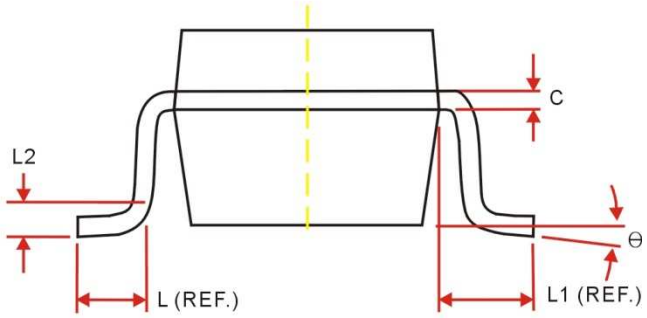
If change is necessary,please follow these guidelines and take Figure for reference.

1) Keep the path of switching current short and minimize the loop area formed by input cap,high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the Vin pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN,SW,and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

PACKAGE OUTLINE DIMENSIONS

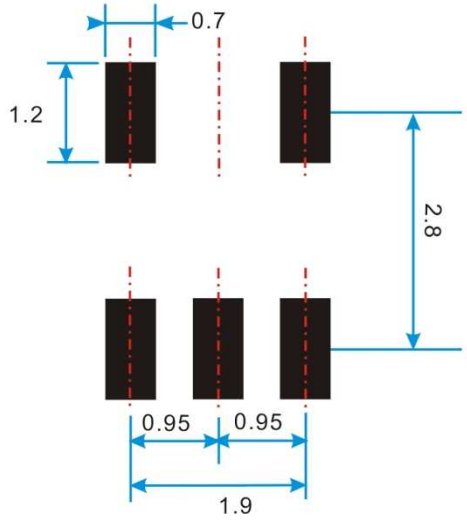
SOT-25 PACKAGE OUTLINE DIMENSIONS





Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.45 MAX.	
A1	0	0.15
A2	0.90	1.30
C	0.08	0.22
D	2.90 BSC.	
E	2.80 BSC.	
E1	1.60 BSC.	
L	0.30	0.60
L1	0.60 REF.	
L2	0.25 BSC.	
Θ	0°	10°
b	0.30	0.50
e	0.95 BSC.	
e1	1.90 BSC.	

SOT-25 PACKAGE FOOTPRINT(mm)



Note :

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