Features

- **300mA/1.8V/2.5V Switching Regulator for Baseband Supply**
- **2.8V/80mA LDO for Baseband Pad Supply**
- **Two 130mA/2.8V Low-noise, High PSRR RF LDO Voltage Regulators**
- **130mA/2.7V/2.8V Baseband Low-noise, High PSRR Analog LDO Regulator**
- **Ultra Low-power RTC LDO Voltage Regulator**
- **Backup Battery Charger**
- **Li-Ion or Li-polymer Battery Charger Controller**
- **Buzzer and Vibrator Drivers**
- **Charging LED Driver**
- **Power Management Start-up Controller and Reset Generation**
- **SIM Level Shifters and SIM 10mA/1.8V/2.8V LDO Voltage Regulator**
- **Ultra-low Sleep Mode Current Consumption (17 µA typ)**
- **Over and Under Voltage Protections**
- **Over Temperature Protection**
- **Low-power Mode and Sleep Mode**
- **Straight and Easy Interfacing to any Baseband Controller**
- **Small 5x5mm, Forty-nine Ball FBGA Package**

Description

The AT73C202 is a low-cost, ultra low-power, power and battery management IC designed to interface directly with state-of-the-art cellular phones, for example with 2.5G GSM phones. It includes all required power supplies tailored to be fully compatible with the sub-systems of recent mobile phone chipsets, including the RF, analog and digital (DSP, microcontroller, memories) sections.

The AT73C202 integrates a step-down DC-DC converter that supplies 300 mA with internal switches and two levels of voltage programming for the baseband core (1.8V and 2.5V). A low-power mode is available in order to minimize standby current consumption during the “quiet” transmission periods.

In addition, the AT73C202 includes a lowcost battery charger, using a simple external PNP transistor for Li-Ion or Li-Polymer batteries. Battery operating conditions are maintained within safe limits under hardware control during the start-up procedure (when the phone is turned on or a charger is plugged in). The battery pre-charge is also integrated and self-operated by the AT73C202. On completion the fast charge and end-of-charge procedure is transferred to the baseband software.

The AT73C202 integrates 7 low-dropout linear regulators specifically designed to supply RF (x2), analog, memories, etc. It also includes a back-up battery charger and an ultra low-power regulator dedicated to the baseband real-time clock (RTC) supply during sleep mode.

The hardwired start-up mechanism (power management controller state machine) ensures safe telephone operation during the wake-up and shut-down procedures, and during the multiple real-life operating conditions of a mobile phone (such charger plug-in, plug-out, battery plug-in, plug-out, low or dead battery, etc.).

The AT73C202 is packaged into a 49 ball (7x7 matrix), 0.65mm pitch, 5mm x 5mm outline FBGA package.

Power Management for Mobiles (PM)

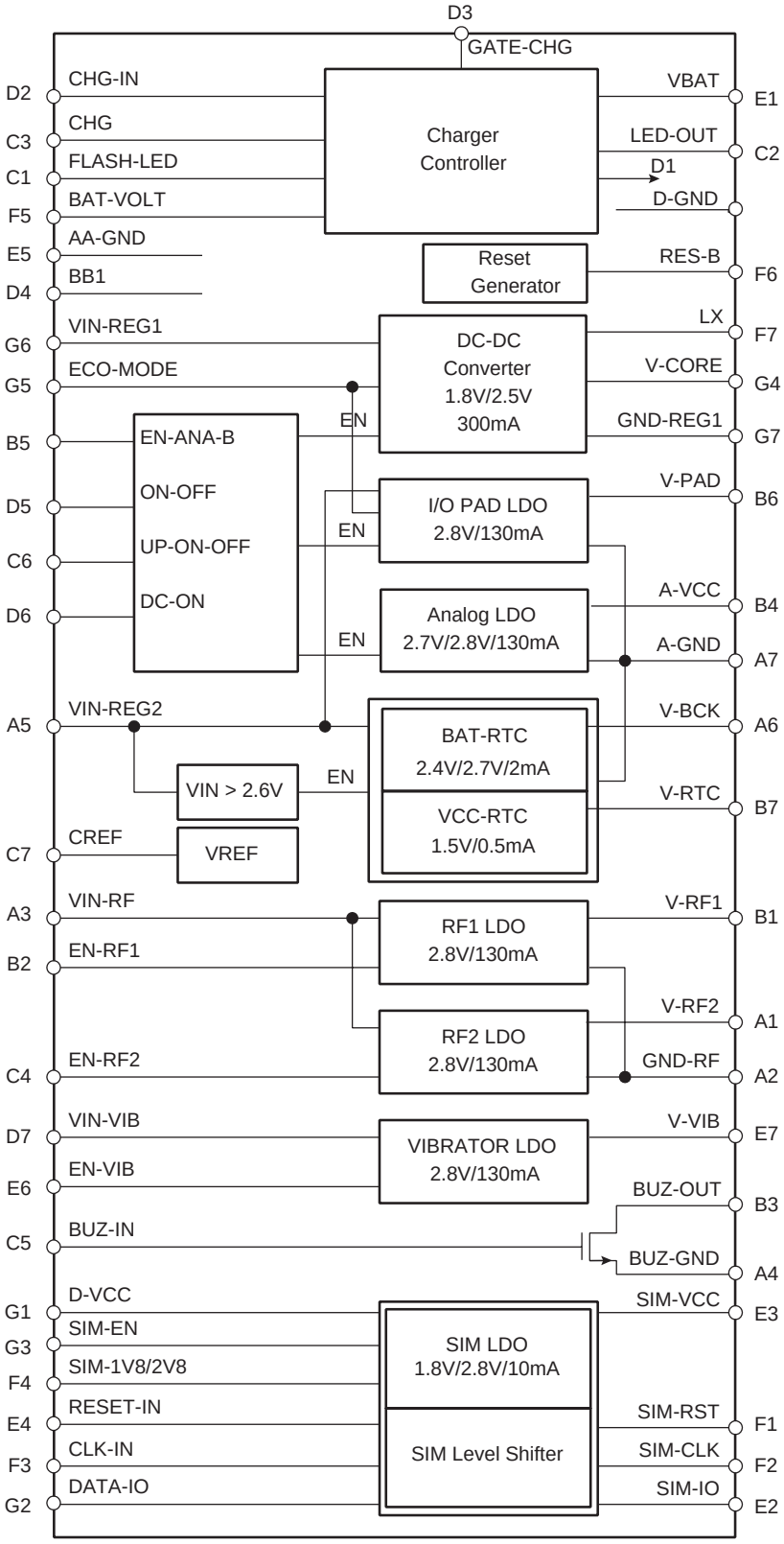
AT73C202 Power and Battery Management Unit for Cellular Phone

Preliminary

2740B–PMGMT–05/03

Functional Diagram

Figure 1. AT73C202 Functional Diagram



Pin Description

Table 1. AT73C202 Pin Description

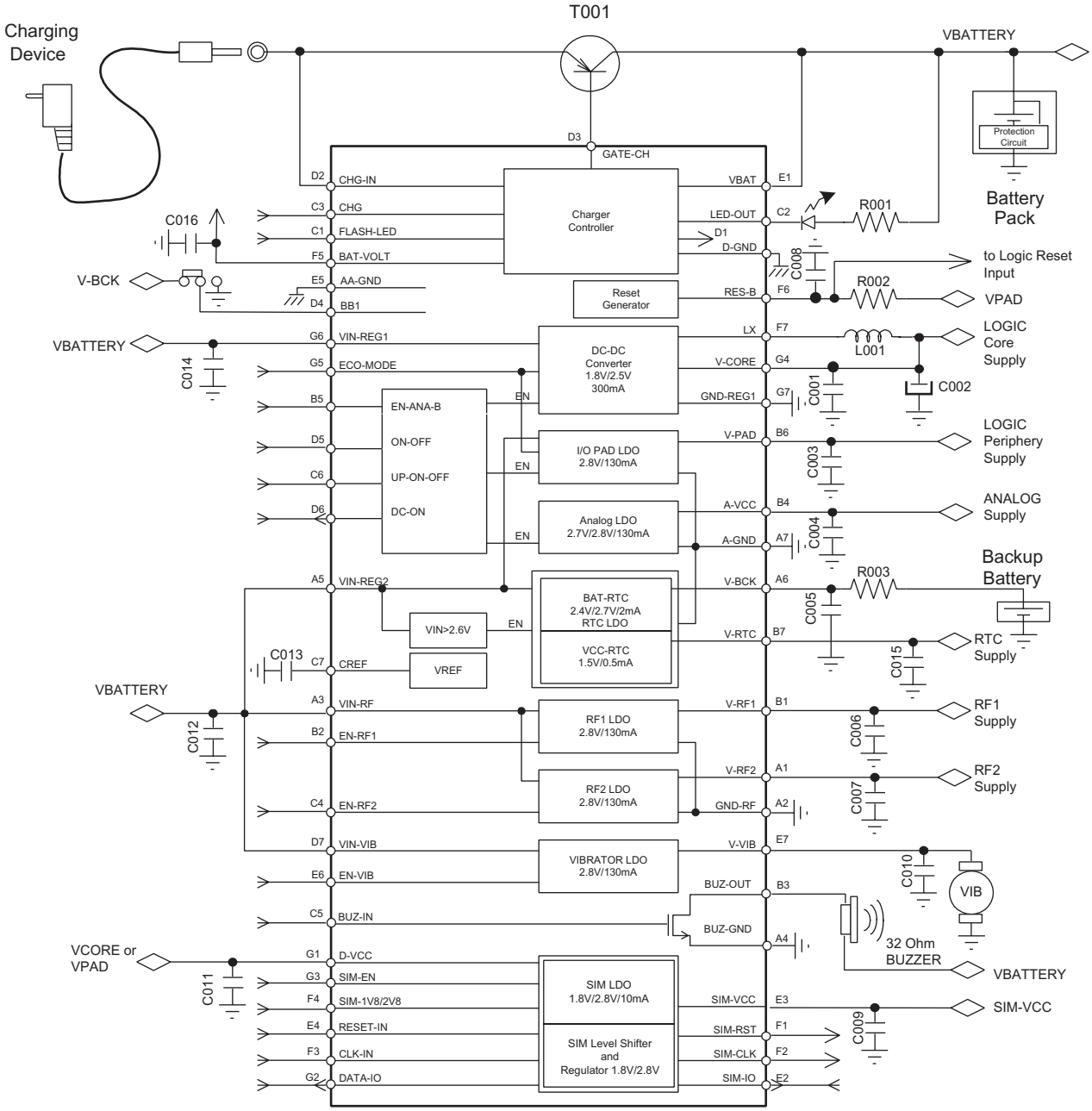
Signal	Ball	Type	Description
Charger Block			
CHG-IN	D2	Power Supply	AC/DC Adapter Input
GATE-CHG	D3	O	External PNP control output
CHG	C3	I	Charger command from Base Band chip
DC-ON	D6	O	AC/DC Adapter detector output
BAT-VOLT	F5	O	Resistance Divider output
FLASH-LED	C1	I	Flash LED input
LED-OUT	C2	O	LED output (Charging phase indicator)
VBAT (V_{BAT1})	E1	Power Supply	Battery Charger
Power On Block			
ON-OFF	D5	I	Key ON/OFF input
UP-ON-OFF	C6	I	Hold the Power ON from Base Band chip
RES-B	F6	O	Reset Open collector Output
AA-GND	E5	Ground	Analog ground
Baseband Supply Block			
VIN-REG1 (V_{BAT2})	G6	Power Supply	Input supply for DC/DC converter
LX	F7	O	DC/DC converter Output Inductor
ECO-MODE	G5	I	DC/DC converter Output (Base Band chip Core supply)
V-CORE	G4	O	DC/DC converter Output (Base Band chip Core supply)
GND-REG1	G7	Ground	Ground of DC/DC Converter
VIN-REG2 (V_{BAT3})	A5		Input supply for Base Band LDO
EN-ANA-B	B5	I	Enable the Analog LDO
A-VCC	B4	O	Analog LDO Output (Base Band chip Analog supply)
A-GND	A7	Ground	Ground of A-VCC, V-PAD and RTC LDO
V-PAD	B6	O	Digital LDO Output (Base Band chip Digital PAD supply)
V-RTC	B7	O	Base Band RTC supply output
V-BCK	A6	O	Back-up Battery RTC charger
RF Supply Block			
VIN-RF (V_{BAT4})	A3	Power Supply	Input supply for RF LDO
EN-RF1	B2	I	Enable LDO RF1
EN-RF2	C4	I	Enable LDO RF2
V-RF1	B1	O	RF1 LDO Output
GND-RF	A2	Ground	Ground of RF1 & RF2 LDO
V-RF2	A1	O	RF2 LDO Output

Table 1. AT73C202 Pin Description (Continued)

Signal	Ball	Type	Description
Vibrator and Buzzer Driver Block			
VIN-VIB (V_{BAT5})	D7	Power Supply	Input Vibrator LDO
EN-VIB	E6	I	Vibrator driver input (from Base Band chip)
V-VIB	E7	O	Vibrator LDO Output
BUZ-IN	C5	I	Buzzer driver input (from Base Band chip)
BUZ-OUT	B3	O	Buzzer output (connected to the buzzer)
BUZ-GND	A4	Ground	Ground of Buzzer Output
SIM Interface Block			
D-VCC	G1	Power Supply	Digital supply for SIM Base Band chip Interface
SIM-EN	G3	I	Input to Power ON the SIM
SIM-1V8/2V8	F4	I	Input to select the SIM Level (1.8V or 2.8V)
RESET-IN	E4	I	Reset Input from base band chip
CLK-IN	F3	I	Clock Input from base band chip
DATA-IO	G2	IO	Data Input/Output from base band chip
SIM-VCC	E3	O	SIM Power Supply (1.8V or 2.8V)
SIM-RST	F1	O	SIM Reset Output
SIM-CLK	F2	O	SIM Clock Output
SIM-IO	E2	IO	SIM Data Input/Output
Miscellaneous			
CREF	C7	IO	Band gap decoupling
D-GND	D1	Ground	Ground for Digital (Charger, SIM & Vibrator)
BB1	D4	I	Chip Configuration: BB1 = 0: First Platform BB1 = 1: Second Platform

Application Schematic

Figure 2. AT73202 Application Schematic



External Components Specifications

Table 2. External Component Specifications

Symbol	Parameters
R001	4.7 kΩ, 1/8 W, 0603
R002	4.7 kΩ, 1/8 W, 0603
R003	2 kΩ, 1/8 W, 0603
C001, C003, C004, C005, C006, C007, C010, C012	2.2µF - X5R 6.3V/10%, 0603
C002	22 µF Tantale R, TYPEA
C009, C011, C015	220 nF - X5R 10V/10%, 0603
C008, C013, C016	10 nF - X5R 10V/10%, 0402
C014	10 µF - X5R 6.3V/10%
L001	10 µH
T001	FMMT593 SOT23 PNP

Power ON Control Block

This block generates the Power ON and Power OFF for the AT73C202. Power ON is activated when one of these conditions is true:

- The AC/DC Charger is plugged (CHG-IN input): the DC-ON pin is then set to high level
- ON/OFF Key is set to high level, which sets the ON-OFF pin to high level
- UP-ON/OFF is set to high level

To achieve all Power ON, the conditions below must be true:

- Battery must be higher than normal operating voltage ($V_{BATTERY}$ > 3.2V)
- Thermal protection is right (T_J < 120°C)

When the ON/OFF Key is pressed (tied to V_{BAT}), the POWER-EN goes to high level and activates the Base Band Chip Core Supply. As the Base Band Chip detects the ON/OFF, it must drive UP-ON/OFF to high level in order to maintain the POWER-EN at high level and the ON/OFF key can be released. When the ON/OFF key is pressed again to power off, the base band chip releases the UP-ON/OFF pin to low level.

Note that UP-ON/OFF can also be generated as a wake-up alarm when the phone is in OFF mode (the UP-ON/OFF pin is supplied by the back-up battery on V-RTC (1.0V to 1.8V).

Charger Controller Block

There are three specific phases of battery charging:

- Pre-charge when V_{BAT} < 3.2V with 50 mA pulsed current stopped by either software or hardware if V_{BAT} > 3.6V or the software crashes.
- Fast charge with C_O current by software
- Pulse charging with C_O current for end of charge by software.

Note: C_O equals 600 mA when the battery capacity equals 600mAH.

Fast charging and pulse charging use only one switch. The pre-charging will be done using a pulse charging C_O during 100 ms each second.

Pre-charging Phase

When the Base Band Chip is powered OFF and battery voltage is under 3.2V, the charge must be performed by the AT73C202. To ensure no damage occurs, the current is limited to 50 mA or nominal capacity divided by 10 (C_O / 10).

When the base band chip is powered ON and sets CHG at high level the pre-charge phase is finished.

In case of a software crash after power on, a watchdog timer of 10s will set the RES-B to "0" and turn off the device.

Pulse & Fast charging

In this phase, the base band chip controls the charge through the CHG pin and monitors the battery voltage and temperature through BAT-VOLT on the AT73C202 and temperature through any available temperature sensor in the battery pack.

When Battery voltage is under 4.1V, the charger is always active (CHG is high level). As soon as battery voltage exceeds 4.1V, the software enters into a pulse charging phase. The pulse charging stops when battery voltage reaches 4.2V.

FLASH-LED Description

During the pre-charging phase, the phone is OFF. To indicate the pre-charging is currently running, a LED driver (LED-OUT, open drain) is turned on every second for 100ms. During the fast charge and pulse charging, the Baseband can control the LED driver through the FLASH-LED pin.

Absolute Maximum Ratings

Operating Temperature (Industrial).....-40°C to +85°C
Storage Temperature.....-55°C to + 150°C
Power Supply Input V_{BAT} and VIN-REGX Pins .....-0.3V to +6.5V
Power Supply Input CHG-IN..... ....-0.3V to +8V
I/O Input (all except to power supply) . -0.3V to V_{MAX}+0.3

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Conditions	Min	Maw	Unit
Operating Temperature		-40	85	°C
Power Supply Input	V_{BAT} and V_{IN}-REGX pins	3.0	4.5	V
Power Supply Input	CHG-IN	4.6	5.5	V

Power Supply Current Consumption

Table 4. Power Supply Current Consumption on V_{BAT} (Fully Charged Backup Battery)

Mode	Condition	Typ	Max	Unit
MODE1 (sleep)	1.2V < V_{BAT} < 2.5V	6.8	8	µA
MODE2 (sleep)	2.5 V <V_{BAT}< 3.2 V	17	28.4	µA
MODE3 (sleep)	3.2 V < V_{BAT} < 4.6 V and Power OFF	17	28.4	µA
MODE4 (standby) (Idle without RX or TX burst)	3.2 V < V_{BAT} < 4.6 V and Power ON	57.5	81.4	µA

Electrical Characteristics

Charger Interface

General conditions unless otherwise noted: $V_{IN} = V_{IN(min)}$ to $V_{IN(max)}$, T_{AMB} = -40°C to +85°C

Table 5. Charger Interface Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GATE-CHG External Transistor						
I_{SINK}	Sink Current		25	30	45	mA
Internal Timer Source (second solution)						
T_{ON}	ON Time	External Transistor is Closed	60	80	100	ms
T	Period		0.9	1	1.1	s
CHG-IN Input Supply						
V_{IN}	Input Voltage		4.6		5.5	V

V-CORE DC to DC

T_{AMB} = -20°C to 85°C, V_{BAT} = 3V to 4.2V unless otherwise specified.

C_{OUT} = 22 µF Tantalum, L_{OUT} = 10 µH.

Table 6. V-CORE(1) DC to DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}(1)	Output Voltage	PWM Mode (BB1 = 1, ECO-MODE = 0)	1.80	1.90	2.0	V
V_{OUT}	Output Voltage	PWM Mode (BB1 = 1, ECO-MODE = 0)	2.45	2.50	2.55	V
I_{OUT}(1)	Output Current	PWM Mode (ECO-MODE = 0)		150	300	mA
I_{OFF}	Standby Current			0.1	1	µA
E_{FF}	Efficiency	I_{OUT} = 10 mA to 200 mA @1.9V		90		%
ΔV_{DCLD}	Static Load Regulation	PWM Mode (10% to 90% of $I_{OUT(MAX)}$		50		mV
ΔV_{TRLD}	transient Load Regulation	PWM Mode (10% to 90% of $I_{OUT(MAX)}$, $T_R = T_F$ = 5µs		50		mV
ΔV_{DCLE}	Static Line Regulation	PWM Mode (10% to 90% of $I_{OUT(MAX)}$, 3.2V to 4.2V)		20		mV
ΔV_{TRLE}	transient Line Regulation	PWM Mode (10% to 90% of $I_{OUT(MAX)}$, 3.2V to 4.2V)		35		mV
V_{OUT}	Output Voltage	LDO Mode (BB1 = 0, ECO-MODE = 1)	1.75	1.85	1.95	V
V_{OUT}	Output Voltage	LDO Mode (BB1 = 1, ECO-MODE = 1)	2.35	2.40	2.45	V
I_{OUT}	Output Current	LDO Mode (ECO-MODE = 1)			10	mA
V_{DROP}	Dropout Voltage	LDO Mode (ECO-MODE = 1)			400	mV

Table 6. V-CORE[1] DC to DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{QC}	Quiescent Current	LDO Mode (ECO-MODE = 1)		11	14	µA
ΔV_{DCLD}	Static Load Regulation	LDO Mode (0 to 10 mA)			50	mV
ΔV_{TRLD}	transient Load Regulation	LDO Mode (0 to 10 mA), $T_R = T_F =$ 5µs			10	mV
ΔV_{DCLE}	Static Line Regulation	LDO Mode (3.2V to 4.2V)			8	mV
ΔV_{TRLE}	transient Line Regulation	LDO Mode (3.2V to 4.2V)			15	mV
PSRR	Ripple Rejection	LDO Mode up to 1 KHz	40	45		dB
ΔV_{LPFP}	Overshoot Voltage	Voltage drop from LDO (LP) to DC-DC(FP)		0	10	mV
ΔV_{FPLP}	Undershoot Voltage	Voltage drop from DC-DC (FP) to LDO (LP)	-15	0		mV

Note: 1. V_{OUT} and I_{OUT} refer to V-CORE.

Table 7. V-CORE DC to DC External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitor Value		17	22	26	µF
C_{ESR}	Output Capacitor ESR				100	mΩ
L_{OUT}	Output Inductor Value		8	10	12	µH
L_{ESR}	Output Inductor ESR	At 100 KHz			1.1	Ω

A-VCC – Analog

T_{AMB} = -20°C to 85°C, V_{BAT} = 3V to 4.2V unless otherwise specified.

Table 8. A-VCC(1)– Analog Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Operating Supply Voltage	All V_{IN}, All T °C, Line, Load	3		5.5	V
V_{OUT}(1)	Output Voltage	BB1 = 0	2.65	2.7	2.75	V
V_{OUT}	Output Voltage	BB1 = 1	2.75	2.80	2.85	V
V_{INT}	Internal Supply Voltage		2.4		2.6	V
I_{OUT}(1)	Output Current			80	130	mA
I_{QC}	Quiescent Current			195	236	µA
DV_{OUT}	Line Regulation	V_{BAT}: 3V to 3.4V, I_{OUT} = 130 mA		3		mV
DV_{PEAK}	Line Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		4		mV
DV_{OUT}	Load Regulation	10% - 90% I_{OUT}, V_{BAT} = 3V		10		mV
		10% - 90%I_{OUT}, V_{BAT} = 5.0V		15		mV
		10% - 90% I_{OUT}, V_{BAT} = 5.5V		15		mV
DV_{PEAK}	Load Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		15		mV
PSRR	Ripple rejection	F = 217Hz – V_{BAT} = 3.6V		70		dB
V_N	Output Noise	BW: 10 Hz to 100 kHz		29		μV_{RMS}
T_R	Rise Time	100% I_{OUT}, 10% - 90% V_{OUT}			50	µs
T_F	Fall Time					
I_{SD}	Shut Down Current				1	µA

Note: 1. V_{OUT} and I_{OUT} refer to A-VCC.

Table 9. A-VCC – Analog External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitor Value		1.98	2.2	2.42	µF
C_{ESR}	Output Capacitor ESR	100 KHz			50	mΩ

V-PAD – PAD Supply

T_{AMB} = -20°C to 85°C, V_{BAT} = 3V to 4.2V unless otherwise specified.

Table 10. V-PAD[1]– PAD Supply Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}[1]	Output Voltage Full Power Mode		2.74	2.8	2.86	V
I_{OUT}[1]	Output Current Full Power Mode			50	80	mA
I_{OUT}	Output Current Low Power Mode				10	mA
I_{QC}	Quiescent Current FP Mode		25	30	36	µA
I_{QC}	Quiescent Current LP Mode		9.75	11.5	13.75	µA
DV_{OUT}	Line Regulation FP Mode	V_{BAT}: 3.4V to 3V, I_{OUT} = 80 mA			1	mV
DV_{PEAK}	Line Regulation Transient FP Mode	V_{BAT}: from 5V to 5.4V and from 3.4V to 3V, I_{OUT} = 80 mA, $T_R = T_F$ = 5 µs			3	mV
DV_{OUT}	Line Regulation LP Mode	V_{BAT}: 3.4V to 3V, I_{OUT} = 5 mA			3	mV
DV_{PEAK}	Line Regulation Transient LP Mode	V_{BAT}: from 5V to 5.4V and from 3.4V to 3V, I_{OUT} = 5 mA, $T_R = T_F$ = 5 µs			4	mV
DV_{OUT}	Load Regulation FP Mode	from 0 to 80mA & from 90% to 10% $I_{OUT(MAX)}$, V_{BAT} = 3.4V			5 (4 at 5.5V)	mV
DV_{PEAK}	Load Regulation Transient FP Mode	from 0 to $I_{OUT(MAX)}$ & from 90% to 10% $I_{OUT(MAX)}$, $T_R = T_F$ = 5 µs, V_{BAT} = 3.4V			23	mV
DV_{OUT}	Load Regulation LP Mode	from 0 to 80mA & from 90% to 10% $I_{OUT(MAX)}$, V_{BAT} = 3.4V			5 (10 at 5.5V)	mV
PSRR	Ripple Rejection	F = 217Hz	40	45		dB
V_N	Output Noise FP mode	BW: 10 Hz to 100 kHz			80	μV_{RMS}
V_N	Output Noise LP Mode	BW: 10 Hz to 100 kHz			300	μV_{RMS}
T_R	Rise Time FP	$I_{OUT} = I_{OUT(MAX)}$	70		130	µs
T_R	Rise Time LP	$I_{OUT} = I_{OUT(MAX)}$	50		170	µs
I_{SD}	Shut Down Current				1	µA
V_{BAT}	Operating Supply Voltage		3		5.5	V
V_{SAUV}	Internal Operating Supply Voltage		2.74	2.8	2.86	V
I_{SC}	Short Circuit Current			50	80	mA

Note: 1. V_{OUT} and I_{OUT} refer to V-PAD.

Table 11. V-PAD – PAD Supply External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitor Value		1.98	2.2	2.42	µF
C_{ESR}	Output Capacitor ESR	100 KHz			50	mΩ

Backup Battery LDO (V-BCK)

T_{AMB} = -20°C to 85°C, V_{BAT} = 3V to 4.2V unless otherwise specified.

Table 12. Backup Battery LDO (V-BCK)[1] Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}[1]	Output Voltage	BB1 = 0	2.4	2.45	2.50	V
V_{OUT}[1]	Output Voltage	BB1 = 1	2.65	2.7	2.75	V
I_{OUT}[1]	Output Current			2	5	mA
V_{DROP}	Dropout Voltage				50	mV
I_{QC}	Quiescent Current		4.8	6.6	9.7	µA
PSRR	Ripple Rejection			40		dB
T_R	Rise Time		110		320	µs

Note: 1. V_{OUT} and I_{OUT} refer to V-BCK.

Table 13. Backup Battery LDO (V-BCK) External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitor Value		1.98	2.2	2.42	µF
C_{ESR}	Output Capacitor ESR	100 KHz			100	mΩ

RTC LDO (V-RTC)

T_{AMB} = -20°C to 85°C, V_{BAT} = 3V to 4.2V unless otherwise specified.

Table 14. RTC LDO (V-RTC)[1] Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}[1]	Output Voltage	BB1 = 0	1.45	1.50	1.55	V
		BB1 = 1 (not used)				
I_{OUT}[1]	Output Current				0.5	mA
V_{DROP}	Dropout Voltage				50	mV
I_{QC}	Quiescent Current		4.8	6.6	9.7	µA
I_{SD}	Shutdown Current			0.1	1	µA
PSRR	Ripple Rejection			40		dB
T_R	Rise time		110		320	µs

Note: 1. V_{OUT} and I_{OUT} refer to V-RTC

Table 15. RTC LDO (V-RTC) External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitor Value		198	220	242	nF
C_{ESR}	Output Capacitor ESR	100 KHz			100	mΩ

RF LDOs (V-RF1 and V-RF2)

Table 16. RF LDOs (V-RF1 and V-RF2)[1] Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Operating Supply Voltage	All V_{IN}, All T°C, Line, Load	3		5.5	V
V_{INT}	Operating Internal Supply Voltage		2.4	2.5	2.6	V
V_{OUT}[1]	Output Voltage		2.74	2.8	2.86	V
I_{OUT}[1]	Output Current			80	130	mA
I_{QC}	Quiescent Current			195	236	µA
DV_{OUT}	Line Regulation	V_{BAT}: 3V to 3.4V, I_{OUT} = 130 mA		3	2	mV
DV_{PEAK}	Line Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		4	2.85	mV
DV_{OUT}	Load Regulation	10% - 90% I_{OUT}, V_{BAT} = 3V		10	1	mV
		10% - 90% I_{OUT}, V_{BAT} = 5.0V		15	1	mV
		10% - 90% I_{OUT}, V_{BAT} = 5.5V		15	1	mV
DV_{PEAK}	Load Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		1.2	2.4	mV
PSRR	Ripple Rejection	F=217Hz – V_{BAT} = 3.6V	70	73		dB
V_N	Output Noise	BW: 10 Hz to 100 kHz		29	37	μV_{RMS}
T_R	Rise Time	100% I_{OUT}, 10% - 90% V_{OUT}			50	µs
I_{SD}	Shut Down Current				1	µA

Note: 1. V_{OUT} and I_{OUT} refer to V-RF1/V-RF2.

Table 17. RF LDOs (V-RF1 and V-RF2) External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitor Value		1.98	2.2	2.42	µF
C_{ESR}	Output Capacitor ESR	100 KHz			50	mΩ

Buzzer Open Drain

General Conditions (unless otherwise noted): $V_{IN} = V_{IN(min)}$ to $V_{IN(max)}$, T_A = -40°C to +85°C

Table 18. Buzzer Open Drain Electrical Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}(1)	Low Output Voltage	I_{OL} = 100 mA			0.4	V
I_{OL}(1)	Low Output Current				100	mA
T_{ON}(1)	Turn-on Time				10	µs
T_{OFF}(1)	Turn-off Time				10	µs

Note: 1. V_{OL}, I_{OL}, I_{OH}, T_{ON} and T_{OFF} refer to Buz-Out.

Vibrator

General Conditions (unless otherwise noted): $V_{IN} = V_{IN(min)}$ to $V_{IN(max)}$, T_A = -40°C to +85°C, C_{OUT} = 2.2µF to Y5V.

Table 19. Vibrator Electrical Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}(1)	Output Voltage		2.74	2.80	2.86	V
I_{OUT}(1)	Output Current			100		mA
V_{DROP}	Dropout Voltage				280	mV
I_{QC}	Quiescent Current			195	236	µA

Note: 1. V_{OUT} and I_{OUT} refer to V-VIB.

Digital Pin Parameters

Conditions: T_{AMB} = -20°C to 85°C, V_{BAT} = 3V to 4.2V unless otherwise specified

Table 20. Digital Pins.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		DC-ON				
V_{OL}	Output Low Voltage			GND		
V_{OH}	Output High Voltage			V-PAD		
I_{OH}	Output Current			1		mA
I_{OL}	Output Current			1		mA
I_{OH}	Leakage Current				1	µA
		ON/OFF				
V_{IH}	High input voltage	$I_{IH(Max)}$ = 20 µA	0.7x V_{BAT}	V_{BAT}		V
V_{IL}	Low input voltage	$I_{IL(Max)}$ = 20 µA		GND	0.3 x V_{BAT}	V
I_{IL}	Low input current				0.1	µA
I_{IH}	High input current				0.1	µA
		UP-ON/OFF				
V_{IH}	High input voltage	$I_{IH(Max)}$ = 20 µA	0.7x V_{RTC}	V-BCK		V
V_{IL}	Low input voltage	$I_{IL(Max)}$ = 20 µA		GND	0.3x V_{RTC}	V
I_{IL}	Low input current				0.1	µA
I_{IH}	High input current				0.1	µA
		ECO-MODE				
V_{IH}	High input voltage		1.5	V-PAD		V
V_{IL}	Low input voltage	$I_{IL(Max)}$ = 20 µA		GND	0.6	V
I_{IL}	Low input current				0.1	µA
I_{IH}	High input current				0.1	µA
		RES-B[1]				
V_{OL}	Output Low Voltage	I_{OL}=1 mA and V_{PAD} = $V_{PAD(MAX)}$			0.2	V
I_{OH}	Output Leakage Current			0.1	1	µA
I_{OL}	Output Current				1	mA
T_{RESET}	Output Delay Time		20		100	ms
I_{SS}	Supply Current			4	5	µA
I_{OFF}	Standby Current			0.1	1	µA
		CHG				
V_{IL}	Input Low Voltage			GND	0.6	V
V_{IH}	Input High Voltage		1.5	V-PAD		V
I_{IL}	Input Low Current				0.1	µA
I_{IH}	Input High Current				0.1	µA
R_{DOWN}	Pull-down resistance	CHG pin	1	1.5	1.8	MΩ

Table 20. Digital Pins. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FLASH-LED & LED-OUT Pins						
T_{ON}	ON Time	External Transistor is closed	60	80	100	ms
T	Period		0.9	1	1.1	s
V_{OL}	Low Output Voltage	I_{OUT} = 5 mA			0.4	V
I_{OL}	Low Output Current				5	mA
I_{OH}	Leakage Current				1	µA
V_{IL}	Low Input Voltage				0.4	V
V_{IH}	High Input Voltage		1.5			V
I_{IL}	Input Low Current				0.1	µA
I_{IH}	Input High Current				0.1	µA
R_{DOWN}	Pull-down resistance	FLASH-LED pin	1	1.5	1.8	MΩ
EN-RF1, EN-RF2						
V_{IH}	High input voltage	IIH(Max) = 20 µA	0.7 x V_{CORE}	V-PAD		V
V_{IL}	Low input voltage	IIL(Max) = 20 µA		GND	0.3 x V_{CORE}	V
I_{IL}	Low input current				0.1	µA
I_{IH}	High input current				0.1	µA
R_{DOWN}	Pull-down resistance		1	1.5	1.8	MΩ
BUZ-IN						
V_{IH}	High Input Voltage	$I_{IH(Max)}$ = 20 µA	1.5	V-PAD		V
V_{IL}	Low Input Voltage	$I_{IL(Max)}$ = 20 µA		GND	0.6	V
I_{IH}	High input current	BUZ-IN pin			0.1	µA
I_{IL}	Low input current	BUZ-IN pin			0.1	µA
R_{DOWN}	Pull-down resistance	BUZ-IN pin	1	1.5	1.8	MΩ
EN_VIB						
V_{IH}	High input voltage	$I_{IH(Max)}$ = 20 µA (EN-VIB)	1.5	V-PAD		V
V_{IL}	Low input voltage	$I_{IL(Max)}$ = 20 µA (EN-VIB)		GND	0.6	V
I_{IL}	Low input current	(EN-VIB)			0.1	µA
I_{IH}	High input current	(EN-VIB)			0.1	µA
R_{DOWN}	Pull-down resistance	EN-VIB pin	1	1.5	1.8	MΩ

Note: 1. V_{IN} = 1.2V to $V_{PAD(MAX)}$. The reset generator has an open collector output. It is enabled only when V_{CORE} is active.

SIM Interface

Conditions are DV_{CC} = 1.8V or 2.8V, t_A = -40°C to +85°C, C_{DVCC} = 100 nF, CSIM-V_{CC} = 100 nF

Table 21. SIM Interface Electrical Characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
DV_{CC}	Digital Supply Voltage	Mandatory	1.65		3.0	V
I_{DVCC}	DV_{CC} Operating Current	CLK_IN at 3.25 MHz		2.5	10	µA
$V_{SIM-VCC}$	SIM-V_{CC} Output Voltage	$I_{SIM-VCC}$ < 10 mA SIM-EN = DV_{CC} SIM-1V8/2V8 = DV_{CC}	1.71	1.8	1.89	V
$V_{SIM-VCC}$	SIM-V_{CC} Output Voltage	$I_{SIM-VCC}$ < 10mA SIM-EN = DV_{CC} SIM-1V8/2V8 = GND	2.74	2.8	2.86	V
$I_{SIM-VCC}$	SIM-V_{CC} Operating Current	$I_{SIM-VCC}$ -> SIM card = 0 $I_{SIM-CLK}$ = 3.25 MHz		25	100	µA
I_{SHDN}	Total Shutdown Current	$I_{SIM-VCC}$ + I_{DVCC} with SIM-EN = GND		0.1	1	µA
I_{QC}	SIM_LDO Quiescent Current	Low-power Mode		8	9.5	µA
I_{QC}	SIM_LDO Quiescent Current	Full-power Mode			60	µA
I_{OUT}	Output Current			10		mA
I_{SC}	Short Circuit Current				40	mA
Digital Interface (RESET-IN, CLOCK-IN, DATA-IO)						
I_{IH}, I_{IL}	Input current	CLK-IN, RST-IN, SIM-EN, SIM-1V8/2V8	-0.1		0.1	µA
I_{IH}	Input current	DATA-IO	-20		20	µA
I_{IL}	Input current	DATA-IO			1	mA
V_{IH}	High input voltage	CLK-IN, RST-IN, DATA-IO, SIM-EN, SIM-1V8/2V8	0.7x DV_{CC}			V
V_{IL}	Low input voltage	CLK-IN, RST-IN, DATA-IO, SIM-EN, SIM-1V8/2V8			0.3x DV_{CC}	V
V_{OH}	High output voltage	DATA-IO, source current = 20 µA	0.7x DV_{CC}			V
V_{OH}	High output voltage	DATA-IO, source current = 5 µA	0.8x DV_{CC}			V
V_{OL}	Low output voltage	DATA-IO, sink current = 200 µA			0.4	V
$R_{DATA-IO}$	Pull-up resistance	Between DATA-IO and DV_{CC}	13	20	28	kΩ
T_R T_F	Rise and fall time	DATA-IO loaded with 30 pF		1.3	2	µs

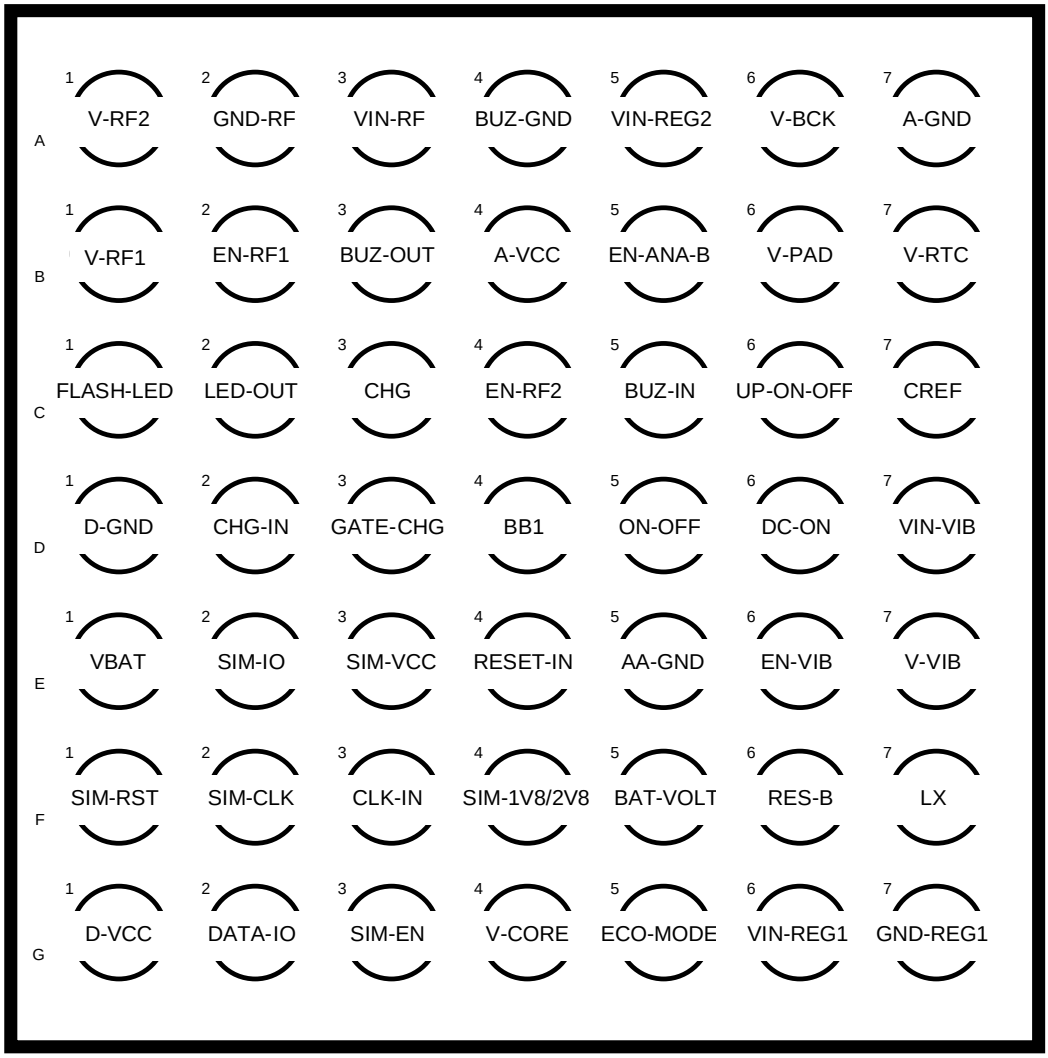
Table 21. SIM Interface Electrical Characteristics. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SIM Interface (SIM-RST, SIM-CLK, SIM-DATA)						
V_{IH}	High input voltage	SIM-DATA with $I_{IH(Max)}$ = ± 20 µA (1)	0.7xSV_{CC}			V
V_{IL}	Low input voltage	SIM-DATA with $I_{IL(Max)}$ = 1 mA			0.3	V
V_{OH}	High output voltage	SIM-DATA, source current = 20 µA (1)	0.8xSV_{CC}			V
V_{OL}	Low output voltage	SIM-DATA, sink current = 200 µA			0.4	V
V_{OH}	High output voltage	SIM-RST, SIM-CLK with source current = 20µA (1)	0.9xSV_{CC}			V
V_{OL}	Low output voltage	SIM-RST, SIM-CLK with sink current = 200 µA			0.4	V
I_{IH}	High input current	SIM-DATA			20	µA
I_{IL}	Low input current	SIM-DATA			1	mA
V_{SD}	Shutdown output voltage	SIM-DATA, SIM-CLK, SIM-RST, SIM-V_{CC} with SIM-EN = GND, with sink current = 200 µA			0.4	V
$R_{SIM-DATA}$	Pull-up resistance	Between SIM-DATA and SIM-V_{CC}	6.5	10	14	kΩ
T_R, T_F	Rise and fall time	SIM-DATA, SIM-RST loaded with 50 pF			1	µs
T_R, T_F	Rise and fall time	SIM-CLK loaded with 50 pF			18	ns
$F_{SIM-CLK}$	Maximum frequency	SIM-CLK loaded with 50 pF			5	MHz

Note: 1. SIM-V_{CC} = SV_{CC}

Package Outline (Top View)

Figure 3. Forty-nine Ball FBGA Package (Top VIew)



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