Features

- **Programmable Resolution, Active CMOS Imager for Video and Still Operation**
- **PC Plug-and-Play Capable in USB Mode**
- **Full 16-bit Digital Interface for Simple, Fast Transfer in Parallel-port Mode**
- **Low, Fixed-pattern Noise**
- **Triple 10-bit ADCs and Column-based CDS for High-quality Display**
- **High Fill Factor and Sensitivity without Microlens Distortions**
- **Available in Color or Black-and-White Versions**
- **Integrated AVR® 8-bit Advanced RISC Microcontroller for System Control**
- **Easy Register-based Programming Modes**
- **Region-of-Interest Image Scan Control for Digital Zoom and Metering**
- **On-board Color Offset and Gain Control**
- **On-board Gamma Lookup Table Available**
- **Full Power Control and Low-power Viewfinder Mode**
- **Master or Slave Mode Operation**

Description

The Atmel AT76C402 is a complete image capture and processing system that has been designed to give quality images using a standard interface with simple operation. This highly-integrated solution provides a product with reduced system cost and rapid time-to-market.

The AT76C402 has two interface modes: USB and parallel port. Both use the device as a slave. This datasheet covers USB mode only. See the “AT76C402 – Parallel Port Mode” datasheet (Literature Number 1372) for parallel port mode pinouts and operation.

The image capture core is a pixel array of 300 x 300 rectangular active pixels with a high physical fill factor of 43% (without micro lenses). A vertical stripe RGB pastel color filter is used with individual column-correlated double sampling (CDS) correction circuitry to produce an exceptionally low level of fixed-pattern image noise (FPN). Individual color gain and offset controls followed by a triple 10-bit analog-to-digital converter further assure an even color response in the digitized images.

Region-of-Interest mode additionally allows the user to define on a frame-by-frame basis the area of the imager to be read, enabling easy digital zoom or complex multi-spot metering routines utilizing an external host.

The data path from the imager is through the gain/offset and ADC block and the lookup table into a 1K x 8 FIFO. The value written into the FIFO is truncated to eight bits. The data is then read by the AVR and passed either via the USB ping-pong FIFO to a USB pad or via a custom 16-bit parallel port.

Timing and control is handled by an on-chip AVR 8-bit microcontroller and timing generator. The AVR executes firmware uploaded into an on-chip 4K x 16 SRAM via a Serial Peripheral Interface (SPI) during device power-up. The SPI is designed to work with off-chip EEPROM or Flash memory. The AVR uses an on-chip 2K x 8 SRAM scratch pad for data operations.

In master mode the AVR controller still boots from an external EEPROM/Flash, but writes the image data back through the SPI into the EEPROM/Flash. The AVR communicates control via the GPIO port which is connected externally. This provides a lower component cost solution for applications which are not transfer time dependent. Master mode is not described further in this datasheet.

USB and Parallel Port Mode Integrated CMOS Imager

AT76C402 – USB Mode

Preliminary

Rev. 1360A–06/00

Pin Configuration

Figure 1. AT76C402 Die View – USB Mode

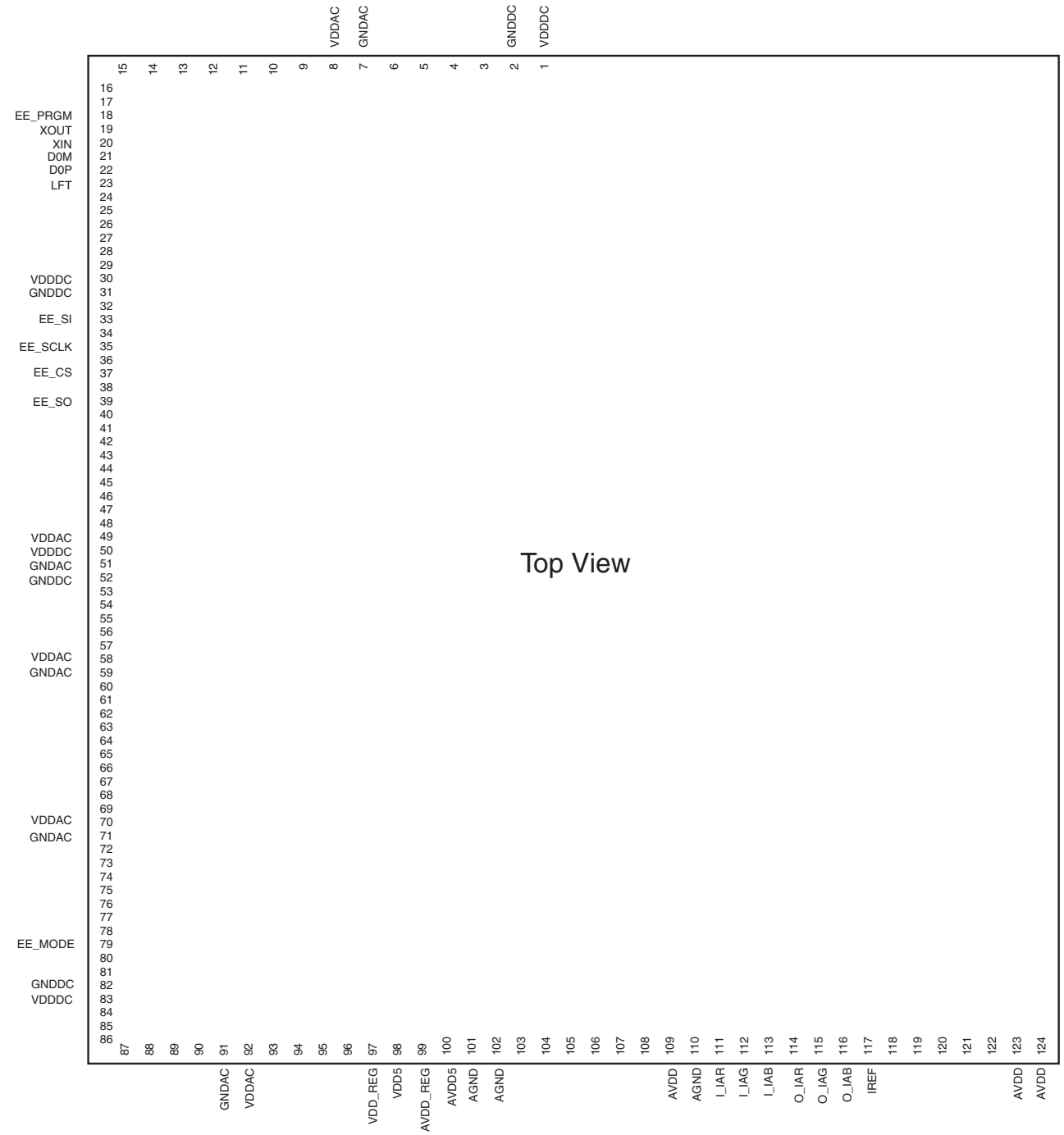


Table 1. USB Mode Pin and Pad Description

Pin Number	Pad Names	Type	Description
1, 30, 50, 83	VDDDC	Digital Power	3.3V Digital DC Power – Core
2, 31, 52, 82	GNDDC	Digital Ground	0.0V Digital DC Ground – Core
7, 51, 59, 71, 91	GNDAC	Digital Ground	0.0V Digital AC Ground – Pad Ring
8, 49, 58, 70, 92	VDDAC	Digital Power	3.3V Digital AC Power – Pad Ring
18	EE_PRGM	Digital Input	Mode Select for Flash or EEPROM Programming
19	XOUT	Analog Out	16 MHz Crystal
20	XIN	Analog Input	16 MHz Crystal
21	D0M	Data -	USB Differential Pad
22	D0P	Data +	USB Differential Pad
23	LFT	Analog Input	PLL Low-pass Filter Terminal
33	EE_SI	Tri-state Digital Output	Serial Peripheral Interface Signal Output
35	EE_SCLK	Tri-State Digital Output	Serial Peripheral Interface Clock Output
37	EE_CS	Tri-state Digital Output	Serial Peripheral Interface Chip Select Output
39	EE_SO	Tri-state Digital Input	Serial Peripheral Interface Signal Input
79	EE_MODE	Digital Input	Select for external EEPROM or Flash
97	VDD_REG		Digital Regulator 3.3V Output for De-coupling
98	VDD5		Digital Regulator 5V Input
99	AVDD_REG		Analog Regulator 3.3V Output for De-coupling
100	AVDD5	Analog Ground	Analog Regulator 5V Input
101, 102, 110	AGND	Analog Ground	Ground Rail for Analog and Pixel Array
109, 123, 124	AVDD	Analog Power	Supply Rail for Analog and Pixel Array
111	I_IAR	Current Input	Red Channel from Gamma
112	I_IAG	Current Input	Green Channel from Gamma
113	I_IAB	Current Input	Blue Channel from Gamma
114	O_IAR	Current Output	Red Channel to Gamma
115	O_IAG	Current Output	Green Channel to Gamma
116	O_IAB	Current Output	Blue Channel to Gamma
117	IREF	Analog In	Current Reference for On-chip Bias Generators

Note: For parallel port pinout, refer to Parallel Port Mode datasheet (Lit. No. 1372).

Block Diagram

Figure 2. Block Diagram of AT76C402

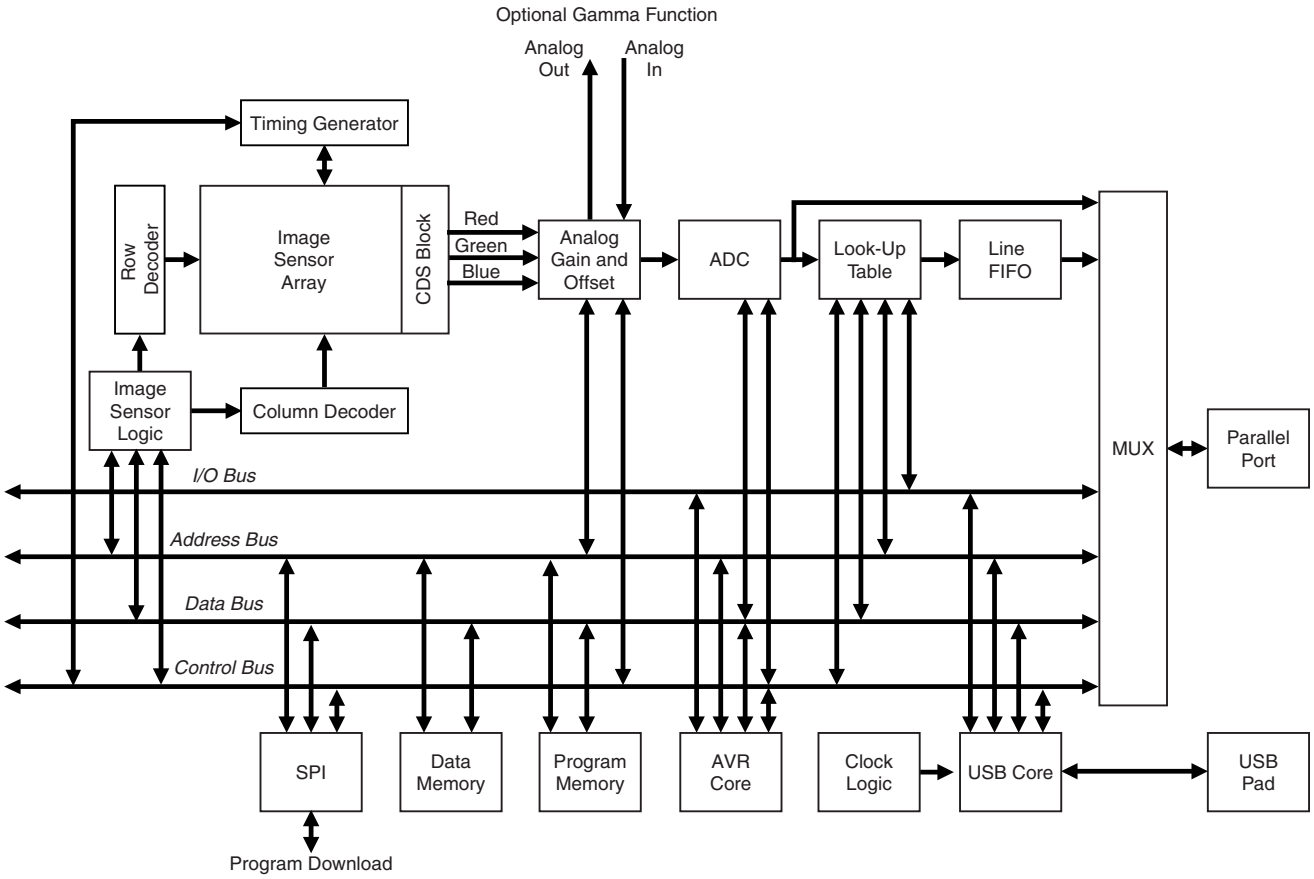


Table 2. Physical and Electrical Parameters

Parameter	Measurement	Units
Resolution	300 x 300	Pixels
Pixel Size	12 (h) x 6 (w)	µm
Image Area	3.6 x 1.8	mm
Fill Factor	43	%
Max Col FPN	0.2	%
Dynamic Range	60	dB
Power Supply	3.3V ± 10% (Parallel Port Mode)	V
Power Consumption	< 100	mW
Readout Rate	3	Mpixels/second
Sensitivity(saturation)	20	UA/lux-sec
Conversion Gain	1.05	nA/e-
Dark Current	0.3 @ Room Temperature	nA/cm^2

Figure 3. Board System Architecture – USB Mode (AT76C402 with External Components)

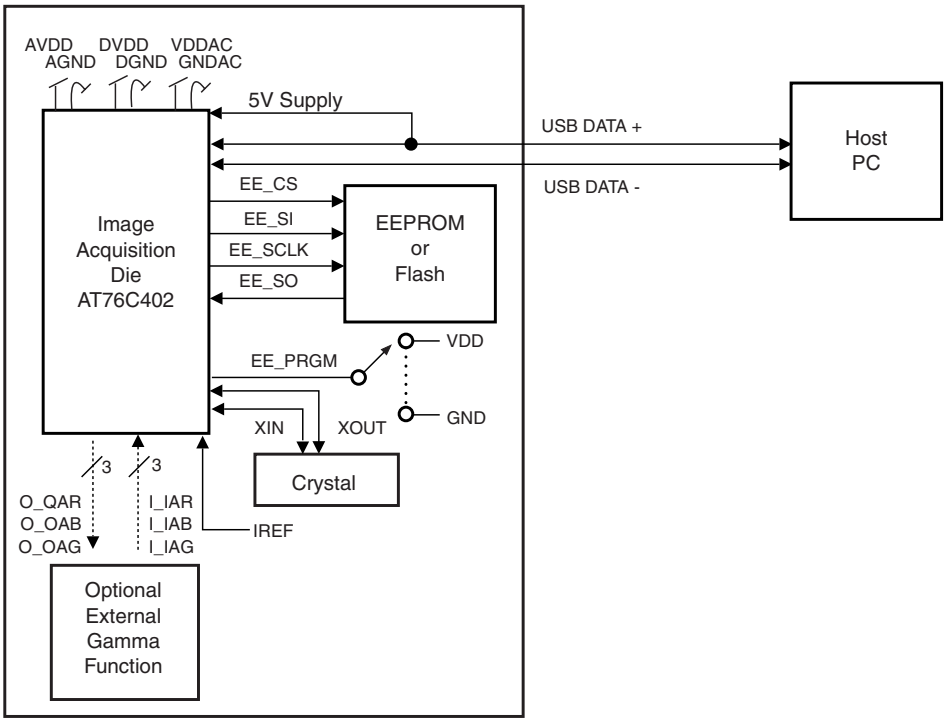
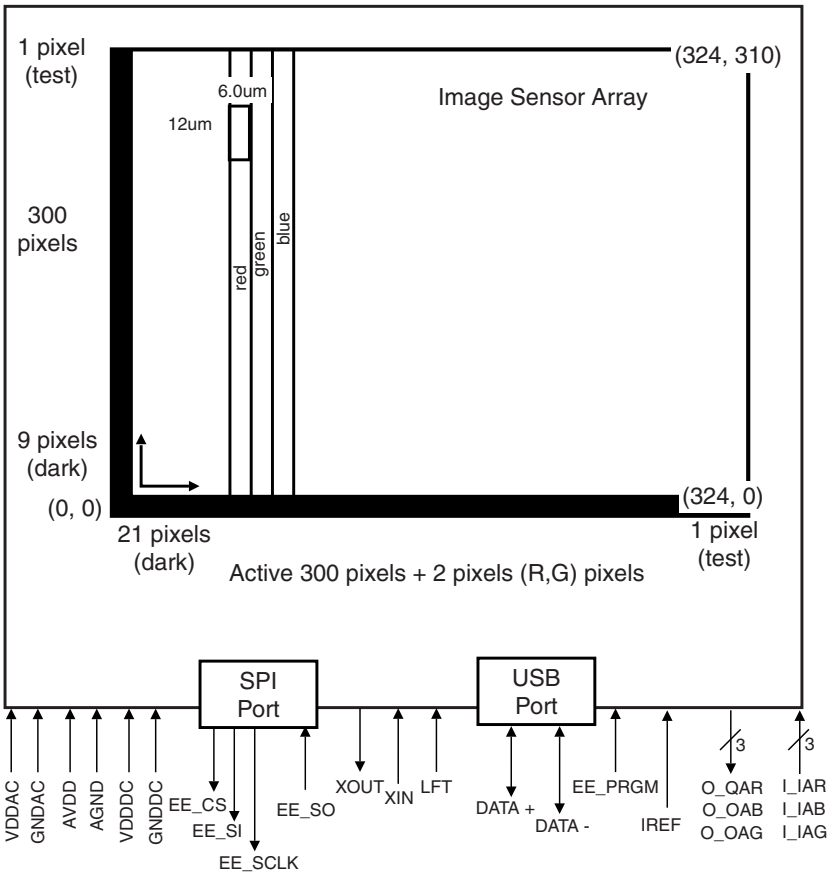


Image Camera System

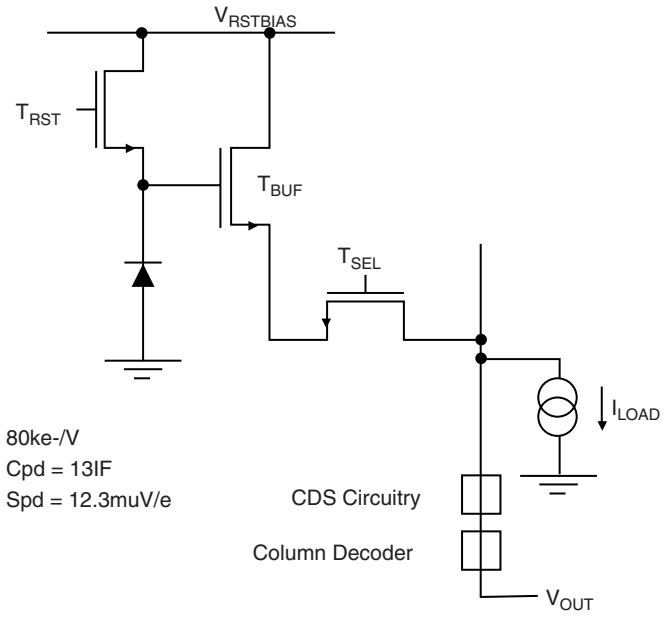


Architectural Overview

Active Pixel Array

The pixel array used is a three-transistor voltage mode photodiode design. To initialize the pixel, the reset transistor T_{RST} (which is common with others across each row) is turned on, and the photodiode active area charges up to the $V_{RSTBIAS}$ line.

Figure 4. Pixel Transistor Schematic



When T_{RST} is turned off to start the integration, the photodiode begins to discharge and theresulting voltage level is buffered by T_{BUF} through to the row select transistor T_{SEL}.

After integration is complete, transistor T_{SEL} (also common with other T_{SEL} across the row) is turned on presenting the pixel voltage to the column readout bus.

Note that the photodiode will continue to integrate if still illuminated or until it is reset again by activating T_{RST} in preparation for another exposure period.

See Figure 4, Figure 5, Figure 6 and Figure 7.

Figure 5. Pixel Select and Reset Timing

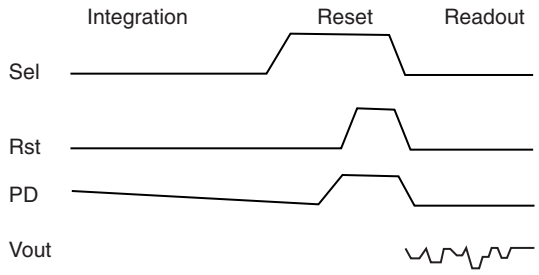


Figure 6. Pixel Cross-section

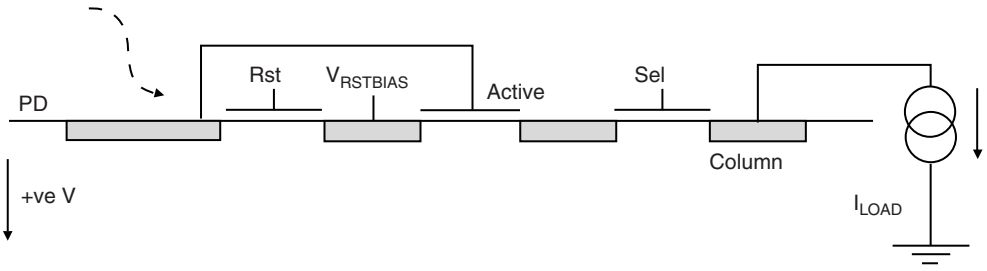
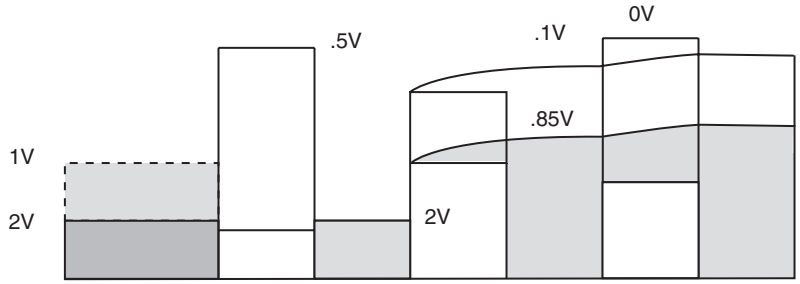


Figure 7. Pixel Charge Potential Plot



Correlated Double Sampling

A CDS block is placed at the bottom of every pixel column signal line. Using the image timing generator, the photodiode voltages from all of the pixels in a row are applied in parallel to their CDS blocks, buffered, clamped and converted to a current. This is then stored in the first of two current memories in each block.

Column-correlated double sampling is then performed by turning on T_{RST}, resetting the pixel and storing the reset voltage after buffering and conversion in a second current memory.

Finally, the difference in the two values, reset and signal-reset, is passed out of the CDS block (still as a current value) onto one of the three color busses (red, green and blue for color; left, middle and right for black-and-white). These values are passed onto the gain/offset and ADC block which can be programmed to provide gain and offset adjustment to the value.

Gain and Offset

Individual gain and offset of the output of the CDS busses are performed using six current mode amplifiers under the control of DACs driven by the contents of six registers in the AVR I/O space. A seventh register (GAIN_MSTR), through a single DAC, is used to control three additional amplifiers ganged together to perform global gain. The red, green and blue channel output is defined by the equation:

$$I_{out} = 2G_{gain} \times F_{gain} \times I_{in} - Offset$$

where

- G_{gain} is the global gain
- F_{gain} is the fine gain per channel
- Offset is the offset correction per channel

Analog Access Port

After gain and offset amplification the three color busses are made available (via register control) through ports O_OAR, O_OAG and O_OAB as current signals at a constant voltage for external processing as required, for example a gamma function. These signals are reinserted into ports I_IAR, I_IAG and I_IAB. See full pinout description for location if required.

It is not necessary (or desirable) to link the ports externally if this feature is not used as the signal can be bridged internally under the control of the ANA_CTL register in the AVR I/O space.

10-bit Analog-to-Digital Converter

Following the internal or external loopback, the three-color bus current signals are passed to three 10-bit pipelined analog-to-digital converters which require eight master clock periods for each conversion.

A digital multiplexer, controlled from the image timing generator, brings the digital image data out via a single 10-bit width data bus.

Bias Generator

There are on-chip voltage and current bias generators which provide all the necessary bias for the imager and analog blocks (Gain/Offset and ADC block). An external resistor connected to IREF provides a stable reference current value (e.g. 10K Ohm across 1.25V provided gives 125 µA for IREF). The block can be powered down to conserve power. For more details, refer to the section “Power Control” on page 13.

Lookup Table

The 10-bit data is compressed to 8-bits via either user-selectable linear truncation or the choice of two non-linear transfer functions stored in an on-chip lookup table (LUT). The tables used in the lookup table are hard-wired and register-selectable. The linear truncation option is done on the eight most significant bits. The two non-linear options are gamma functions:

Lookup Table A is an intermediate lookup table defined as:

$$y = 72.85 \cdot \log_2(\gamma) + 255$$

$$\gamma = n\left(\frac{1 - 0.0884}{1023}\right) + 0.0884$$

where

- n is a 10-bit input value and
- y is an 8-bit output value

Lookup Table B is a logarithmic lookup table defined as:

$$y = 25.5 \cdot \log_2(n + 1)$$

where

- n is a 10-bit input value and
- y is an 8-bit output value

The lookup table can be bypassed if desired and the full 10-bit data can be brought out through the parallel port in parallel port mode. Refer to the “AT76C402 Parallel Port Mode” datasheet, Literature Number 1372.

Row/Column Timing

The imager scanning circuits, the row and column decoders, are under the control of the timing generator. In turn, the AVR controls the generator function using the values stored in the AVR I/O space register. These determine the region of interest to be viewed, the start and end locations and the exposure mode and exposure time. The values in these registers are uploaded into the device during power up.

The imager scans from left to right and bottom to top; both still and video modes are supported.

AVR Microcontroller

This is a low-power 8-bit RISC microprocessor based on a Harvard architecture. It supports internal and external interrupts, sleep control and a rich 8-bit instruction set with 32 general-purpose working registers. All the registers are directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The architecture supports high-level languages as well as extremely dense assembler programs

USB Controller

The USB controller consists of a serial-interface engine (SIE), a serial bus controller and a system interface. The SIE performs the clock/data separation, NRZI encoding and decoding, bit insertion and deletion, CRC generation and checking and the serial-parallel data conversion. The serial bus controller consists of a protocol engine and a USB device with a control end point and data end points. The serial bus controller manages the device address, monitors the status of the transactions, manages the FIFO and communication to the microcontroller through a set of status and control registers. The system interface connects the serial bus controller to the microcontroller.

The controller is a full-speed, 12 MBs transfer core designed to work with the AVR microcontroller. It allows the USB host to configure the device and receive serial communication to and from the device.

The controller supports three endpoints. The first, EB0, is the command 8-byte endpoint. The second, EB1, is the bulk transfer endpoint with a 64-byte ping-pong data FIFO. This configuration allows for back-to-back data transfer and retransfer of packet data if required. The third, EB2, is the user-defined interrupt 2-byte endpoint. The USB registers are mapped explicitly to addresses in the SRAM memory space. Communication with the controller is based on the Universal Serial Bus Specification Version 1.0.

Line FIFO

The data from the imager via the ADC can be wrtten into the FIFO based on the AVR I/O space register assigned to this function. The FIFO enables the user to fill it with more than two lines of information, the controller can then start to read this data out and, while it does this, the FIFO is filled with the next line of data. This feature increases data throughput.

Serial Peripheral Interface

Code from either an external EEPROM or Flash is downloaded into the device on power-up using a 4-wire serial peripheral interface (SPI). The selection between downloading from either memory is determined by the status of the EE_MODE pin, 0 for EEPROM, 1 for Flash. To program the device, EE_PRGM must be toggled to 0 to load the code and switched back to 1 after programming for normal operation.

Functional Description

There is an additional option of writing image values or parameters to external Flash. See “External Memory Interface” on page 18 for timing diagrams.

Scan Control

The AT76C402 integrates all the functions required to capture, digitize and process an image. To allow maximum flexibility, the individual functions are register-programmable and are accessible via the AVR I/O space. The user can therefore control precisely the various functional blocks to accomplish a customized operation.

The image is read from bottom to top, left to right. A row decoder and counter controls the row read-out, and a column decoder and counter control the column read-out. The row decodes a maximum of 310 and the column decoder a maximum of 108 (108 x 3 triplets = 324).

The desired region of interest is defined using registers residing in the AVR I/O space. These include the registers RST_START_ROW, SEL_START_ROW, END_ROW, START_COL and END_COL. See “AVR I/O Space Register Map” on page 14 for names and addresses.

Internal Image Scan Modes

Single Still Frame Mode

Still frame operation is achieved using an electronic half shutter and is usually augmented by an external mechanical shutter for high-speed exposures.

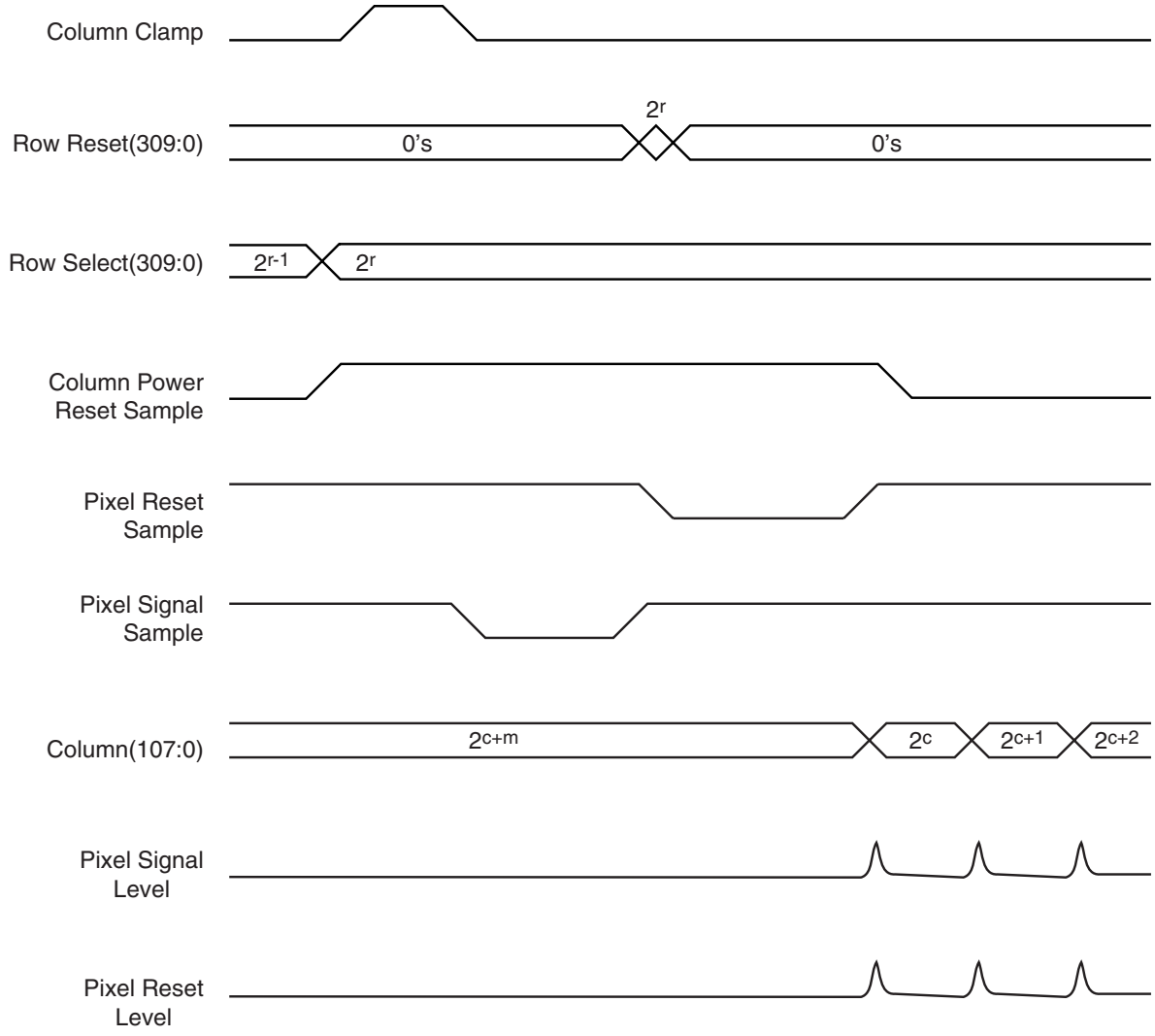
Setting bit 2 = 0 of the IMAGE_CAPTURE_MODE register in the AVR I/O space selects still frame mode. The expo-

sure time is determined under external control and can be as short or as long as the user requires.

After the exposure period (and possibly after the external shutter has been closed), the image is read out on a line-by-line basis starting with the lower left hand corner of the area defined in the SEL_START_ROW and START_COL registers until it reaches the values in END_ROW and END_COL. The data is read out row-by-row at the rate as determined by the Line FIFO. The RST_START_ROW registers are not used in this mode. The initialization and readout sequence is controlled under firmware.

Although a mechanical shutter may be used to prevent direct exposure after reading of the image has begun, the pixels will continue to integrate dark current. The readout period, once the shutter is closed, should therefore be kept as short as possible in relation to the exposure time to avoid a brightness gradient down the picture. If this is not possible due to system or transmission channel constraints then a simple algorithm can be implemented to correct for it.

Figure 8. Timing Diagram Showing Internal CDS Operation for Still Frame Mode



Moving Blade Mode

For continuous image acquisition, exposure is controlled using a moving blade electronic shutter the width of which is written to the RST_START_ROW registers defined in the AVR I/O space before a frame is exposed.

Figure 9. Moving Blade Shutter

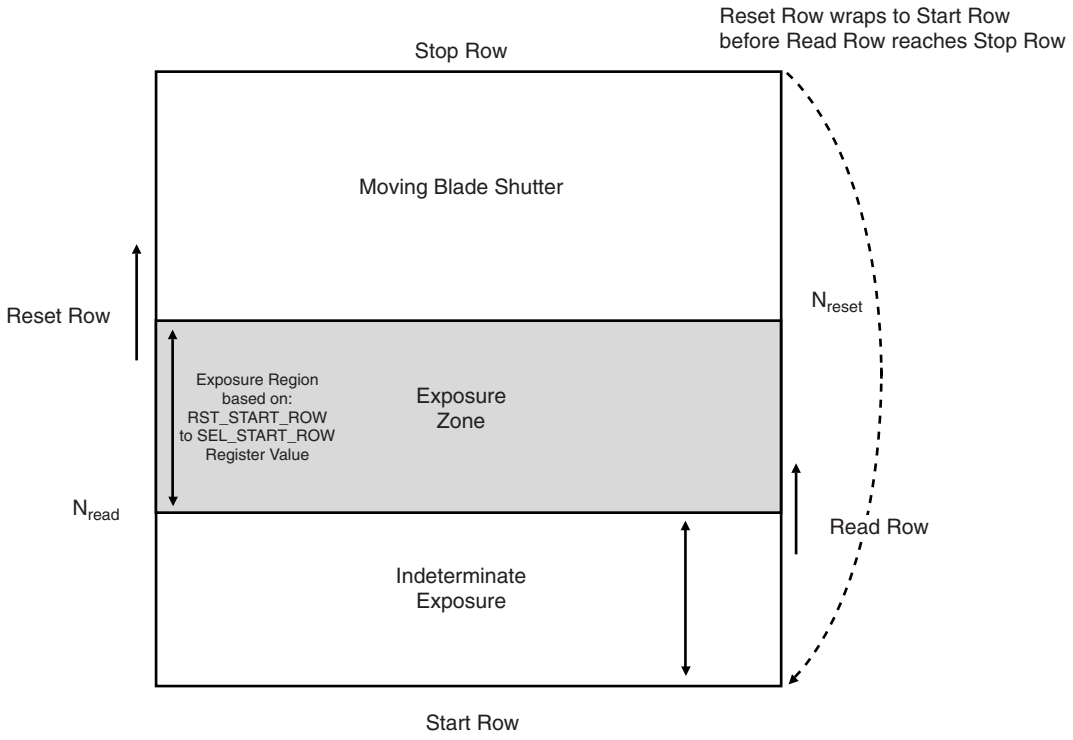
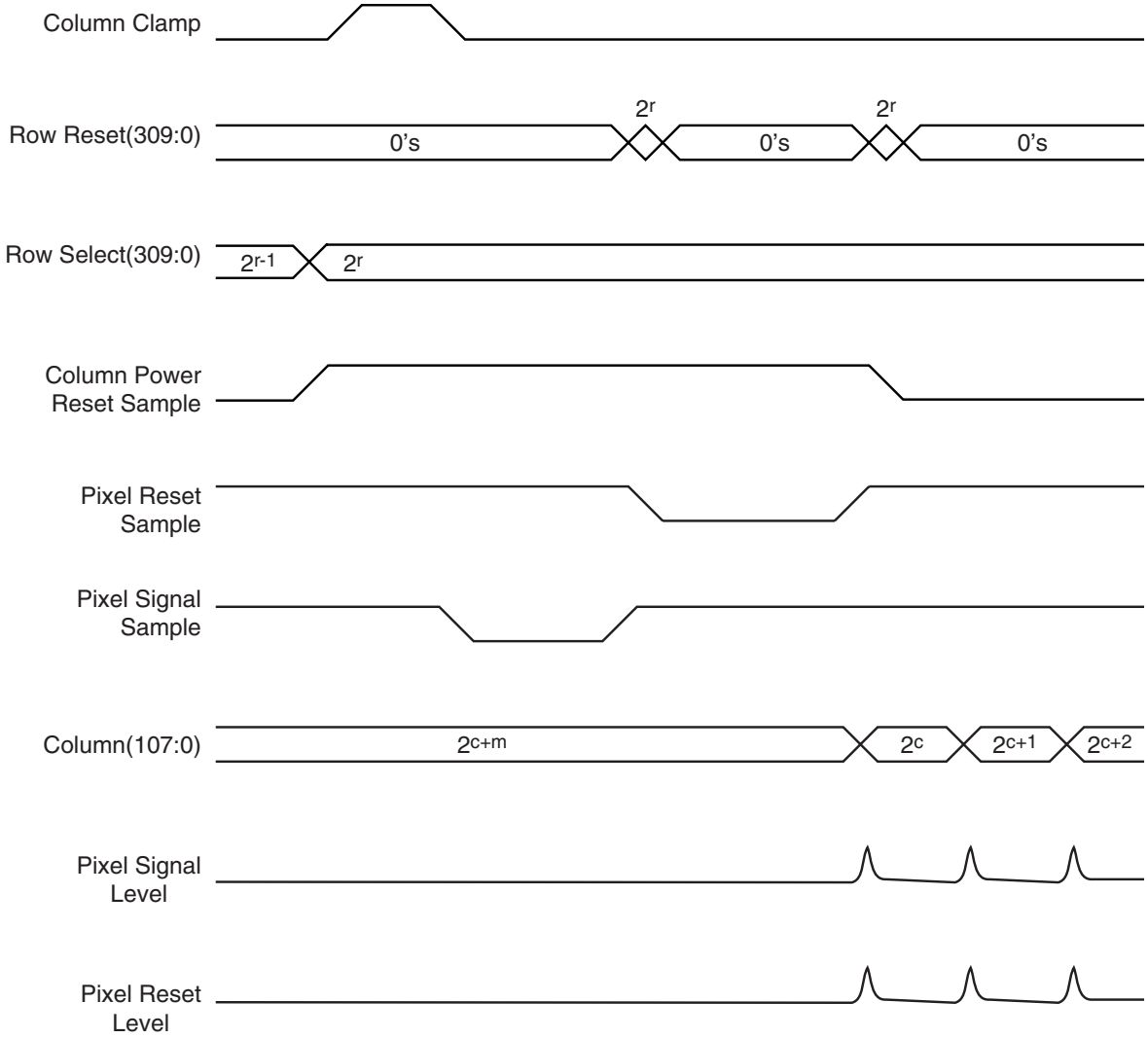


Figure 10. Timing Diagram Showing Internal CDS Operation for Moving Blade Mode



Again, a region of interest can be defined using the start and end values for the row and column as defined in the AVR I/O space. The reset register for the row in this case needs to be defined and the value between this and the select row register is the exposure line. The exposure can be calculated as:

$$\text{Exposure (ms)} = \text{Row Blanking Period} + \text{Row Read Period} \times (\text{RST\_START\_ROW} - \text{SEL\_START\_ROW})$$

For the first frame valid data is not available until the programmed exposure period for the first line has been reached. During this period, the last n (where n is the number of lines of the exposure) lines of the imager are read out followed by the first frame sync. As these lines will have been reset at an indeterminate time, the data obtained will be random. To establish the true start of the image, the user should flush the first frame. Subsequent frames of image will contain full valid data as the reset and read points will smoothly wrap around the imager.

After the latency determined by the exposure programmed into the register, real image data is available at the output.

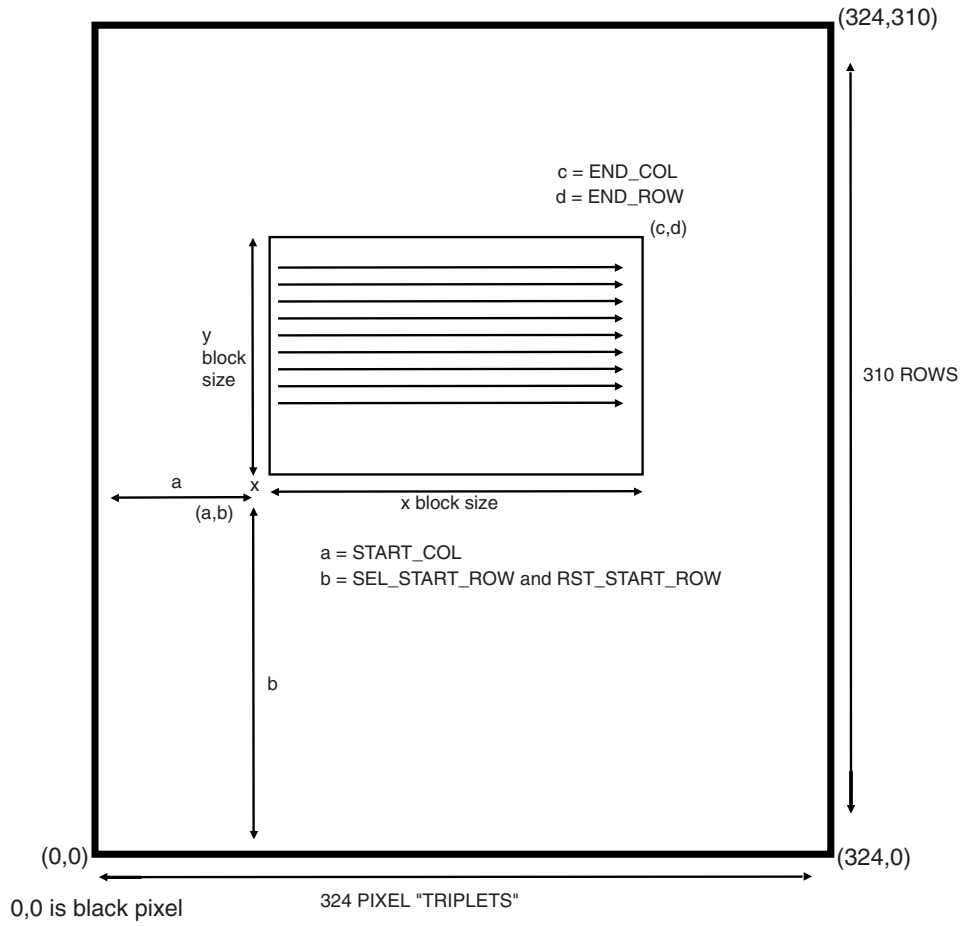
Region of Interest

It is possible to define the area of the pixel array the imager scans by writing to START_COL, RST_START_ROW, SEL_START_ROW, END_ROW and END_COL registers. As seen in Figure 12, the lower left-hand corner is used as the start address. Data is written into the appropriate registers as the number of RGB triplets from the left hand edge and the number of pixel rows from the bottom. For this calculation, all rows are taken into account.

The end position of the scan is set by the appropriate registers, writing it as the number of RGB triplets horizontally and the number of rows vertically. If none is defined, then default values are used. The registers are defined in the AVR I/O space.

Pixels that are not read will not be reset other than through the user strobe Frame Reset (in still mode). It is not necessary however as the unread pixels will simply integrate up to saturation and no blooming effect will be visible.

Figure 11. Region of Interest – Calculation



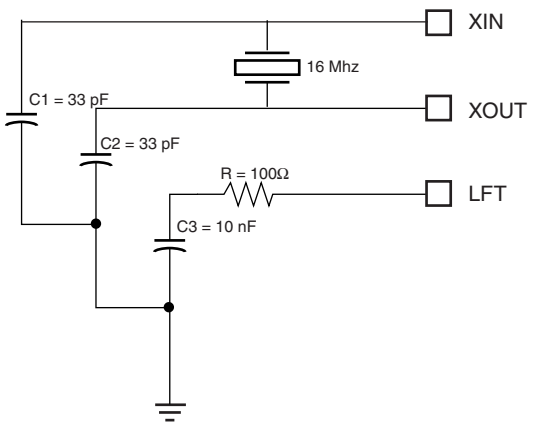
Clocks

In functional mode the chip requires three external clock pin connections. XIN and XOUT connect the 16 MHz on-chip oscillator to an external crystal and LFT connects the phase-locked-loop to an external low-pass filter.

The combination produces two clock domains for use on-chip, 48 MHz and 9/12/16 MHz. The 48 MHz clock is the master clock, but only a small part of the logic is clocked at this frequency. The majority is clocked at a lower rate which is determined by the mode of operation.

In USB mode, this clock is normally 12 MHz but may increase or decrease to 16 MHz or 9 MHz in order to synchronize with the USB serial stream. In parallel port mode, this clock runs at 16 MHz.

Figure 12. External Components with On-chip Oscillator and PLL



Reset

The device has four hardware reset modes and one software reset mode. The first uses an on-chip power-on-reset cell which generates a reset pulse during device power-up. The second uses a dedicated input pin. The third applies to parallel port mode. The fourth applies to USB mode. The USB core detects a host request for a reset. The fifth is a software reset generated by setting a register control bit TG_CMD[4].

Power Control

Individual control over the main power-consuming blocks are provided by the ANA_CTL register. The bias generators, ADC converters and analog amplifiers can be turned off to conserve power in standby.

For low power operation, the master clock can also be reduced to a minimum of 1 MHz in parallel port mode.

The clocks can also be suspended either in USB or parallel port mode using the USB host-suspend interface or the parallel port host-suspend operation. In either mode the AVR shuts down the on-chip oscillator. An external signal from the USB or the parallel port will re-start the device.

Interrupt Priority

The device supports seven interrupts in total. Table 3 gives information on the priority.

Table 3. USB Interrupt Priority

Interrupt	Description
1	USB (Highest priority)
2	USB suspend and resume
3(1)	Unused
4(1)	Unused
5(1)	Parallel port
6(1)	External interrupt
7(1)	Unused

Notes: 1. For more details on these interrupts, refer to the Parallel Port Mode datasheet, Literature Number 1372.

Memory Space

The AVR memory space is divided into three sections. The first allocation is for the AVR I/O space registers. These are the 32 8-bit working registers (0x0000 to 0x001F) and the I/O registers (0x0020 to 0x005F). The second is for the 2K x 8 SRAM scratch pad memory (0x0800 to 0x0FFF). The third is for the USB register map (0x1F00 to 0x1FFF).

Registers

AVR I/O Space Register Map

The 6-bit AVR address bus allows for 64 possible I/O registers with single-cycle accesses in conjunction with a read strobe (iore) and a write strobe (iowe). Data is transferred on two separate 8-bit buses, shared for both I/O and data memory accesses; one for reads (dbusin[7:0]) and one for writes (dbusout[7:0]). See “AVR I/O Registers” on page 24 for detailed descriptions.

Table 4. AVR I/O Address Map

Register	I/O Address		Memory Address	Type	Default	Function
IMGBUF_PREFTCH	0	0x00	0x20	Read	xxxxxxxxb	Image Data FIFO Prefetch
PP_CMD_IN	1	0x01	0x21	Read	xx000000b	Parallel Port Command from Host
PP_DATA_IN	2	0x02	0x22	Read	00000000b	Parallel Port Data from Host
PP_STAT_AVR	3	0x03	0x23	Bit 0: R/W Bit 1-5: Read	xx000000b	Parallel Port Status (writing bit 0 resets the status bit)
PP_CMD_OUT	4	0x04	0x24	Write	00000000b	Parallel Port Command to Host
PP_DATA_OUT	5	0x05	0x25	Write	00000000b	Parallel Port Data to Host
TG_CMD	9	0x09	0x29	Write	xx000000b	Timing Generator Command
TG_STAT_AVR_RD	10	0x0A	0x2A	Read	xxxxxx00b	Timing Generator Status
TG_STAT_AVR_WR	11	0x0B	0x2B	Write	xxxxxxx0b	Timing Generator Status Shadow
LINE_RD_MUL	16	0x10	0x30	R/W	xx000000b	Line Multiplier for FIFO Loading
END_COL	17	0x11	0x31	R/W	x1101011b	End Column Address
END_ROW_L	18	0x12	0x32	R/W	00110101b	End Row Address (low byte)
END_ROW_H	19	0x13	0x33	R/W	xxxxxxx1b	End Row Address (high byte)
SEL_START_ROW_L	20	0x14	0x34	R/W	00000000b	Start Row Select (low byte)
SEL_START_ROW_H	21	0x15	0x35	R/W	xxxxxxx0b	Start Row Select (high byte)
RST_START_ROW_L	22	0x16	0x36	R/W	00000000b	Start Row Reset (low byte)
RST_START_ROW_H	23	0x17	0x37	R/W	xxxxxxx0b	Start Row Reset (high byte)
START_COL	24	0x18	0x38	R/W	x0000000b	Start Column Address
IMAGE_CAPTURE_MODE	25	0x19	0x39	R/W	00000000b	Image Capture Mode
LED_INT	26		0x3A	R/W	10000000b	LED Intensity
ANA_CTL	27	0x1B	0x3B	R/W	xxx00000b	Analog Control Register
GAINB	28	0x1C	0x3C	R/W	xx000000b	Gain Right
GAING	29	0x1D	0x3D	R/W	xx000000b	Gain Center
GAIN_MSTR	30	0x1E	0x3E	R/W	xxxxxx00b	Gain Global
GAINR	31	0x1F	0x3F	R/W	xx000000b	Gain Left
OFFB	32	0x20	0x40	R/W	xxx00000b	Offset Right
OFFG	33	0x21	0x41	R/W	xxx00000b	Offset Center
OFFR	34	0x22	0x42	R/W	xxx00000b	Offset Left

Table 4. AVR I/O Address Map (Continued)

Register	I/O Address		Memory Address	Type	Default	Function
TEST_MODE	35	0x23	0x43	R/W	00000000b	Test Modes
UART	36	0x24	0x44	Bit 0: R/W bit Bit 1: Read only	xxxxxxx0b	UART Data
GPIO	41	0x29	0x49	R/W	00000000b	Control Port Data
GPIO_DIR	42	0x2A	0x4A	R/W	11111111b	Control Port Direction
FL_CMD_STAT	45	0x2D	0x4D	Read	00000000b	Flash Controller Status
FL_CMD_OP	46	0x2E	0x4E	R/W	00000000b	Flash Controller Opcode
FL_CMD_ADR1	47	0x2F	0x4F	R/W	00000000b	Flash Controller Address Register 1
FL_CMD_ADR2	48	0x30	0x50	R/W	00000000b	Flash Controller Address Register 2
FL_CMD_ADR3	49	0x31	0x51	R/W	00000000b	Flash Controller Address Register 3
FL_DBUF1	50	0x32	0x52	R/W	00000000b	Flash Controller Data Buffer 1
FL_DBUF2	51	0x33	0x53	R/W	00000000b	Flash Controller Data Buffer 2
FL_DLEN_L	52	0x34	0x54	R/W	00000000b	Flash Controller Data Buffer Length (low byte)
FL_DLEN_H	53	0x35	0x55	R/W	00000000b	Flash Controller Data Buffer Length (high byte)
	56	0x38	0x58			Reserved for Future AVR Release
	57	0x39	0x59			Reserved for Future AVR Release
	58	0x3A	0x5A			Reserved for Future AVR Release
RAMPZ	59	0x3B	0x5B	R/W	00000000b	AVR Extended Memory Pointer Register
	60	0x3C	0x5C			Reserved for Future AVR Release
SPL	61	0x3D	0x5D	R/W	00000000b	AVR Stack Pointer Low Register
SPH	62	0x3E	0x5E	R/W	00000000b	AVR Stack Pointer High Register
SREG	63	0x3F	0x5F			AVR Status Register

Table 5. Scratch Pad Memory Map

Memory Address	Function
0x0800 - 0x0FFF	2K x 8-bit memory

USB Mode Operation

The USB mode is selectable via the status of the OP_MODE pin. By default this pin is set to logic level 0 using an internal pull down to configure the device in USB Mode. It is therefore not shown in the pinout for the device in USB mode.

The device appears to the host as a USB slave imaging device with three endpoints.

- Endpoint 0 is a control endpoint with an 8-byte buffer
- Endpoint 1 is a bulk in endpoint with a 64-byte buffer
- Endpoint 2 is a interrupt endpoint with a 2-byte buffer

Table 6. USB Register Memory Map

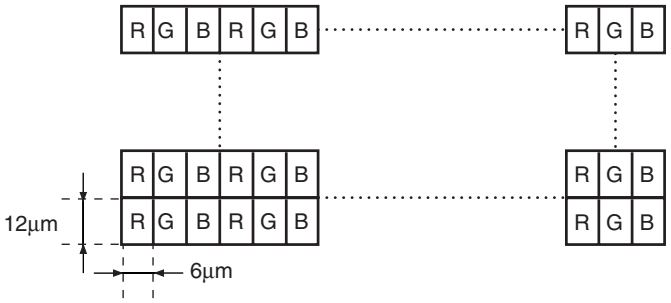
Register	Memory Address	Default	Function
FRM_NUM_H	0x1FFD	xxxxx000	Frame Number High Register
FRM_NUM_L	0x1FFC	xxxxx000	Frame Number Low Register
GLB_STATE	0x1FFB	xxxxx000	Global State Register
SPRSR	0x1FFA	xxxxx000	Suspend/Resume Register
SPRSIE	0x1FF9	xxxxxx00	Suspend/Resume Interrupt Enable Register
UISR	0x1FF7	00000000	USB Interrupt Status Register
UIAR	0x1FF5	xxxxx000	USB Interrupt Acknowledge Register
UIER	0x1FF3	xxxxx000	USB Interrupt Enable Register
FADDR	0x1FF2	00000000	Function Address Register
ENDPPGPG	0x1FF1	00000000	Function Endpoint Ping-Pong Register
ECR0	0x1FEF	0xxx0000	Endpoint0 Control Register
ECR1	0x1FEE	0xxx0000	Endpoint1 Control Register
ECR2	0x1FED	0xxx0000	Endpoint2 Control Register
CSR0	0x1FDF	x1110000	Endpoint0 Control and Status Register
CSR1	0x1FDE	x1110000	Endpoint1 Control and Status Register
CSR2	0x1FDD	x1110000	Endpoint2 Control and Status Register
FDR0	0x1FCF	00000000	FIFO 0 Data Register
FDR1	0x1FCE	00000000	FIFO 1 Data Register
FDR2	0x1FCD	00000000	FIFO 2 Data Register
FBYTE_CNT0_L	0x1FBF	00000000	Byte Count FIFO 0 Register [7:0]
FBYTE_CNT1_L	0x1FBE	00000000	Byte Count FIFO 1 Register [7:0]
FBYTE_CNT2_L	0x1FBD	00000000	Byte Count FIFO 2 Register [7:0]
FBYTE_CNT0_H	0x1FAF	00000000	Byte Count FIFO 0 Register [10:8]
FBYTE_CNT1_H	0x1FAE	00000000	Byte Count FIFO 1 Register [10:8]
FBYTE_CNT2_H	0x1FAD	00000000	Byte Count FIFO 2 Register [10:8]

Color Filtering and Color Recovery

The imager utilizes vertical stripes of pastel red, green and blue filtering laid over the pixels, which are rectangular with a height-to-width ratio of 2:1.

Black and white versions of the imager are available without the color filter layers but these still retain the rectangular pixels.

Figure 13. Vertical Stripe RGB Color Fiters



To produce full color information for each pixel, the user must perform color recovery externally to the AT76C402, either in hardware or software. When low-resolution mode is used, full color recovery may not yield improved image quality due to the subsampling utilized in the imager.

Full color information is available vertically, and thus color recovery can be achieved simply by processing nine adjacent pixels sequentially across the row in real time as they are read out of the imager.

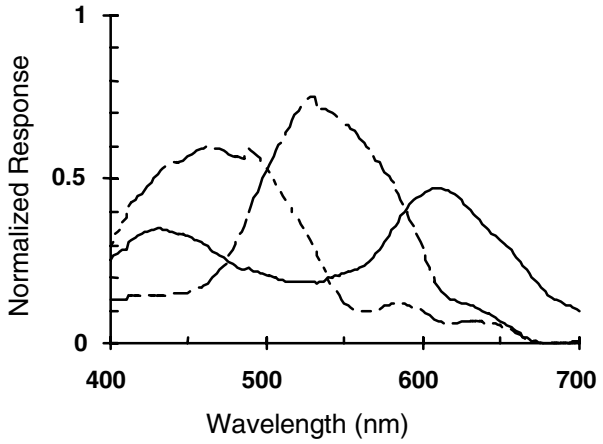
Optimum color recovery is achieved by using a simple Median Filter Transform (MFT). This color recovery method is covered under US and International patents (US Patents 4,663,665; 4,774,565 and 4,724,395) but a license to use this algorithm will be made available royalty free to be used ONLY in conjunction with the AT76C402. As a working estimate, color recovery can be performed using less than 20,000 gates of logic.

A full description of the color recovery method is available under NDA and a diskette with example Verilog and C-code is available on purchase of the device.

Table 7. Sensor Optical Performance

Description	Performance
Quantum efficiency of sensor pixel without color filters at 450 nm, 550 nm, 650 nm	> 0.40
Color filters	RGB color stripes
Optical conversion including color filters	> 40,000 e-/ux-s
Relative signal with same gain at 450 nm, 550 nm, 650 nm	Matched within 20%

Figure 14. Filter Response Characteristic Diagram – Color Filter Transmission with CM500 IR Cutoff



External Memory Interface

EEPROM Mode

At reset, a download state machine will read program code from an off-chip serial EEPROM and store it into a program storage RAM. The download state machine will load the entire RAM space, even if the code size is smaller than the full range. The microcontroller will be held in reset by the state machine until the download is complete. The microcontroller will then begin execution from location 0000 in the RAM.

Figure 15. EEPROM Read Data Timing Diagram

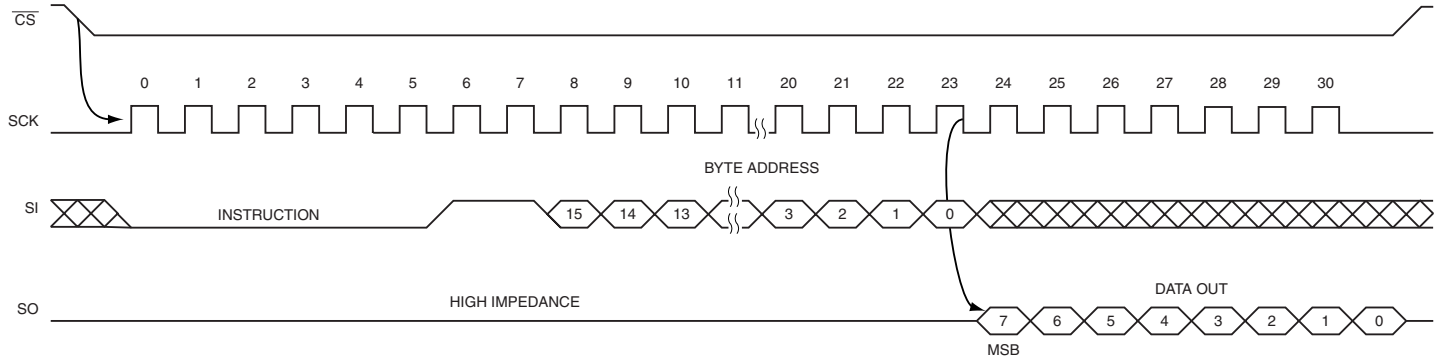


Figure 16. EEPROM Write Data Timing Diagram

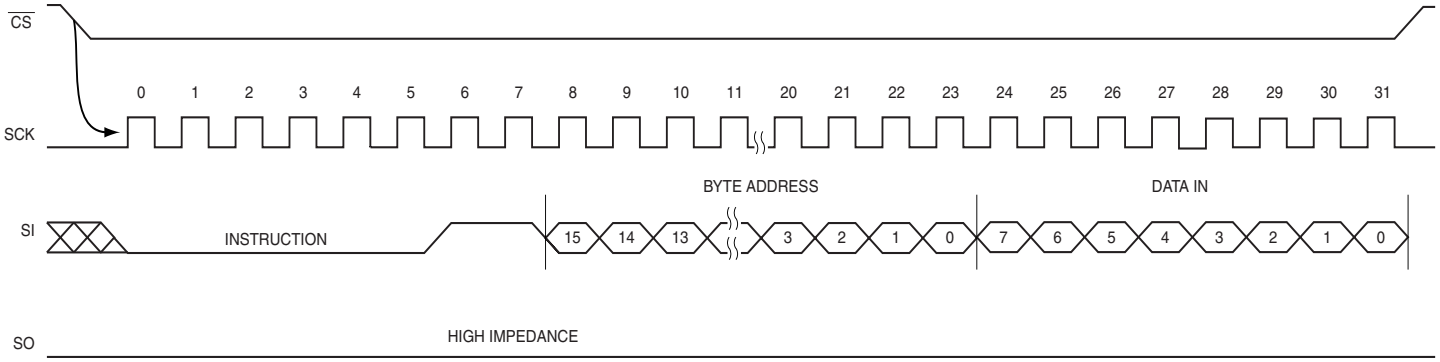
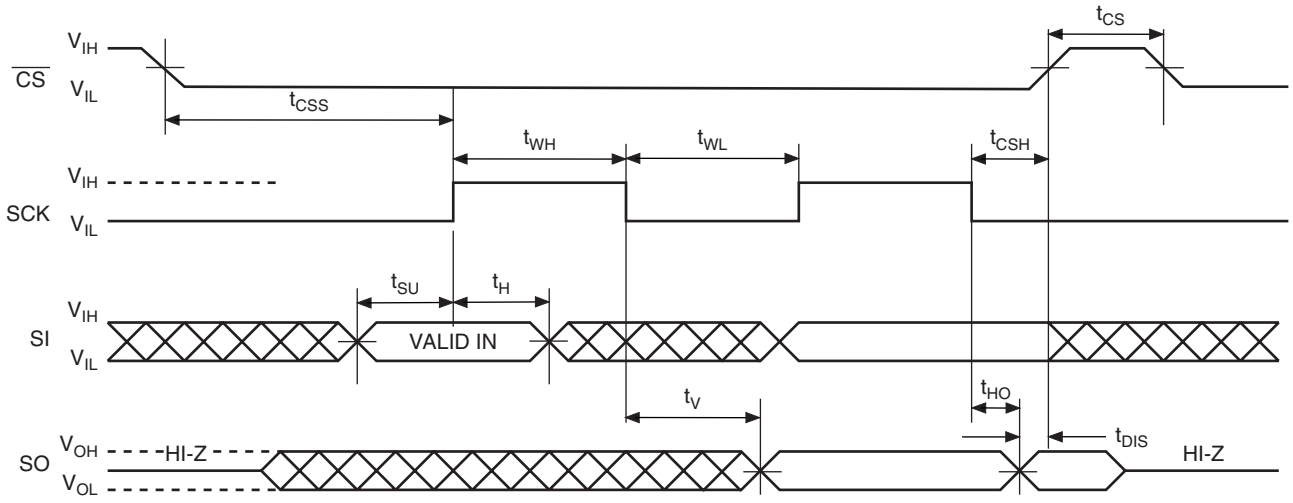


Figure 17. EEPROM Control Signal Timing Relationships



Flash Memory Mode

In Flash memory mode the SPI interface is managed by a controller capable of reading and writing an external Flash nonvolatile memory. The Flash memory is configurable in two different configurations; first as a memory that holds program code for download at power-up and second as a memory that can receive and send image data.

Timing diagrams are provided below. Note that there is a control signal (not shown in diagrams) that is not part of the EEPROM interface. A ready/busy (SPI_RDY) pin is driven low when the flash memory device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), is pulled low during programming operations, compare operations, and during page-to-buffer transfers. The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Figure 18. Main Memory Page Program through Buffers

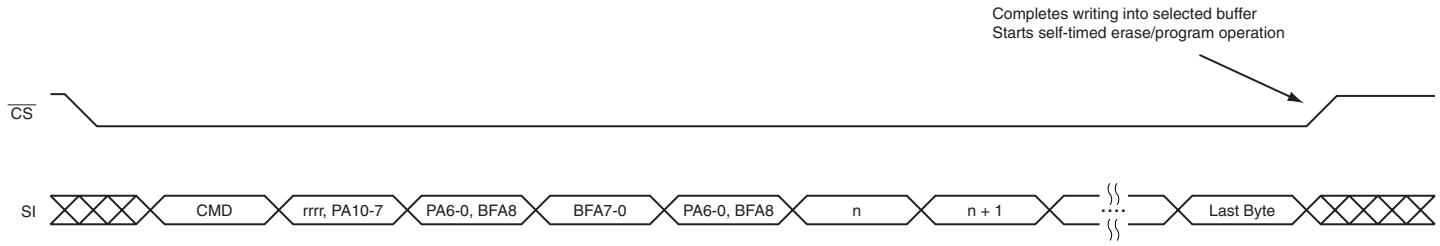


Figure 19. Buffer Write

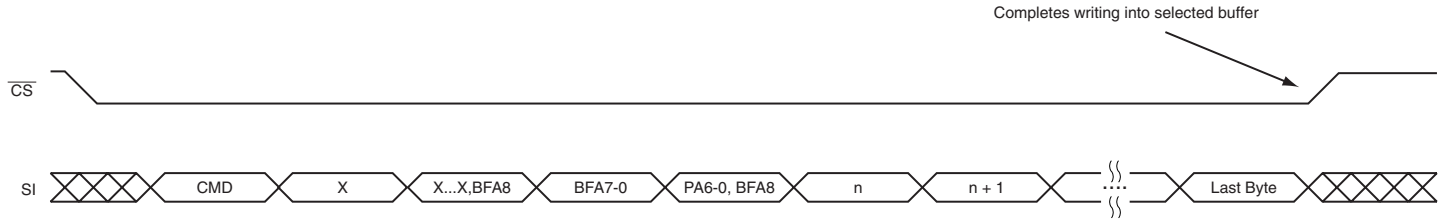


Figure 20. Main Memory Page Read

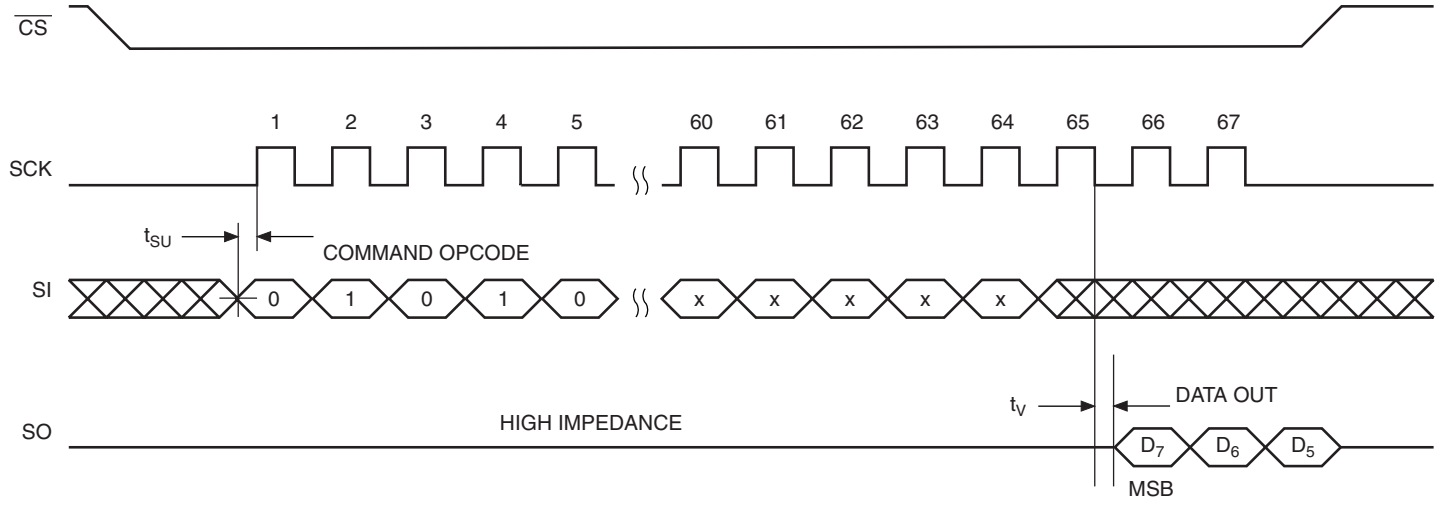


Figure 21. Buffer Read

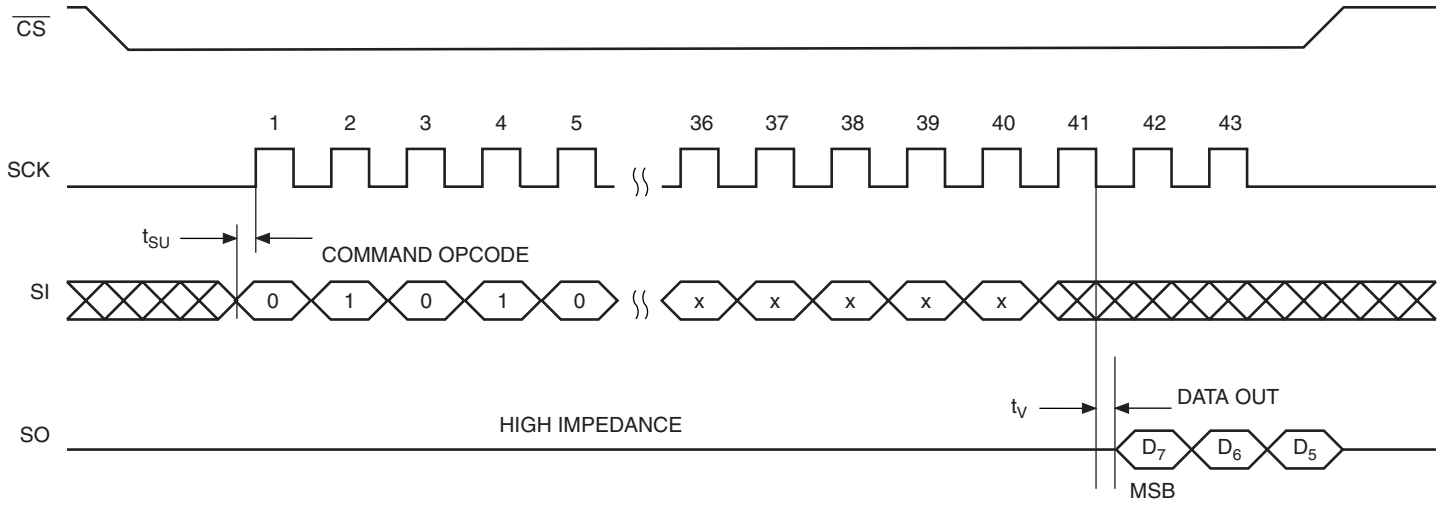
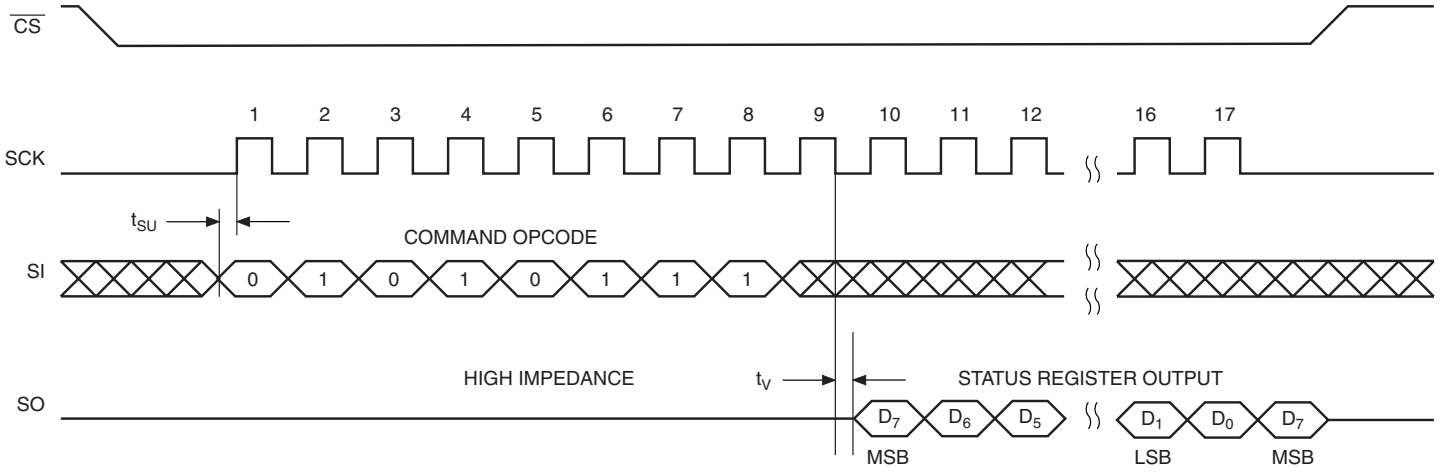


Figure 22. Status Register Read



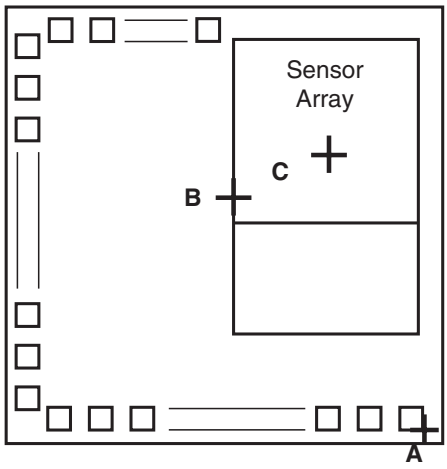
Suggested Lens Information

To be supplied.

Packaging Information

To be supplied.

Figure 23. Die and Sensor Location



A: Bottom right pad
B: Bottom left active pixel
C: Center of sensor active array

Note: Reference point (0, 0) is center of pad A.

	x	y
A to B	-1960	3259
A to C	-988	5119

Table 8. AT76C402 Pin and Pad Bond Locations

Pad Number	Pad Name	x (µm)	y (µm)
1	VDDDC	-2473	7514
2	GNDDC	-3985	7514
7	VSSAC	-5165	7514
8	VDDAC	-5369	7514
18	EE_PRGM	-7494	6944
19	XOUT	-7494	6846
20	XIN	-7494	6626
21	D0M	-7494	6520
22	D0P	-7494	6424
23	LFT	-7494	6310
30	VDDDC	-7493	5661
31	GNDDC	-7493	5571

Table 8. AT76C402 Pin and Pad Bond Locations

Pad Number	Pad Name	x (µm)	y (µm)
33	EE_SI	-7493	5389
35	EE_SCLK	-7493	5208
37	EE_CS	-7493	5027
39	EE_SO	-7493	4845
49	VDDAC	-7493	3938
50	VDDDC	-7493	3847
51	GNDAC	-7493	3757
52	GNDDC	-7493	3666
58	VDDAC	-7493	3122
59	GNDAC	-7493	3031
70	VDDAC	-7493	2024
71	GNDAC	-7493	1933
79	EE_MODE	-7493	1208
82	GNDVDC	-7493	823
83	VDDDC	-7493	718
91	GNDAC	-6782	0
92	VDDAC	-6676	0
97	VDD_REG	-6062	0
98	VDD5	-5837	0
99	AVDD_REG	-5634	0
100	AVDD5	-5468	0
101	AGND	-5243	0
102	AGND	-5143	0
109	AVDD	-3754	0
110	AGND	-3654	0
111	I_IAR	-2892	0
112	I_IAG	-2720	0
113	I_IAB	-2550	0
114	O_IAR	-2378	0
115	O_IAG	-2208	0
116	O_IAB	-2036	0
117	IREF	-1536	0
123	AVDD	-100	0
124	AVDD	0	0

Note: (0, 0) is center of pad in bottom right-hand corner. Refer to Figure 1 and Figure 23.

Electrical Specification

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Operating Supply Voltage	-0.3		4.6	V
V_{IN}	DC Input Voltage	-0.3		V_{DD} + 0.3	V
V_{OUT}	DC Output Voltage	-0.3		V_{DD} + 0.3	V
Temp	Operating Free Air Temp	-40		+85	°C

Table 10. DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Operating Supply Voltage	3.0	3.3	3.6	V
I_{DD}	Overall Supply Current			70	mA
V_{IH}	High Level Input Voltage	0.7 x V_{DD}		V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	0		0.3 x V_{DD}	V
V_{OH}	High Level Output Voltage	V_{DD} - 0.1			V
V_{OL}	Low Level Output Voltage			V_{SS} + 0.1	V
	Leakage Currents		100		nA
C_I load	Digital Input Cap Load		8		pF
C_O load	Digital Output Cap Load		43		pF

Notes:
1. I_{DD} is with no load on all outputs.
2. V_{IH} inputs are 5V-tolerant.
3. V_{OH} is with I_{OL} = 0.3 mA.
4. V_{OL} Low Level Output Voltage is with I_{OL} = 0.3 mA.
5. V_{OL} Leakage Currents for outputs and bidirectional pads.

AVR I/O Registers

IMGBUF_PREFTCH

Register Name: IMGBUF_PREFTCH

Description: One byte of image data from 8-bit FIFO

PP_CMD_IN

Register Name: PP_CMD_IN

Description: Parallel port command from 8-bit host

Bit Value	Description
0000000	Inactive
00000001	Take image
00000010	Abort
00000100	Upload parameters
00001000	Detect an image
00010000	Download parameters
00100000	Suspend

PP_DATA_IN

Register Name: PP_DATA_IN

Description: Parallel port data from 8-bit host

PP_STAT_AVR

Register Name: PP_STAT_AVR

Description: Parallel port status (8-bit)

Default: 00000000

Bit Value	Description
Bit 0 = 1	Packet Out (Read/Write-1-Modify)
Bit 1 = 1	Line in (Read only)
Bit 2 = 1	Host command pending (Read only)
Bit 3 = 1	Host data pending (Read only)
Bit 4 = 1	ASIC command pending (Read only)
Bit 5 = 1	ASIC data pending (Read only)

PP_CMD_OUT

Register Name: PP_CMD_OUT

Description: Parallel port command to 8-bit host. Note that any write to this register generates an interrupt to the host (signal B_pp_data[9]). Values are firmware defined.

PP_DATA_OUT

Register Name: PP_DATA_OUT

Description: Parallel port data to 8-bit host

TG_CMD

Register Name: TG_CMD

Description: Timing generator command

Bit Value	Definition
00000000	Idle
00000001	Read line (initiates line transfer to FIFO)
00000010	Start image readout
00000100	Frame reset (only in still mode)
00001000	Illumination LED on (only in still mode)
00010000	Abort readout (held while bit is high)
00100000	Enter sleep mode

TG_STAT_AVR_RD

Register Name: TG_STAT_AVR_RD

Description: Timing generator status

Bit Value		Definition
Bit 0	1	Line stored in image data FIFO
Bit 1	0	Parallel port mode
	1	USB mode

TG_STAT_AVR_WR

Register Name: TG_STAT_AVR_WR

Description: Timing generator status shadow

Bit Value	Definition
Bit 0 = 1	Modify bit 1 of TG_STAT_AVR_RD

LINE_RD_MUL

Register Name: LINE_RD_MUL

Description: Line multiplier for FIFO loading

Default Value: 0

Value: Number of additional line required on one side of the image data FIFO before pingponging to the other side. This must satisfy the inequality:

$$\mathrm{LINE\_RD\_MUL} + 1 > 64 / (3 \cdot (\mathrm{END\_COL} - (\mathrm{START\_COL} + 1)))$$

END_COL

Register Name: END_COL
Description: End column address
Default Value: x1101011

Bit Value	Description
x0000000	Pixel triplet corresponding to columns 1, 2, 3
x0000001	Pixel triplet corresponding to columns 4, 5, 6
...	...
x1101010	Pixel triplet corresponding to columns 319, 320, 321
x1101011	Pixel triplet corresponding to columns 322, 323, 324
x1101100	Out of range
...	...

END_ROW_L

Register Name: END_ROW_L
Description: End row address (low byte)
Default Value: 00110101

Bit Value	Description
00000000	Row 1
00000001	Row 2
...	...
00110100	Row 309
00110101	Row 310
00110110	Out of range
...	...

END_ROW_H

Register Name: END_ROW_H
Description: End row address (high byte)
Default Value: xxxxxxx1

Bit Value	Description
xxxxxxx0	Row 1
xxxxxxx0	Row 2
...	...
xxxxxxx1	Row 309
xxxxxxx1	Row 310
xxxxxxx1	Out of range
...	...

SEL_START_ROW_L

Register Name: SEL_START_ROW_L
Description: Start of active row (low byte)
Default Value: 00000000

Bit Value	Description
00000000	Row 1
00000001	Row 2
...	...
00110100	Row 309
00110101	Row 310
00110110	Out of range
...	...

SEL_START_ROW_H

Register Name: SEL_START_ROW_H
Description: Start of active row (high byte)
Default Value: 00000000

Bit Value	Description
xxxxxxx0	Row 1
xxxxxxx0	Row 2
...	...
xxxxxxx1	Row 309
xxxxxxx1	Row 310
xxxxxxx1	Out of range
...	...

RST_START_ROW_L

Register Name: RST_START_ROW_L
Description: Start of reset row (low byte)
Default Value: 00000000

Bit Value	Description
00000000	Row 0
00000001	Row 1
...	...
00110100	Row 308
00110101	Row 309
00110110	Out of range
...	...

RST_START_ROW_H

Register Name: RST_START_ROW_H
Description: Start of reset row (high byte)
Default Value: 00000000

Bit Value	Description
xxxxxxx0	Row 0
xxxxxx0	Row 1
...	...
xxxxxxx1	Row 308
xxxxxxx1	Row 309
xxxxxxx1	Out of range
...	...

START_COL

Register Name: START_COL
Description: Start column address
Default Value: x0000000

Bit Value	Description
x0000000	Pixel triplet corresponding to columns 1, 2, 3
x0000001	Pixel triplet corresponding to columns 4, 5, 6
...	...
x1101010	Pixel triplet corresponding to columns 319, 320, 321
x1101011	Pixel triplet corresponding to columns 322, 323, 324
x1101100	Out of range
...	...

IMAGE_CAPTURE_MODE

Register Name: IMAGE_CAPTURE_MODE
Description: Image capture mode
Default Value: 00000000

Bit Value		Description
Bit 0	0	Truncated data
	1	Lookup table
Bit 1	0	Lookup table A
	1	Lookup table B
Bit 2	0	Still mode
	1	Continuous mode
Bit 3	0	Illumination LED active
	1	Illumination LED powered down
Bit 4	0	BUF_12M clock to external clock pin
	1	BUF_12M/2 clock to external clock pin
Bit 5	0	Parallel port not in program counter mode
	1	Program counter output
Bit 6	0	Illumination LED pulsed
	1	Illumination LED continuous
Bit 7	0	Indicator LED on
	1	Indicator LED off

LED_INT

Register Name: LED_INT
Description: LED intensity
Default Value: 10000000

Bit Value	Description
00000000	Zero
00000001	1/255th full brightness
00000010	2/255th full brightness
...	...
11111110	254/255th full brightness
11111111	Full brightness

ANA_CTL

Register Name: ANA_CTL

Description: Analog control register

Bit Value	Description
Bit 0 = 1	Power down A-to-D
Bit 1 = 1	Power down image array
Bit 2 = 1	Power down gain and offset
Bit 3 = 1	Test mode
Bit 4 = 1	Gamma mode
Bit 7:5	Don’t care

GAINB

Register Name: GAINB

Description: Gain left

Default Value: 00000000

Bit Value	Definition
xx000000	1.00x gain
xx000001	1.03x gain
xx000010	1.06x gain
xx000011	1.09x gain
xx000100	1.12x gain
...	...
xx111110	2.86x gain
xx111111	2.89x gain

GAING

Register Name: GAING
Description: Gain center
Default Value: 00000000

Bit Value	Definition
xx000000	1.00x gain
xx000001	1.03x gain
xx000010	1.06x gain
xx000011	1.09x gain
xx000100	1.12x gain
...	...
xx111110b	2.86x gain
xx111111b	2.89x gain

GAIN_MSTR

Register Name: GAIN_MSTR
Description: Gain global
Default Value: 00000000

Bit Value	Definition
xxxxxx00	1x gain
xxxxxx01	2x gain
xxxxxx10	4x gain
xxxxxx11	8x gain

GAINR

Register Name: GAINR
Description: Gain right
Default Value: 00000000

Bit Value	Definition
xx000000	1.00x gain
xx000001	1.03x gain
xx000010	1.06x gain
xx000011	1.09x gain
xx000100	1.12x gain
...	...
xx111110	2.86x gain
xx111111	2.89x gain

OFFB

Register Name: OFFB
Description: Offset left
Default Value: 00000000

Bit Value	Definition
xxx00000	-2.4 µA
xxx00001	-2.4 µA
...	...
xxx01100	0 µA
...	...
xxx11110	+3.6 µA
xxx11111	+3.8 µA

OFFG

Register Name: OFFG
Description: Offset center
Default Value: 00000000

Bit Value	Definition
xxx00000	-2.4 µA
xxx00001	-2.4 µA
...	...
xxx01100	0 µA
...	...
xxx11110	+3.6 µA
xxx11111	+3.8 µA

OFFR

Register Name: OFFR
Description: Offset right
Default Value: 00000000

Bit Value	Definition
xxx00000	-2.4 µA
xxx00001	-2.4 µA
...	...
xxx01100	0 µA
...	...
xxx11110	+3.6 µA
xxx11111	+3.8 µA

TEST_MODE

Register Name: TEST_MODE

Description: Engineering and manufacturing test modes

Default Value: 00000000

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal operation	x	x	x	x	x	0	0	0
PLL test mode	x	x	x	x	x	0	0	1
SPI test mode	x	x	x	x	x	0	1	0
LUT ROM	x	x	x	x	x	0	1	1
AVR & USB scan	x	x	x	x	x	1	0	0
Not used	0	0	x	x	x	1	0	1
ISA column counter only	0	1	x	x	x	1	0	1
ISA row select counter only	1	0	x	x	x	1	0	1
ISA row reset counter only	1	1	x	x	x	1	0	1
ISA control signals	0	x	x	x	x	1	1	0
ISA control signals with inverted data	1	x	x	x	x	1	1	0

UART

Register Name: UART

Description: UART port data. The receive input is synchronized to the internal 12/16 MHz clock rising edge.

Bit Value	Definition
Bit 0	Pin TX (output)
Bit 1	Pin RX (input)

GPIO

Register Name: GPIO

Description: Control port data (bidirectional with status as input or output set by GPIO_DIR register). GPIO inputs are synchronized to the internal 12/16 MHz clock rising edge.

Bit Value	Description
Bit 0	Pin CP<0>
Bit 1	Pin CP<1>
Bit 2	Pin CP<2>
Bit 3	Pin CP<3>
Bit 4	Pin CP<4>
Bit 5	Pin CP<5>
Bit 6	Pin CP<6>
Bit 7	Pin CP<7>

GPIO_DIR

Register Name: GPIO_DIR

Description: Control port direction (specifies whether corresponding bit in GPIO is read or write

Bit Value			Description
Bit 0	Pin CP<0>	0	Output
		1	Input
Bit 1	Pin CP<1>	0	Output
		1	Input
Bit 2	Pin CP<2>	0	Output
		1	Input
Bit 3	Pin CP<3>	0	Output
		1	Input
Bit 4	Pin CP<4>	0	Output
		1	Input
Bit 5	Pin CP<5>	0	Output
		1	Input
Bit 6	Pin CP<6>	0	Output
		1	Input
Bit 7	Pin CP<7>	0	Output
		1	Input

FL_CMD_STAT

Register Name: FL_CMD_STAT

Description: Flash controller status. See “External Memory Interface” on page 18 for timing diagrams.

Bit Value		Description
Bit 0	0	Ready
	1	Busy
Bit 1	1	Done
Bit 3	1	Data buffer 1 busy
Bit 4	1	Data buffer 2 busy
Bit 6	0	Write
	1	Read
Bit 7	1	Start

FL_CMD_OP

Register Name: FL_CMD_OP

Description: Flash controller opcode. See “External Memory Interface” on page 18 for timing diagrams.

Opcodes	Description
0x52	Main memory page read
0x53	Main memory page to buffer 1 transfer
0x54	Buffer 1 read
0x55	Main memory page to buffer 2 transfer
0x56	Buffer 2 read
0x57	Status register
0x58	Auto page rewrite through buffer 1
0x59	Auto page rewrite through buffer 2
0x60	Main memory page to buffer 1 compare
0x61	Main memory page to buffer 2 compare
0x82	Main memory page program through buffer 1
0x83	Buffer 1 to main memory page program with built-in erase
0x84	Buffer 1 write
0x85	Main memory page program through buffer 2
0x86	Buffer 2 to main memory page program with built-in erase
0x87	Buffer 2 write
0x88	Buffer 1 to main memory page program without built-in erase
0x89	Buffer 2 to main memory page program without built-in erase

FL_CMD_ADR1

Register Name: FL_CMD_ADR1

Description: Flash controller address register 1

FL_CMD_ADR1

Register Name: FL_CMD_ADR2

Description: Flash controller address register 2

FL_CMD_ADR1

Register Name: FL_CMD_ADR3

Description: Flash controller address register 3

FL_DBUF1

Register Name: FL_DBUF1

Description: Flash controller data buffer 1

FL_DBUF2

Register Name: FL_DBUF2
Description: Flash controller data buffer 2

FL_DLEN_L

Register Name: FL_DLEN_L
Description: Flash controller data buffer length (low byte)

FL_DLEN_H

Register Name: FL_DLEN_H
Description: Flash controller data buffer length (high byte)

RAMPZ

Register Name: RAMPZ
Description: AVR extended memory pointer register
Default: 00000000b

Bit Value		Definition
Bit 0	0	Low memory page (0x0000 - 0x7FFF)
	1	High memory page (0x8000 - 0xFFFF)

SPL

Register Name: SPL
Description: AVR pointer low register
Default: 00000000b

SPH

Register Name: SPH
Description: AVR pointer high register
Default: 00000000b

SREG

Register Name: SREG

Description: AVR status register

Bit Value			Description
Bit 0	Carry Flag	1	Carry in arithmetic or logic operation
Bit 1	Zero Flag	1	Zero result after arithmetic or logic operation
Bit 2	Negative Flag	1	Negative result after arithmetic or logic operation
Bit 3	Two's Complement Overflow Flag	1	Two's complement arithmetic
Bit 4	Sign Bit	1	Exclusive or between negative flag & two's complement overflow flag
Bit 5	Half-carry Flag	1	Half carry in arithmetic operation
Bit 6	Bit Copy Storage	1	Storage location for bit copy operation
Bit 7	Global Interrupt Enable	0	Interrupts disabled
		1	Interrupts enabled

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

1360A–06/00/0M