Features

- Servo Processing Unit (SPU), Using Dedicated 16-bit Instruction Cycle AVR® RISC Cores (3), Giving 120 MIPS Maximum Processing Power with 40 MHz SYSCLK
- SPU Includes 17 x 17 Single-clock Cycle MAC
- On-chip Debugger Monitor for Program Development (OCDM)
- 8K Words Program RAM
- 4K Bytes Data RAM
- On-chip Clock Frequency Synthesizer with Output Clock Buffers for AT78C1501 Controller
- On-chip S/H and WCS Timing State Machine (TSM) for Conversion of Focus, Tracking and SUM Signals
- 10-bit 1.2 µsec ADC with six-channel MUX
- Synchronized ADC Conversions with SPU Interrupt Service Routine
- Three Fast 10-bit 500 nsec (rise time) DACs for Servo Loops and Adjustments
- Three 8-bit DACs for Offset Adjustment and Spin Loop
- Bandgap ADC and DAC Midpoint Reference Outputs
- SPU Implemented Spindle Speed Control
- Spindle Interface Logic and Hardware Support for Both CAV and CLV Spindle Control Modes
- Eight General Purpose I/O Pins
- SPU Servo Control of Focus, Fine Track, Coarse Track and Tray Load Motors
- High-speed Track Counter for Accurate High-speed Track Counts (1.4 MHz when used with AT78C1503 Read Channel)
- Lower Power Operations with 3.3V Core and 5V Tolerant I/Os
- 8-bit Data and 14-bit Address Controller/Microprocessor Interface
- 3-pin Universal Serial Port Interface to Program Read Channel and Power Devices
- Power Management
- On-chip UART to Access OCDM Unit

Description

The Atmel AT78C1502 high-performance servo controller fully integrates all of the control and demodulation functions for DVD and CD, optical/mechanical systems. Packaged in 128-lead TQFP and fabricated in 0.35 micron CMOS, the device operates on a 3.3V logic/analog supply and provides 5V tolerance for digital I/O. An AVR-based Servo Processing Unit (SPU) embedded in the device provides programmable control of spindle speed, coarse and fine tracking, focus, sled, draw motor and tilt. The three parallel programmable AVR microcontrollers in the SPU are the heart of the system, offering a range of servo sample rates. With only a 40 MHz system clock, 120 MIPS of processing power is provided. Real-time notch filters can also be calculated. Fast 10-bit DACs provide real-time control of servo loops and other system adjustments. A universal serial port and many general purpose I/Os are provided.

AVR0 is the master AVR of the three microcontrolloers, communicating with AVR1, AVR2 and the ARMTDMI in the AT78C1501 interface controller and to the AT78C1503 read channel. An On-Chip Debugger Monitor (OCDM) is offered to enable programmers to easily observe theeffect of changes to code on each AVR.

System-level evaluation boards are available with development code in both C and native code for basic operation of all servos. Simple changes to the code allow any mechadeck to be interfaced to the AT78C1502.

DVD/CD Servo

AT78C1502

Rev. 2050A–DVD–07/02

Figure 1. DVD System Block Diagram

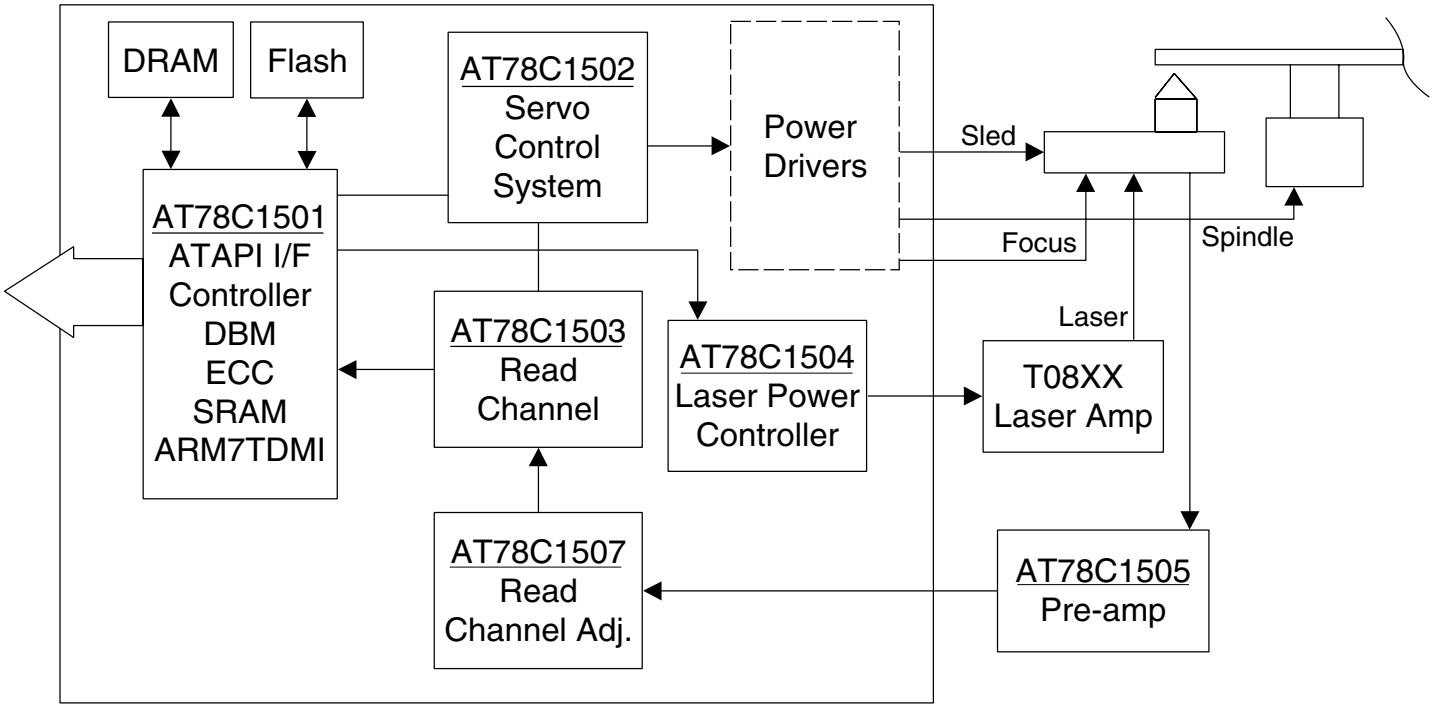
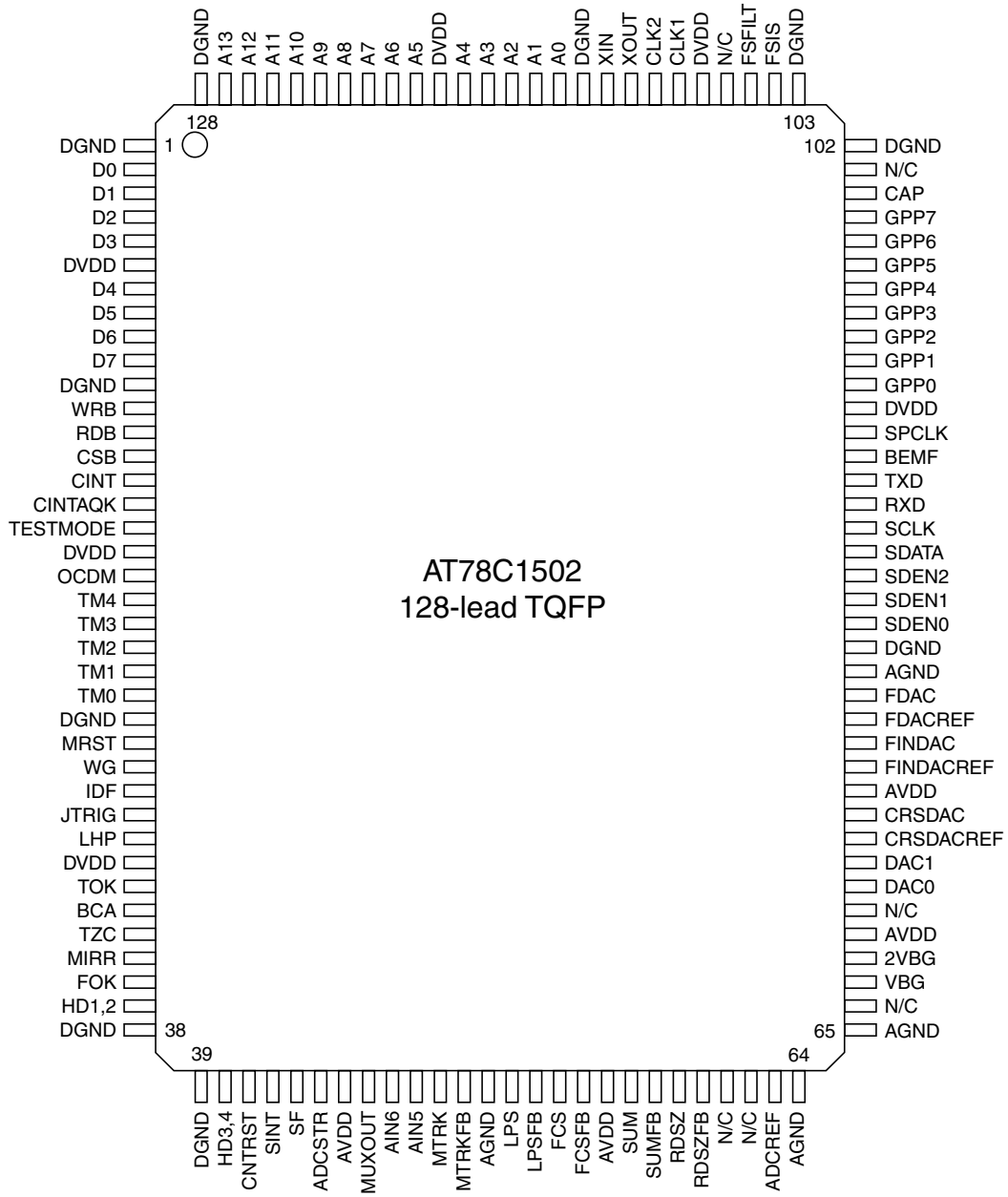


Figure 2. Pin-out



External Pin Definition

P = Power or ground, B = Bidirectional, I = Digital Input, O = Digital Output.

AI = Analog Input, AO = Analog Output.

Table 1. External Pin Definition

Pin #	Symbol	Type	Description
1	DGND	P	Digital Ground
2	D0	B	Data Bus
3	D1	B	Data Bus
4	D2	B	Data Bus
5	D3	B	Data Bus
6	DVDD	P	Digital VDD
7	D4	B	Data Bus
8	D5	B	Data Bus
9	D6	B	Data Bus
10	D7	B	Data Bus
11	DGND	P	Digital Ground
12	WRB	I	Chip Write Select
13	RDB	I	Chip Read Select
14	CSB	I	Chip Select Input
15	CINT	I	Interrupt Input from Controller
16	CINTACK	O	Controller Interrupt Acknowledge
17	TMODE	I	Test Mode Select Input – Active-low
18	DVDD	P	Digital VDD
19	OCDM_ENAB	I	On-chip Debug/Monitor Mode
20	TM4/MUX4	I	Test Mode Select
21	TM3/MUX3	I	Test Mode Select Input/MUX Output
22	TM2/MUX2	I	Test Mode Select Input/MUX Output
23	TM1/MUX1	I	Test Mode Select Input/MUX Output
24	TM0/MUX0	I	Test Mode Select Input/MUX Output
25	DGND	P	Digital Ground
26	MRST	I	Master Reset Input
27	WG	I	Write Gate Input from Controller
28	IDF	I	I/D Field Input from Controller
29	JTRIG	I	Jump Trigger Input from Controller
30	LHP	I	Laser High Power Input from Controller
31	DVDD	P	Digital Power
32	TOK	I	Track OK Input from Read Channel
33	BCA	I	Burst Cutting Area (Defect Flag Input)

Table 1. External Pin Definition (Continued)

Pin #	Symbol	Type	Description
34	TZC	I	Track Zero Crossing from Read Channel
35	MIRR	I	Mirror Input from Read Channel
36	FOK	I	Focus OK Signal from Read Channel
37	HD1,2	I	Header 1, 2 Input from Read Channel
38	DGND	P	Digital Ground
39	DGND	P	Digital Ground
40	HD3,4	I	Header 3, 4 Input from Read Channel
41	CNTRST	I	TSM Counter Reset Signal
42	SINT	O	Servo Interrupt Output to Controller
43	SF	O	Servo Fault Output to Controller
44	ADCSTR	O	ADC Strobe Output from TSM
45	AVDD	P	Analog VDD
46	MUX_OUT	AO	Analog MUX Output
47	AIN6	AI	Analog Input to MUX
48	AIN5	AI	Analog Input to MUX
49	MTRK	AI	MUXed Track Track/Hold Input
50	MTRKFB	AI	MUXed Track Filter Input
51	AGND	P	Analog Ground
52	LPS	AI	Lens Position Sensor Track/Hold Input
53	LPS	AI	Lens Position Sensor Filter Input
54	FCS	AI	Focus Error Signal Track/Hold Input
55	FCSF	AI	Focus Error Signal Filter Input
56	AVDD	P	Analog VDD
57	SUM	AI	Slow Sum Track/Hold Input
58	SUMF	AI	Slow Sum Input Filter
59	RDSZ	AI	Read Size Input
60	RDSZF	AI	Read Size Input Filter
61	N/C		No Connect
62	N/C		No Connect
63	ADCREF	AI	Reference I/P for ADC
64	AGND	P	Analog GND
65	AGND	P	Analog GND
66	N/C		No Connect
67	VBG	AO	Bandgap Output Voltage
68	2VBG	AO	2*Bandgap Output Voltage
69	AVDD	P	Analog VDD

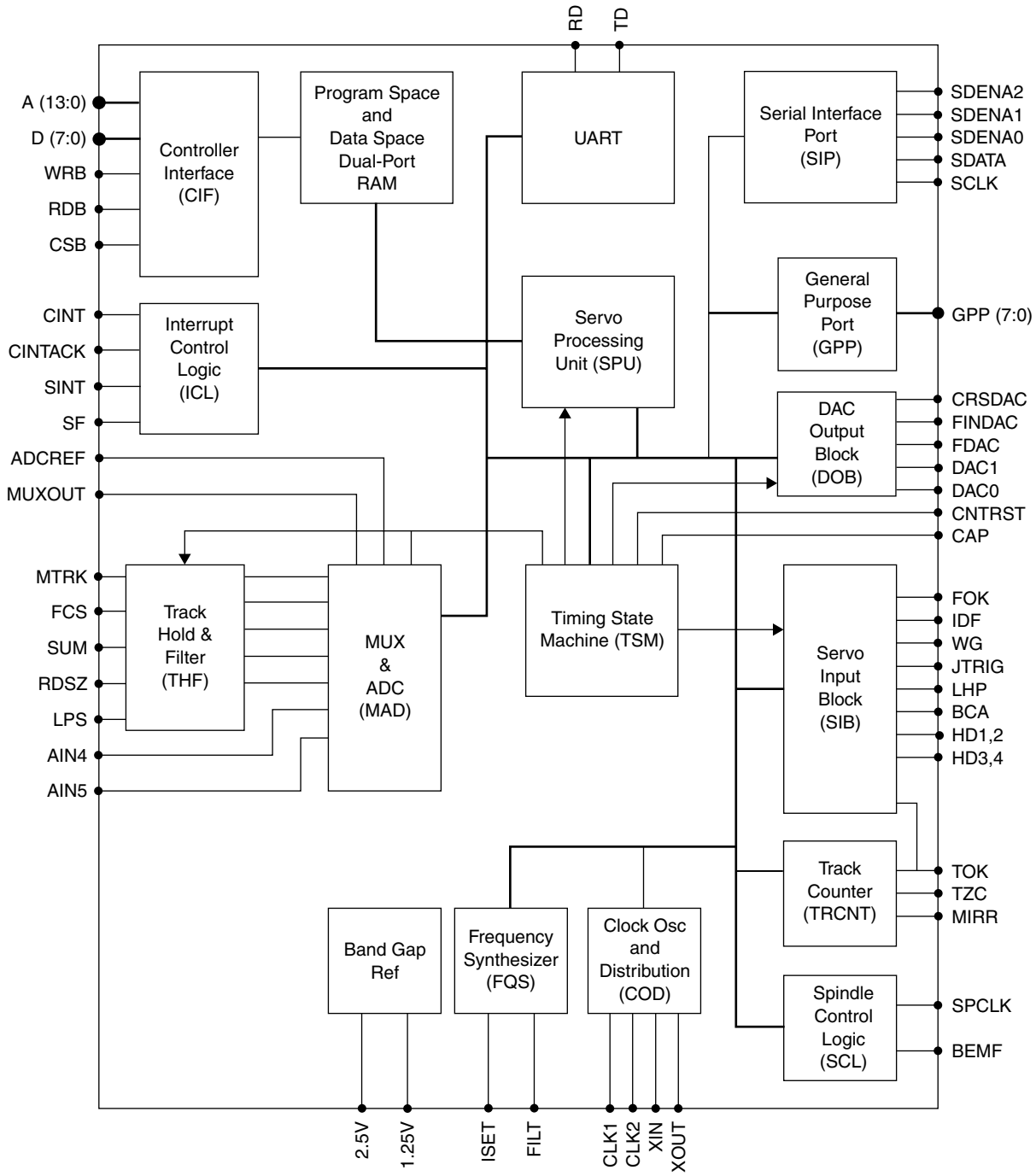
Table 1. External Pin Definition (Continued)

Pin #	Symbol	Type	Description
70	N/C		No Connect
71	DAC0	AO	8-bit Offset DAC Output
72	DAC1	AO	8-bit Offset DAC Output
73	CRSDAC	AO	10-bit Coarse Tracking DAC
74	CRSDACREF	AI	Coarse DAC Ref Input
75	AVDD	P	Analog VDD
76	FINDAC	AO	10-bit Fine Tracking DAC
77	FINDACREF	AI	Fine DAC Ref Input
78	FDAC	AO	10-bit Focus DAC
79	FDACREF	AI	Focus DAC Ref Input
80	AGND	P	Analog GND
81	DGND	P	Digital GND
82	SDEN0	O	Serial Data Enable #0
83	SDEN1	O	Serial Data Enable #1
84	SDEN2	O	Serial Data Enable #2
85	SDATA	B	Serial Data
86	SCLK	O	Serial CLK
87	RXD	I	UART Receive Data Input
88	TXD	O	UART Transmit Data Output
89	BEMF	I	Back EMF Zero Crossing Input
90	SPCLK	O	Spin Pseudo Register Output
91	DVDD	P	Digital VDD
92	GPP0	B	General Purpose I/O Port Bit
93	GPP1	B	General Purpose I/O Port Bit
94	GPP2	B	General Purpose I/O Port Bit
95	GPP3	B	General Purpose I/O Port Bit
96	GPP4	B	General Purpose I/O Port Bit
97	GPP5	B	General Purpose I/O Port Bit
98	GPP6	B	General Purpose I/O Port Bit
99	GPP7	B	General Purpose I/O Port Bit
100	CAP	I	External Event Capture
101	N/C		No Connect
102	DGND	P	Digital Ground
103	DGND	P	Digital Ground
104	FSIS	I	Frequency Synthesizer Iset
105	FSFILT	I	Frequency Synthesizer Filter

Table 1. External Pin Definition (Continued)

Pin #	Symbol	Type	Description
106	N/C		No Connect
107	DVDD	P	Digital VDD
108	CLK1	O	Clock 1 Output
109	CLK2	O	Clock 1 Output
110	XOUT	O	Crystal Out Connection
111	XIN	I	Crystal Input/Clock Input
112	DGND	P	Digital Ground
113	A0	I	Address Bus Input
114	A1	I	Address Bus Input
115	A2	I	Address Bus Input
116	A3	I	Address Bus Input
117	A4	I	Address Bus Input
118	DVDD	P	Digital VDD
119	A5	I	Address Bus Input
120	A6	I	Address Bus Input
121	A7	I	Address Bus Input
122	A8	I	Address Bus Input
123	A9	I	Address Bus Input
124	A10	I	Address Bus Input
125	A11	I	Address Bus Input
126	A12	I	Address Bus Input
127	A13	I	Address Bus Input
128	DGND	P	Digital GND

Figure 3. Block Diagram



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2050A–DVD–07/02